Investigation of Electric Double Layer Effects at Li_3PO_4 Li^+ Solid Electrolyte Thin Film Interfaces Using a Field-Effect Transistor with Al-doped SiC (0001) Single Crystal

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We developed a Li^+ electrolyte-gated electric double layer transistor (EDLT) using Al-doped SiC (0001) single crystal as the channel material. Thanks to the high tolerance of SiC single crystal to plasma irradiation, the Al-doped SiC EDLT was successfully fabricated with RF sputtered Li_3PO_4 Li^+ solid electrolyte thin film, which was previously difficult due to plasma-induced damage to the semiconductor channel. The EDLT operation of the device was confirmed by observing a 75% resistance change in the transfer characteristics. Hall measurements were employed to evaluate carrier density changes and directly investigate the behavior of the EDL at the interface. The calculated capacitance revealed contributions from both the EDL capacitance and depletion layer capacitance, indicating that the depletion layer formed on the SiC channel surface prevented accurate evaluation of EDL capacitance. For accurate EDL capacitance measurement, generating an accumulation layer on the surface of the semiconductor channel is found to be essential.

1. Introduction

All-solid-state batteries consisting of inorganic materials are seen as a promising path for next-generation battery technology, essential for achieving carbon neutrality and possessing diverse applications, notably in electric vehicles.[1)] Despite the high expectations for their superior energy density and safety features, a major barrier to their widespread adoption lies in the output reduction caused by elevated interface resistance at the lithium solid electrolyte/electrode interface. One of the suspected causes of this interface resistance is the electric double layer (EDL) effect (or space charge layer), triggered by variations in Li^+ concentration near the interface.[2-7)] This effect involves the accumulation of charged ions from the electrolyte at the electrode interface, generating a layer of positive or negative charge, with the opposing charge distributed onto the electrode, resulting in an overall charge distribution near the interface. While the formation of an EDL near the electrode interface is well-documented in liquid electrolytes, its occurrence in solid electrolyte systems, known for their possible mixed ion/electron conductivity, presents a complexity due to the participation of multiple charge carriers.[8,9)] Consequently, discerning the EDL effect of solid electrolytes becomes challenging. Furthermore, recent

advances in applying solid electrolyte interfacial functions to state-of-art neuromorphic computing or physical properties tuning urge investigation of ionic behavior near the solid electrolyte interfaces.[10-15)]

The present authors devised a new method to evaluate the charge of the electric double layer on a solid electrolyte surface through Hall measurements, leveraging the mechanism of a EDL transistor (EDLT) and the properties of chemically inert hydrogenated diamond.[16,17)] A lithium solid electrolyte was used for the dielectric part of the EDLT, and diamond, which does not react with Li^+ and does not insert or desert ions, was used for the semiconductor (channel). This configuration allows the charge induced by the EDL effect of the solid electrolyte to be detected as a variation in the electron carrier density on the diamond surface through Hall effect. However, hydrogenated diamond has the disadvantage that plasma irradiation associated with sputter deposition and heat treatment at high temperatures damages the terminated hydrogen, which limits the types of electrolytes and deposition methods applied to the evaluation.

In the present study, we fabricated devices using Al-doped 4H-Silicon Carbide (0001) wafers as channel materials, which can withstand the sputtering process and high-temperature conditions involved in the electrolyte thin-film deposition. 4H-SiC is a compound semiconductor composed of Si and C, well known for its thermal and chemical stability. While the typical semiconductor Si has a thermal resistance limit of around 150 °C leading to thermal runaway,[18)] SiC semiconductors have been confirmed to operate stably even at temperatures above 250 °C.[19)] This is due to its wide bandgap of 3.26 eV,[20)] which minimizes carrier generation from heat, resulting in a lower leakage current. We deposited Li_3PO_4, a lithium solid electrolyte widely used in solid-state batteries,[2-4)] onto the channel material using the sputtering method. The channel resistance measurements indicated minimal damage caused by the sputtering process. Furthermore, resistance changes of 75% during gate voltage (V_g) sweeps confirmed the operation of the device as an EDLT. SiC single crystal is so chemically inert that we need high energy ion-implantation above several tens kV and a post-annealing at a very high temperature of 1700 degrees C for doping. Since the present experimental condition is with a very low voltage below 3 V at RT, the insertion and desorption of Li ions is unlikely to occur. Evaluation of carrier density changes through Hall measurements provided insights into the EDL formation and its behavior at solid electrolyte interfaces. Based on these findings, we discuss the suitability of materials for EDL formation and evaluation in detail.

2. Experimental procedure

DEVICE FABRICATION

Figure 1(a) shows a schematic diagram of the Al-doped SiC EDLT before and after the application of gate voltage. First, ultrasonic cleaning was performed in acetone for 10 minutes (twice) and

then in ethanol for 10 minutes. After cleaning, the substrate was ashed in an oxygen plasma (O_2 : 100 sccm) with an RF power of 300 W for 3 minutes using a plasma asher. For ion implantation, HMDS was spin-coated at 3000 rpm for 10 seconds, followed by OFPR800 at 6000 rpm for 60 seconds. After baking at 90 °C for 3 minutes, exposure was carried out using DL-1000, and development was performed with NMD-3 and pure water. Next, Al was ion-implanted into the P- area, which serves as the channel, at a density of 5×10^{18} cm^{-3} to a thickness of 300 nm, and in the P^+ area, which is used to form the channel and ohmic contact, at a density of 5×10^{19} cm^{-3} to a thickness of 100 nm. Al density and the thickness were estimated by Monte Carlo simulation using SRIM-2008 software based on SiC density (3.215 g/cm^3), energy and dose density for Al-implantation (20 to 250 keV, 7.0×10^{12} to 7.9×10^{13}/cm^2), and incident angle (tilted 7 degrees in the vertical direction of the plane). For carrier activation, the substrate was annealed at 1700 °C for 30 minutes in an Ar atmosphere. Since 1700 °C is higher than the epitaxial growth temperature of SiC, surface atoms may rearrange or Si may desorb, so the surface was capped by a carbon film before annealing. Then, electrodes were formed on the p^+ area by EB evaporation with Ni : 40 nm, Ti : 50 nm, Al: 90 nm, and Pt : 50 nm, and ohmic contact was established by annealing at 800 °C for 10 minutes in an Ar atmosphere. To increase the change in resistance, the channel was thinned by dry etching using a CHF_3 gas in a CE300I dry etching system. Etching time dependence of *I-V* characteristic of the channel is shown in Figure 1(b). As etching time becomes longer, from 60 to 180 s, the slope of the *I-V* becomes more gentle (higher resistance). The channel resistance under each etching time condition calculated from Fig. 1(b) is plotted with respect to etching time in Figure 1(c). Since the channel resistance is inversely proportional to the channel thickness, longer etching time made channel resistance becomes higher. The final channel thickness, calculated from the resistance value, was 18 nm.

Li_3PO_4 (1000 nm) and Si (20 nm) were deposited by the RF sputtering method at room temperature using Li_3PO_4 and Si targets, respectively, with a supply of pure Ar gas at a fixed flow rate of 10 sccm. Sputtering times were 180 minutes for Li_3PO_4 target and 8 minutes for Si target, respectively. And sputtering power and pressure were 50 W and 0.93 Pa for both Li_3PO_4 and Si targets. We chose the amorphous Li_3PO_4 because it has compatibility with relatively high Li^+ conductivity and stability. That is the reason why the amorphous Li_3PO_4 is widely used as a solid electrolyte for solid-state batteries.[21,22] Si was used for the gate electrode, since it is a promising material for the anodes of solid-state lithium batteries due to its high Li capacitance and low working electric potential.[23,24] A Pt electrode (50 nm) was deposited on the Si by electron beam evaporation. Figure 1(d) shows the comparison of resistance values before and after Li_3PO_4 deposition using sputtering, calculated from the orange line (indicated as 180s Etching) and the red line (indicated as After Sputtering Li_3PO_4) in Fig. 1(b). In cases for sputtering on the surface of hydrogen-terminated diamond surfaces, it causes significant damage of the channel, appearing

as a huge resistance jump in several orders of magnitude, rendering them unsuitable for use. On the other hand, it was confirmed that, in the present case with Al-doped SiC, the resistance change was limited to as low as approximately 20 %. This indicates that the sputtering process causes minimal damage to the Al-doped SiC channel, compared to the case with hydrogen-terminated diamond.

Additionally, we fabricated a two-terminal device for the impedance measurement of Li_3PO_4, as shown in Figure 1(e). A 5 nm Ti and 35 nm Pt bottom electrode were deposited on a SiO_2 substrate using electron beam evaporation, followed by the deposition of a 100 nm Li_3PO_4 layer using RF sputtering. A 50 nm Pt top electrode was then deposited via EB evaporation.

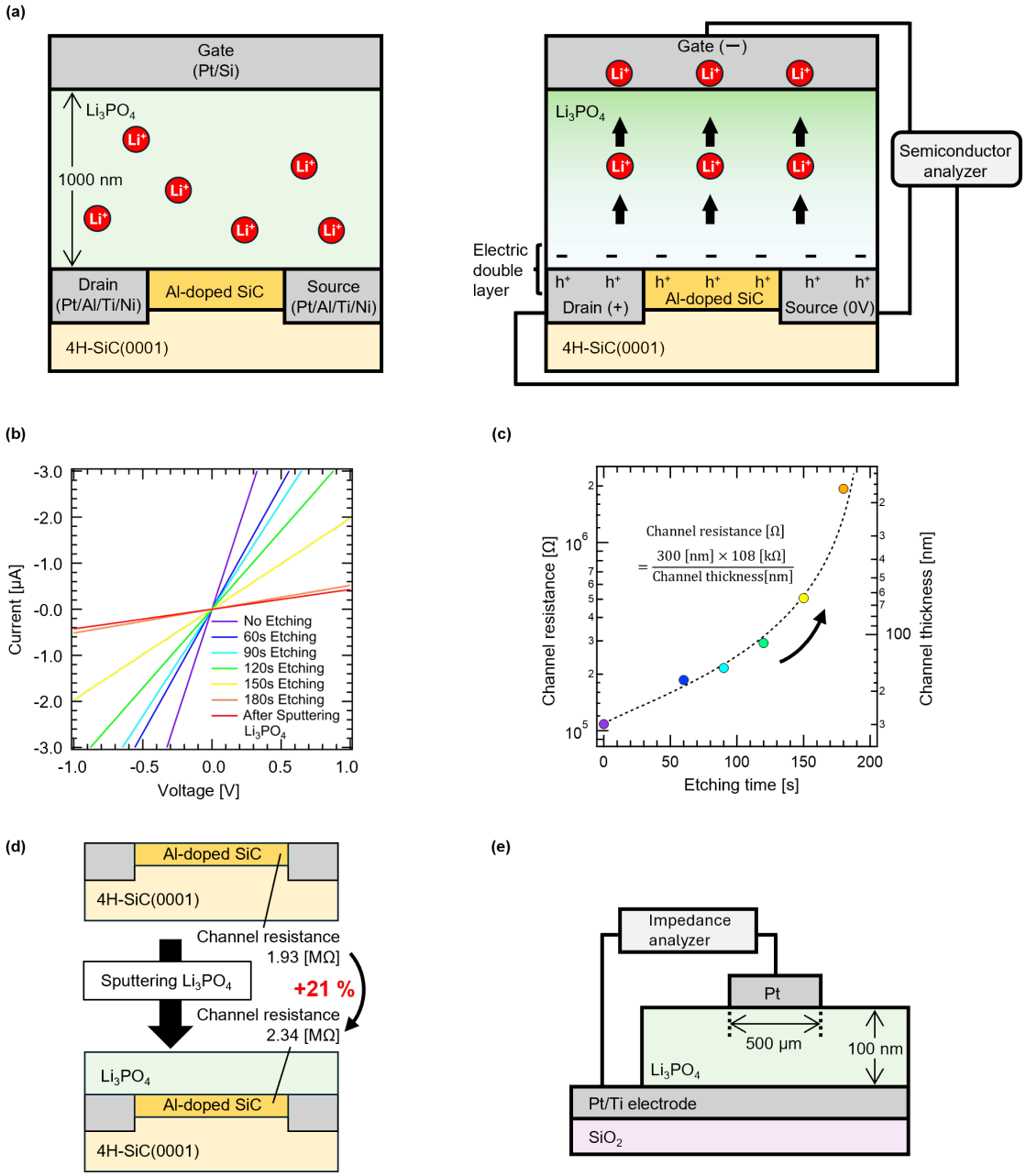

Figure 1. (a) Schematic diagram of Al-doped SiC EDLT and electric double layer effect before and after the application of gate voltage. The minus signs in the figure indicate negative charges. **(b)** Resistance changes by etching process and Li_3PO_4 sputtering. **(c)** The relationship between etching time, channel resistance, and channel thickness in etching. **(d)** Resistance changes by Li_3PO_4 sputtering. **(e)** Schematic diagram of the device used for impedance measurements of Li_3PO_4.

3. Results and Discussion

3.1Electrical Characteristics of Al-doped SiC EDLT

The electrical characteristics of the fabricated device shown in Fig. 1(e) were measured at room temperature in a vacuum chamber. Figure 2(a) shows the Cole-Cole plot, the fitting results, and the equivalent circuit. Here, the resistance of the lead wire, including the contact resistance, is denoted as R_{lead}, bulk resistance as R_{b}, and electrode interface resistance as R_{if}. From the fitting results, the resistances were $R_{\mathrm{lead}} = 125\ \Omega$, $R_{\mathrm{b}} = 13.4\ \mathrm{k}\Omega$, and $R_{\mathrm{if}} = 413.5\ \mathrm{M}\Omega$ respectively. In the present study, the equivalent circuit was applied, although there appears to be a slight deviation between the experimental result and simulation, possibly due to the non-uniformity of Li concentration in the thin-film growth direction, leading to multiple resistance components. The conductivity was calculated by assuming that the resistance of the Li_3PO_4 amorphous thin film is R_{b}, resulting in a value of $3.8 \times 10^{-8}\ \mathrm{S/cm}$. The right plot in Fig. 2(a) confirms that there is no significant electronic conduction, indicating that Li_3PO_4 functions as an ionic conductor.

Next, we used the source measurement unit (SMU) of a semiconductor parameter analyzer (4200A-SCS, Keithley) to analyze the electrical characteristics of the EDLT shown in Fig. 1(a). We confirmed the ohmic contact at various gate voltages (V_G), ranging from -0.5 V to 3V [Figure 2(b)]. The drain current (I_D)-V_G and gate current (I_G)-V_G curves of the Al-doped SiC EDLT are shown in Figure 2(c). In Fig. 2(c), the V_G was swept from 0 V to 3 V, then reversed to -1 V and back to 0 V at the sweep rate of 0.03 V/s. By application of a V_G, this Al-doped SiC EDLT changes the channel resistance by charging (discharging) the EDL at the Al-doped SiC/Li_3PO_4 interface. When a negative V_G is applied, Li^+ ions in Li_3PO_4 being attracted toward the gate electrode from the Al-doped SiC/Li_3PO_4 interface to form the EDL with negatively charged Li vacancy in the Li_3PO_4 and positively charged hole in the Al-doped SiC, resulting in the low channel resistance shown in right panel of Fig. 1(a). Here, as shown in Figure. 2(d), applying a V_G smaller than -1 V causes the I_G to increase rapidly. In this range, the I_G overlaps with the I_D, making it impossible to accurately measure the channel resistance changes from the I_D. On the other hand, the application of a positive V_G causes Li^+ ions to accumulate at the Al-doped SiC/Li_3PO_4 interface, reducing the hole density on the surface of the Al-doped SiC channel, which results in

increased channel resistance. The application of V_G resulted in the maximum resistance variation of 67.4%. Additionally, the direction of the resistance change was consistent with the theoretical operating principle of the device. These findings confirm the successful fabrication of the EDLT device using Al-doped SiC single crystal.

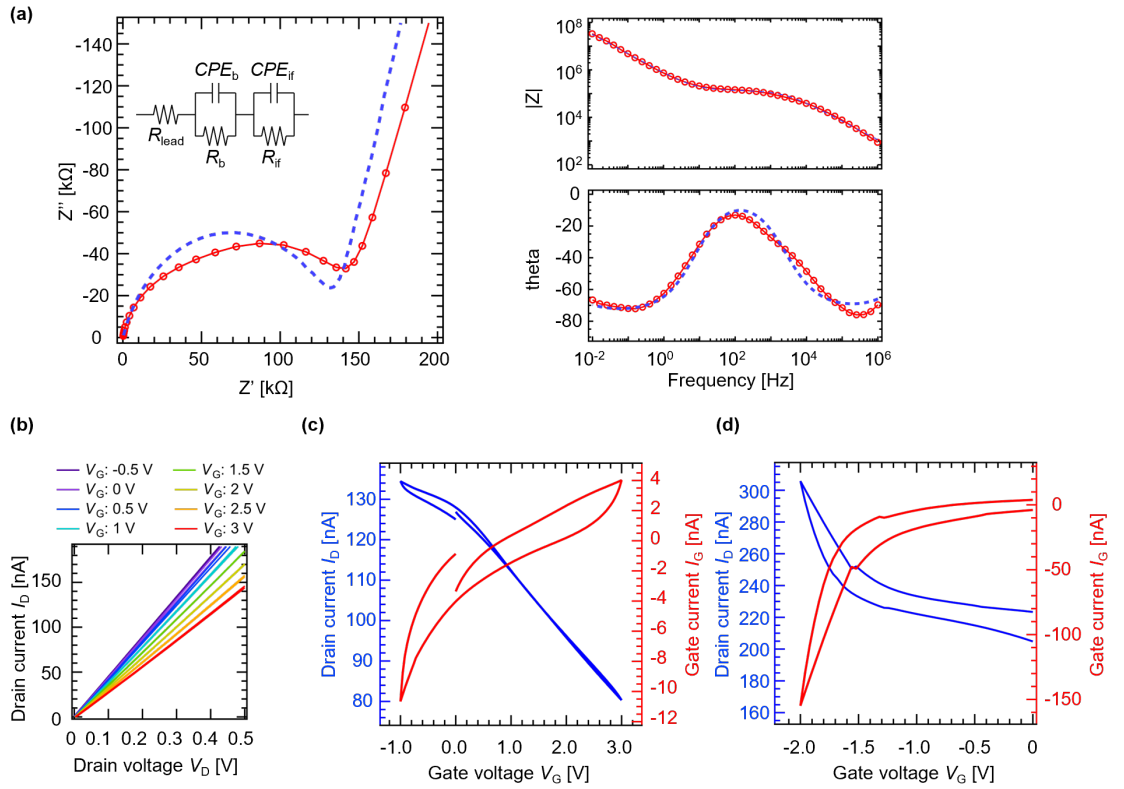

Figure 2. (a) Impedance measurement results of Li_3PO_4 and the equivalent circuit (the blue dashed line represents the fitting results). **(b)** I_D-V_D characteristics. **(c)** The I_D-V_G and I_G-V_G curves of the p-doped SiC EDLT during V_G sweeping (V_G was swept from 0 V to 3 V, then reversed to -1 V and back to 0 V) at the sweep rate of 0.03 V/s. **(d)** The I_D-V_G and I_G-V_G curves of the p-doped SiC EDLT during V_G sweeping (0 V to -2 V, then back to 0 V) at the sweep rate of 0.03 V/s.

3.2 Hall measurement of Al-doped SiC EDLT

To evaluate the EDL at the Al-doped SiC/Li_3PO_4 interface in the EDLT, Hall measurements were performed at 300 K in a He gas. The V_G was adjusted from 0 to 3 V, increasing by 0.2 V each time, and electrical resistance, carrier density, and mobility were measured in a magnetic field for each value. Figure 3(a) presents a schematic diagram of the device used for Hall measurements, an optical microscope image, and the dimensions of the channel. The channel size are 100 μm in length, 300 μm in width, with electrode widths of 50 μm, fabricated via photolithography on a Al-doped SiC substrate (for further details, see device fabrication section).

The upper panel of Figure 3(b) shows changes in the carrier density of the Al-doped SiC EDLT obtained from Hall measurements, with carrier density decreasing by about half as V_G increased from 0 to 3 V increments. When a positive V_G is applied, Li^+ ions in the Li_3PO_4 layer move toward the SiC channel side, reducing holes at the channel surface. This process suppresses the EDL effect at the channel/Li_3PO_4 interface, leading to an increase in channel resistance, as shown in the lower panel of Fig 3(b). When the V_G was varied within the range of 0 to 3 V, the channel resistance exhibited a 59.4% change in the V_G sweep shown in Fig 2(c), while the carrier density measured in the Hall measurement in the upper panel of Fig. 3(b) changed by 60.8%. Thus, there was no significant difference in the magnitude of change. However, the difference in the shape of the variations can be attributed to the measurement methods. In the V_G sweep, the V_G was swept at 0.03 V/s, on the other hand, in the Hall measurements, the V_G was fixed at a given V_G while the magnetic field was varied, resulting in each V_G being applied continuously for 50 minutes. These differences in measurement methods are the reason for the difference shapes of the two graphs. As shown in the middle panel of Fig. 3(b), the Hall mobility decreases from 80 $cm^2/V{\cdot}s$ as the gate voltage increases and is lower than the reported literature value of 80–110 $cm^2/V{\cdot}s$, indicated by the blue band.[25,26] However, the activation energy of the Al acceptor in SiC is about 150-190 meV, significantly higher than the room temperature activation energy of 25 meV. As a result, the carrier density at room temperature is lower than the doped carrier density.

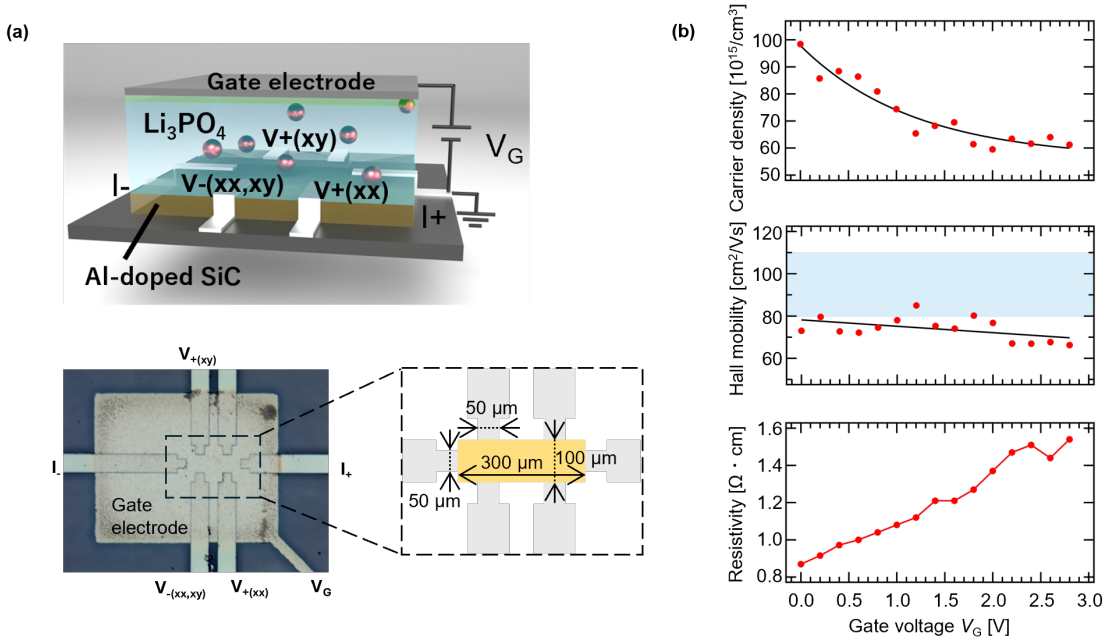

Figure 3. (a) Schematic diagram of the Al-doped SiC EDLT along with an optical microscope image of the Hall-bar electrodes and channel dimensions. **(b)** Carrier density (upper panel), Hall mobility (middle panel) and electrical resistivity (lower panel) for Al-doped SiC EDLT determined by Hall measurement.

The differential capacitance, $C_{EDL}={}^{d\,Q}/_{d\,V_G}$, was calculated based on the changes in carrier density obtained from Hall measurements shown in the upper panel of Figure 4 (a). Q is the electrical charge density. As shown in Fig. 4(a), the differential capacitance was determined to be several nF/cm², which is significantly lower than the expected EDL capacitance, which is on the order of several μF/cm².[16,27-30] Here, as depicted in Figure 4(b), two possible scenarios can be considered to interpret the observed low capacitance. The first scenario, as depicted on the left side of Fig. 4(b), involves Li^+ ions in Li_3PO_4 being attracted toward the gate electrode under the applied V_G. This leads to the formation of an EDL at the Li_3PO_4/Al-doped SiC interface and an accumulation layer on the SiC surface. In this case, only the EDL capacitance (C_{EDL}) is included, and C_{EDL}, which is on the order of several μF/cm², can be directly measured. The second scenario involves Li^+ ions in Li_3PO_4 accumulating at the Li_3PO_4/Al-doped SiC channel interface under the applied V_G, resulting in the formation of a depletion layer on the SiC surface. In this case, the depletion layer capacitance (C_{DL}) appears in addition to the EDL capacitance (C_{EDL}), causing the combined capacitance to be significantly lower than that of the EDL alone. Based on these two scenarios, we concluded that the latter scenario occurs in the present measurements. Furthermore, as shown in the graph in Figure 4(c), which illustrates the relationship between the calculated space charge layer thickness on the surface of the SiC channel and dopant density in the SiC channel.[31] The thickness of the space charge layer formed on the SiC surface shown in Fig. 4(c) was calculated based on the equation derived from Poison's equation.[31]

$$W = \sqrt{\frac{2\varepsilon_s V_{bp}}{qN}} \quad (1)$$

where W, N, q, ε_s, and V_{bp} are the thickness of the space charge layer, dopant density, elementary charge, the permittivity of SiC (9.7), and built-in potential (assumed to be 1 V). The carrier density obtained from the Hall measurements suggest that the depletion layer thickness is approximately 100 nm (shown by a red band in Fig. 4(c)). Considering the channel thickness of 18 nm, this aligns with the latter scenario. To achieve the former condition (without depletion layer) with the current device, a large negative gate voltage would need to be applied. Gate voltage application modulates not only the thickness of the space charge layer, but also energy difference between Fermi level and valence band maximum, leading to carrier density variation and the resultant resistivity variation. However, the application of the required negative V_G resulted in an excessively large leakage current that prevented accurate Hall measurements.

The expected energy diagram at the Li_3PO_4/Al-doped SiC channel interface is shown in Figure 4(d). The upper panel of Fig. 4(d) illustrates the relationship between the reported electron affinity, work function and ionization potential of the electrolyte and the Al-doped SiC EDLT channel before and after junction formation.[32-34] Upon junction formation, electrons are transferred from Li_3PO_4 to the SiC channel, bending the energy band downward and forming a depletion layer on the Al-doped SiC channel surface. As illustrated, the built-in potential (V_{bp}) generated by the electric field in the depletion layer is too large to apply a V_G sufficient to form an accumulation layer in this device. To accurately measure the EDL capacitance, as shown in the lower panel of Fig. 4(d), it is necessary to form an accumulation layer on the Al-doped SiC channel surface. This requires constructing the channel using semiconductor material with a Fermi level lower than that of the electrolyte (i.e., lower work function than Li_3PO_4). P-type semiconductor materials with lower work function than the current device would allow the formation of an accumulation layer in the semiconductor channel, leading to achieving the optimal condition for evaluation of C_{EDL}. Alternatively, n-type semiconductor materials with higher work functions can also satisfy the condition for generating an accumulation layer on the channel surface.

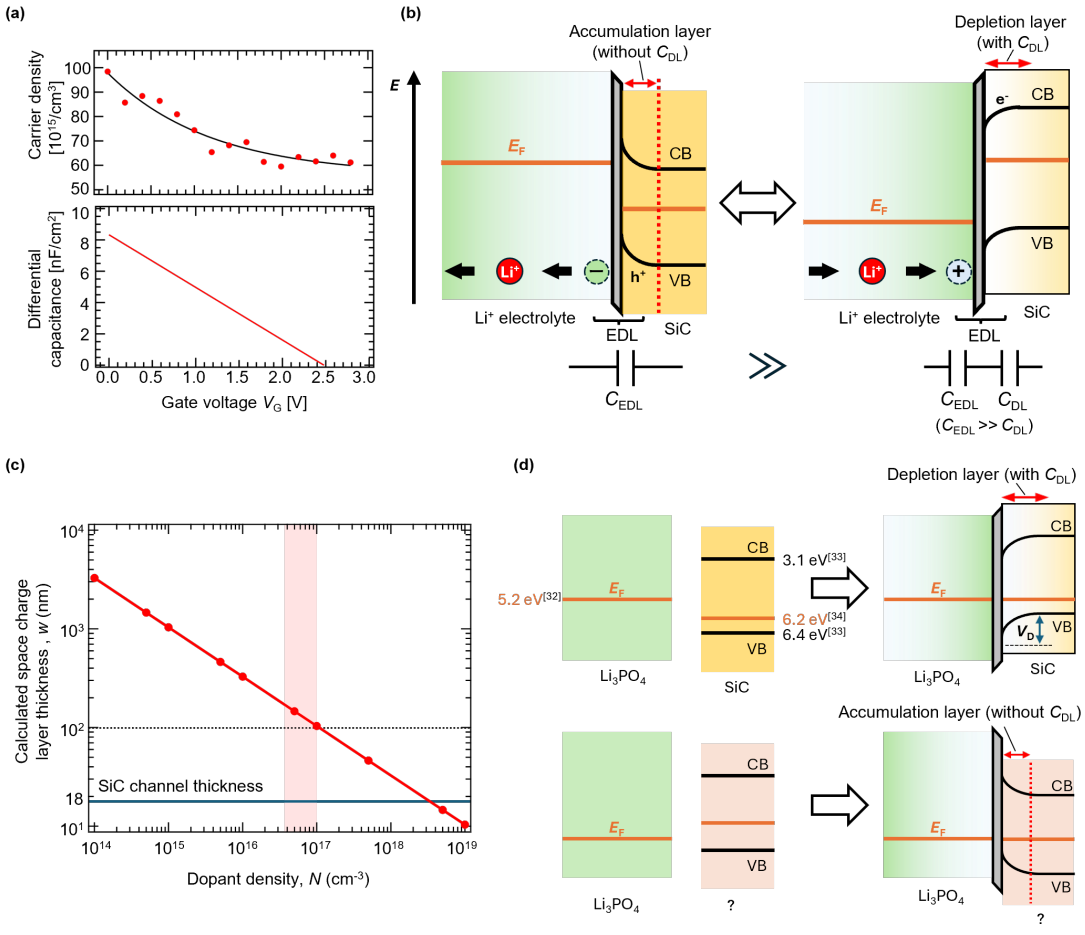

Figure 4. (a) The differential capacitance calculated from the results of the Hall measurements. **(b)** The energy band diagrams and the relationship between capacitance in the two expected states of the Al-doped SiC EDLT. **(c)** The relationship between impurity concentration and the space charge layer. The red vertical band represents the range of impurity concentration in the Al-doped SiC EDLT, while the blue horizontal line indicates the channel thickness of the Al-doped SiC EDLT. **(d)** (Upper) Energy band diagrams of Li_3PO_4 and the Al-doped SiC EDLT channel before and after junction formation. (Lower) Ideal energy band diagrams of a solid electrolyte and semiconductor material before and after junction formation in a system optimized for measuring electric double layer capacitance.

4. Conclusion

In this study, an electrolyte-gated EDLT was fabricated using Li_3PO_4 as the solid electrolyte and Al-doped SiC as the channel material, which was selected to achieve high tolerance to reduce the channel damage, and the electrical characteristics and behavior of the EDL were investigated. Device operation was confirmed by observing resistance changes in response to applied V_G, which aligned with the theoretical operating principle of EDLT. This demonstrated the stable operation of Al-doped SiC in the fabricated device. Hall measurements were employed to evaluate carrier density changes and to calculate the differential capacitance, probing the behavior of the EDL at the solid electrolyte/semiconductor interface. The differential capacitance results revealed that, in the current device configuration, the measured capacitance consists of contributions from both the EDL capacitance and the depletion layer capacitance formed on the SiC surface. This resulted in a reduction of the combined capacitance compared to the theoretical value of EDL capacitance alone. These findings indicate that depletion layer formation is dominant during the measurements. This depletion layer on the SiC surface is likely caused by the redistribution of Li^+ ions in the Li_3PO_4 near the interface, which alters the internal potential and reduces carrier density at the channel surface. For direct and effective measurement of the EDL effect, we found that the Fermi level of the channel material must be lower than that of the electrolyte, in the case of the p-type channel. This can be achieved by choosing the appropriate semiconductor materials for the channel, allowing the accurate evaluation of the EDL capacitance. In addition to the semiconducting characteristics of the channel, the electrochemical window of the electrolyte is also needed to be considered. The findings of this study provide significant insights into the characterization of electrolyte interface properties and the design of next-generation functional devices utilizing electrolytes, including neuromorphic computing devices.[35-40] In this research, SiC was selected as a material capable of withstanding the high damage and thermal stresses associated with device fabrication processes that were difficult to overcome using hydrogen-terminated diamond. This study pioneers the exploration of EDL effects with electrolytes, deposition methods, and processes

that were previously challenging. We believe that these advancements can lead to the development of high-performance all-solid-state batteries and neuromorphic devices. Furthermore, the proposed strategies for material selection and device architecture promise to enhance the performance and reliability of such technologies, laying a solid foundation for future research and development.[41,42)]

Acknowledgement

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