Self-aligned gate electrode for hydrogen-terminated diamond field-effect transistors with a hexagonal boron nitride gate insulator

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Diamond electronic devices have garnered significant interest owing to their excellent semiconducting properties. We recently demonstrated that excluding surface-transfer doping results in enhanced carrier mobility and a normally off behavior in diamond field-effect transistors (FETs) with a hexagonal boron nitride (h-BN) gate insulator. In our previous study, the gate electrode was overlapped onto the source/drain electrodes to prevent the increase in access resistance caused by the exclusion of the surface-transfer doping. However, it is known that gate overlap increases parasitic capacitance and gate leak current. In this study, we developed a technique for self-aligning the gate electrode with the edge of h-BN using oblique-angle deposition. The diamond FET with self-aligned gate electrode exhibits optimal FET characteristics, including high mobility of $\approx$400 $cm^2V^{-1}s^{-1}$, low sheet resistance of 2.4 kΩ, and output characteristics demonstrating pinch-off behavior. Furthermore, the capacitance-voltage characteristics clearly indicate distinct ON and OFF states, validating the efficacy of this technique. This method enables the fabrication of diamond/h-BN FETs with no gate overlap and without increasing the access resistance, making it promising approach for developing high-speed, low-loss diamond FETs with a wide application scope.

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Diamond, a wide-gap semiconductor with excellent properties such as a high mobility, high breakdown electric field, and high thermal conductivity, is a promising electronic material. Recently, research on diamond electric devices such as field-effect transistors (FETs) has gained momentum. Diamond FETs are primarily fabricated on hydrogen-terminated diamond surfaces, because the hydrogen-termination-mediated upward shift in the valence band (VB) of diamond allows the incorporation of hole carriers[1]. Owing to this upward shifted VB, atmospheric adsorbates[2], acidic gases[3] (such as NO_2), and solid insulators[4] with a high electron affinity (such as V_2O_5) can be used as surface acceptors for hydrogen-terminated diamonds. Electrons in the VB of a hydrogen-terminated diamond migrate to these surface acceptors, resulting in the formation of a two-dimensional hole gas, and this process is called surface-transfer doping. Hydrogen-terminated diamond FETs fabricated by surface-transfer doping exhibit high-temperature operations[5] at 400°C , high breakdown source–drain voltage[6] exceeding 2000 V, high drain current density[7] of 1.3 Amm^{-1}, high-frequency operation[8] with high cut-off frequency of 70 GHz, and operation under radiation[9]. However, ionized surface acceptors limit the mobility of diamond FETs[10].

In our previous studies, we fabricated hydrogen-terminated diamond FETs with a reduced surface acceptor density to achieve mobility enhancement. First, we fabricated the FETs using single-crystalline hexagonal boron nitride (h-BN) as the gate insulator to reduce the density of insulator defects, which could act as acceptor states. The FET showed a relatively high channel mobility of approximately 300 $cm^2V^{-1}s^{-1}$.[11,12] Next, FETs were fabricated using an air-free process, wherein the hydrogen-terminated surface was not exposed to air, to reduce the density of surface acceptors originating from air adsorbates, and a high channel mobility of 680 $cm^2V^{-1}s^{-1}$ was observed, which resulted in the lowest minimum channel sheet resistance of 1.4 kΩ reported to date for hydrogen-terminated diamond FETs. Our results show that surface-transfer doping is not necessary for the operation of hydrogen-terminated diamond FETs and that reducing the density of surface acceptors can improve the performance of diamond FETs.[13]

In diamond FETs with a h-BN gate insulator[13], the gate electrode overlaps with source/drain electrodes (Fig. 1a) to eliminate the access region. We fabricated the FETs on IIa-type hydrogen-terminated diamonds with a low surface-acceptor density. If the gate electrode does not overlap with the source/drain electrodes, as shown in Fig. 1b, then the on-resistance of the FET is high owing to the high access resistance. To prevent this

phenomenon, we used FET structures with gate overlap. However, such structures exhibit certain shortcomings: 1) A large parasitic capacitance that renders the FET unsuitable for high-speed operations; 2) a large gate leak current that limits carrier density; 3) the h-BN layer may detach from the diamond surface near the source and drain electrodes, thereby reducing the gate-bias effect near the electrodes; and 4) h-BN lattice distortions that occur near the electrodes reduce the breakdown gate voltage.

Figure 1c shows the desirable FET structures for mitigating these limitations: 1) The gate electrode should extend to the edge of h-BN, and 2) the surface of the access region should be hydrogen-terminated to allow surface-transfer doping. However, fabricating such a structure using standard lithography techniques is challenging because of the inevitable electrode misalignment caused by the lithographic alignment accuracy. Although h-BN may be dry-etched using the gate electrode as a mask to avoid misalignment of h-BN and the gate electrode, dry etching may damage the edges of h-BN and the hydrogen-terminated surface of the access region, potentially causing a high gate leakage current and access resistance.

In this study, we developed a method to induce self-alignment of the gate electrode with the source/drain electrodes for fabricating a desirable device. A hydrogen-terminated diamond was laminated with an h-BN thin film, onto which Pd was deposited at an angle of 45° (Fig. 2a). Here, the tilt angle is defined as an angle between the direction of evaporated Pd and the normal direction to the diamond substrate. Because h-BN functioned as a mask during the deposition, the deposited Pd film was disconnected near the edge of h-BN (Fig. 2a). The Pd films deposited on h-BN and the diamond were used as the gate and source/drain electrodes, respectively. We leveraged the surface conductivity induced by the surface-transfer doping in the access region, and Pd was used to form good ohmic contacts with the hydrogen-terminated diamond[14–16].

Before fabricating the FET structure, we confirmed the occurrence of disconnection of the Pd film near the h-BN edges owing to the oblique-angle deposition. We used an oxygen-terminated IIa diamond substrate that did not exhibit electrical conduction. After transferring a 35-nm-thick h-BN layer, a 20-nm-thick Pd layer was deposited at an angle of 45°. Figure 2b shows the scanning electron microscopy (SEM) image of the deposited Pd film; h-BN is shown in the left half of the SEM image, and a 67-nm gap is visible between the deposited Pd films. This gap is wider than that expected from the deposited thicknesses of the h-BN and Pd films. Although the underlying mechanism for this wide gap remains

obscure, it may be attributed to the ability of the Pd film deposited on h-BN to also function as a mask. The measured electrical resistance between the Pd film on h-BN (left side of the SEM image) and that on the diamond substrate (right side of the SEM image) exceeded 1 GΩ, confirming the disconnected state of the Pd film.

Hydrogen-terminated diamond FETs with self-aligned gate electrodes were fabricated using an oblique-angle deposition technique. The fabrication process is as follows: We used IIa-type (111) single-crystalline diamond substrate (purchased from Technological Institute for Superhard and Novel Carbon Materials (TISNCM)), same as our previous studies[11–13]. First, the diamond substrate was cleaned using an organic solvent (isopropyl alcohol and acetone) and a hot mixed acid (nitric acid:sulfuric acid = 1:3, 200°C). The diamond surface was terminated with hydrogen via hydrogen annealing and plasma treatment in a chemical vapor deposition (CVD) chamber. Hydrogen annealing were performed at an H_2 gas flow rate of 500 sccm, a pressure of 80 Torr, and a temperature of 650°C for 35 min. The hydrogen plasma treatment was conducted at a microwave power of 300 W, an H_2 gas flow rate of 500 sccm, a pressure of 30 Torr, and a stage temperature of 600°C for 10 min. The hydrogen-terminated diamond substrate was then transferred from the CVD chamber to an Ar-gas-filled glove box under vacuum using a vacuum suitcase to avoid air exposure. Subsequently, the hydrogen-terminated diamond surface was laminated with a single-crystalline h-BN thin film inside the glove box (Fig. 3a). The h-BN film fabricated in this study had a thickness of 16 nm, with 32-nm-thick folded region near the edge, and functioned as a gate insulator. To transfer the h-BN film, first, single-crystalline h-BN was cleaved using a Scotch tape and transferred onto a Si/SiO_2 substrate; then, the cleaved h-BN was picked-up from the substrate using a viscoelastic polymer stamp and transferred onto a hydrogen-terminated diamond surface using a process similar to that used in previous studies[17,18]. Unlike the gel-sheet-based dry transfer method, which was used in our previous study[13], the pick-up method[19] is useful for avoiding the formation of hydrocarbon-containing contamination bubbles at the interface. Huang et al. recently fabricated diamond/h-BN heterostructures using this pick-up method[20]. In our previous study, diamond was laminated with h-BN at room temperature[13], whereas in this study, this process was conducted at 110°C. We heated the diamond substrate during the lamination process to desorb impurities and thus reduce the density of impurities at the diamond/h-BN interface. However, heating the diamond may have heated the polymer holding h-BN, and impurities desorbed from the

heated polymer may have contaminated the diamond/h-BN interface. After the transfer of h-BN, the sample was annealed at 200°C for 3 h in a glove box. The source/drain and self-aligned gate electrodes were simultaneously fabricated by depositing a 20-nm-thick Pd layer at an angle of 45° with electron-beam lithography and lift-off process. (Fig. 3b) Then, h-BN was etched into a Hall bar shape. h-BN etching was performed using the capacitively coupled plasma reactive ion etching method at a radiofrequency power of 35 W, a pressure of 10 Pa, and N_2, CHF_3, and O_2 gas flow rates of 96, 2, and 2 sccm, respectively. The diamond surface underwent oxygen termination, except the region under h-BN—the access region—and the electrodes, for device isolation (Fig. 3c). Subsequently, 30-nm-thick Al_2O_3 was deposited by atomic layer deposition at 120°C to passivate the device and was wet-etched using diluted tetramethylammonium hydroxide to form through-holes for electrical measurements. Finally, Ti(10 nm)/Au(100 nm) was deposited as a gate contact. (Fig. 3d) Through these processes, a hydrogen-terminated diamond FET with a self-aligned gate electrode was fabricated, as shown in Fig. 3e. We used a gated Hall bar structure to evaluate the mobility and carrier density accurately through Hall effect measurements.

Figure 4a shows the output characteristics of an FET with a self-aligned gate electrode. The FET exhibits p-type operation; the drain current density increases under negative gate voltages. Although the device has a long gate length of 25 μm, a relatively high maximum drain current density of $\approx$30 mAmm^{-1} is obtained. Figure 4b shows the transfer characteristics. The sheet conductance was measured using the four-probe method, in which current flows between the source and drain electrodes (electrodes Nos. 2 and 5 in Fig. 3e), and the voltage drop between the voltage probes (electrodes Nos. 3 and 4 in Fig. 3e) was measured. The measurement was carried out with a drain current of less than 10 nA (by applying a voltage of 100 mV through a 10 MΩ series resistor). The maximum sheet conductance was 4.1×10^{-4} S. This corresponds to the sheet resistance of 2.4 kΩ. This minimum sheet resistance is lower than those of most diamond FETs reported to date.

The resistances measured using the four- and two-probe configurations were used to evaluate the contact resistances (R_{cS} and R_{cD}) at the source and drain electrodes normalized by the channel width (W_{G}):

$$(R_{\mathrm{cS}} + R_{\mathrm{cD}})W_{\mathrm{G}} = [R_{2\mathrm{p}} - (L_{\mathrm{G}}/L_{\mathrm{p}})R_{4\mathrm{p}}]W_{\mathrm{G}}; \quad (1)$$

here, $R_{4\mathrm{p}}$ and $R_{2\mathrm{p}}$ are the resistances measured using the four- and two-probe configurations,

respectively; L_G is the channel length; and L_p is the distance between the voltage probes. The normalized contact resistance ($(R_{cS} + R_{cD})W_G$) of the FET is evaluated to be 50 Ωmm with an applied gate voltage of -6 V. This contact resistance includes the access resistance. This value was larger than 5∼15 Ωmm of the contact resistance of the TiC electrodes formed by Ti/Pt deposition and subsequent annealing in our previous FETs[13], and 1.74 Ωmm for Au electrode[21]. The larger contact resistance of Pd was also observed in previous reports[15,16] and may be caused by physiosorbed molecules[16] which reduce the work function of the deposited Pd film. Depositing Pd in ultra-high vacuum could suppress the reduction of work function and decrease the contact resistance. The contact resistance increases at lower temperatures, but is still 440 Ωmm at 4.4 K with applied gate voltage of -6 V. This indicates that the Pd electrodes functioned even at low temperatures. In this study, carriers in the access region were introduced using air adsorbates. Access resistance may be reduced by increasing the carrier density in the access region through NO_2 gas exposure or V_2O_5 deposition[22].

Figure 4c shows the capacitance–voltage (C–V) characteristics measured with an AC amplitude of 50 mV across various gate voltages and frequencies. During the C-V measurements, the five electrodes of the Hall bar were shorted to avoid the estimate of the insulator capacitance being affected by parasitic capacitances, as discussed below. Initially, the capacitance between the five electrodes and gate was measured at frequencies ranging from 1 kHz to 1 MHz with V_{GS} set to 0 V. Subsequently, similar measurements were performed with an applied gate voltage ranging from -6 V to 6 V in steps of 0.5 to 1 V. The capacitance was normalized to the area of the gate electrode (117 μm^2). In the ON state regime, the measured capacitance at V_{GS} = -6 V is 0.24 μFcm^{-2} and remains nearly constant upto V_{GS} = 0 V. However, during the transition from the ON to OFF state, the capacitance decreases and becomes ≈0.07 μFcm^{-2} at V_{GS} = 2 V, which stays nearly unchanged thereafter. It may be mentioned here that the OFF-state capacitance is the parasitic capacitance between the five electrodes and gate, while the ON-state capacitance is the sum of the parasitic and insulator (h-BN) capacitances. Therefore, the capacitance of h-BN can be calculated by subtracting the OFF-state capacitance from the ON-state capacitance, which is found to be 0.17 μFcm^{-2}. Since the thickness of h-BN is 16 nm, the dielectric constant of h-BN is calculated to be $3.2\epsilon_0$ (ϵ_0 is the permittivity in vacuum), which is in good agreement with those reported in previous studies[23]. Here, the capacitance in the two-folded regions (13 μm^2) is considered to be half of that in the non-folded region. It is noteworthy that

obtaining an accurate estimate of h-BN capacitance is challenging if the five electrodes are not shorted and the capacitance is measured between gate and only one of the Hall bar electrodes. This difficulty arises because, in the OFF-state, the measured capacitance primarily consists of the parasitic capacitance between gate and the Hall-bar electrode, while in the ON-state, capacitance includes the parasitic capacitances between gate and the other Hall-bar electrodes[24].

The carrier density of the FET was evaluated through Hall-effect measurements with magnetic field sweeping between -1 and 1 T. Here, current flows between electrodes Nos. 2 and 5 in Fig. 3e, and the Hall voltage between electrodes Nos. 1 and 3 and the longitudinal voltage between electrodes Nos. 3 and 4 are measured. Figure 4d shows the gate voltage dependence of the carrier density obtained from the Hall effect measurements. The carrier density increased linearly with the gate voltage, and the maximum sheet carrier density reached 6.5×10^{12} cm^{-2}. Linear fitting of this curve reveals the threshold voltage as ≈0.3 V. Unlike our previous study[13], the FET operated in the normally on mode. This normally on operation can be ascribed to two primary mechanisms. The first reason is that the material of gate electrode differs from our previous studies[13]. Pd was used for gate electrode in this study, while graphite was used for gate electrode in our previous study[13]. The work function of Pd (5.1 eV)[25] is higher than that of graphite (4.7 eV)[26], which induces a positive shift in the threshold voltage. Second, the density of the charged impurities at the diamond/h-BN interface was higher than that observed in our previous study. According to the equation[27]

$$V_{\rm th} = -\frac{e(n_{\rm depl} - n_{\rm ic})t_{\rm hBN}}{\epsilon_{\rm hBN}} + \psi_{\rm s}(p_{\rm 2D} \to 0) + \phi_{\rm ms}, \tag{2}$$

the measured threshold voltage ($V_{\rm th}$) corresponds to a net sheet density of 1×10^{12} cm^{-2} for the negative charges at the interface. Here, $n_{\rm depl}$ is the sheet density of the fixed charge in the depletion layer; $n_{\rm ic}$ is the net sheet density of the interface negative charge; $\psi_{\rm s}(p_{\rm 2D} \to 0)$ (<0) is the surface potential at the limit of the low-hole sheet density ($p_{\rm 2D}$); $e\phi_{\rm ms} = e\phi_{\rm m} - e\phi_{\rm s}$(≈ 4.8 eV) is the difference between the work function ($e\phi_{\rm m} \approx 5.1$ eV)[25] of the Pd gate and that ($e\phi_{\rm s} \approx 0.3$ eV)[13,28] of the hydrogen-terminated surface; and $n_{\rm depl}$ and $\psi_{\rm s}$ are calculated using the Schrödinger and Poisson equations for a given $p_{\rm 2D}$ with $N_{\rm D}$ (nitrogen) = 500 ppb and $N_{\rm A}$ (boron) = 7 ppb. The negative charge density of 1×10^{12} cm^{-2} is higher than that in our previous study[13] (4×10^{11} cm^{-2}). We believe that the charged impurities originate from those desorbed from the polymer holding h-BN; as mentioned before, this polymer is

heated during the transfer of h-BN. Notably, the normally on mode cannot be attributed to the unintentional contamination of boron in diamond. In the transfer characteristics shown in Fig. 4b, the conductance decreases to almost zero at a positive gate voltage, whereas boron-contamination-induced conductance should have a finite value.

Figure 4e shows the gate voltage dependence of the mobility. Evidently, the Hall mobility, effective mobility($\mu_{\rm eff} = \frac{t_{\rm hBN}}{\epsilon_{\rm hBN}} \frac{\sigma}{|V_{\rm GS} - V_{\rm th}|}$), and field-effect mobility($\mu_{\rm FE} = \frac{t_{\rm hBN}}{\epsilon_{\rm hBN}} \left| \frac{\partial \sigma}{\partial V_{\rm GS}} \right|$) are almost consistent; here $t_{\rm hBN}$ and $\epsilon_{\rm hBN}$ are the thickness and dielectric constant of h-BN, respectively; $\epsilon_{\rm hBN}$ is $3.2\epsilon_0$ as mentioned before; $V_{\rm GS}$ and $V_{\rm th}$ denote the gate and threshold voltages, respectively; and σ is the sheet conductance (Fig. 4b). The maximum mobility ($\approx$400 $\rm cm^2V^{-1}s^{-1}$) is relatively high (Fig. 4e). However, this value was slightly lower than that in our previous study[13] possibly owing to the slightly high density of charged impurities at the diamond/h-BN interface. We believe that this discrepancy can be mitigated by further improving the h-BN transfer technique; for instance, the impurities in the polymer holding h-BN may be desorbed by annealing the polymer in a glove box before use.

In this study, we developed a method for fabricating gate electrodes that self-align with the source/drain electrodes by depositing Pd at an angle of 45°. During the oblique-angle deposition, the h-BN gate insulator acted as a mask, allowing simultaneous fabrication of source/drain electrodes and a self-aligned gate electrode. We fabricated a diamond FET with a self-aligned gate electrode and obtained good FET characteristics. We envision that increase in the h-BN thickness and deposition from a larger angle can widen the gap between the gate and source/drain electrode, thereby allowing the application of high source-drain voltage and reduction in parasitic capacitance. Although the same material was used for the source/drain and gate electrodes in this study, the materials of the source/drain and gate electrodes could be modified by depositing two different metals from different angles. For example, if a low-work-function metal (such as Al) is deposited at an angle of 70°, followed by a high-work-function metal (e.g., Pd, Au) deposited at an angle of 45°, then we can fabricate an FET with both good ohmic contacts and a normally off operation. We believe that the method developed in this study for fabricating self-aligned gate electrodes can contribute to the construction of diamond FETs incorporated with h-BN gate insulators that can operate at remarkably high speeds.

Data availability

The data supporting the findings of this study are available from the corresponding author upon reasonable request.

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Acknowledgments

We thank H. Osato, E. Watanabe, D. Tsuya, N. Ikeda, and A. Ohi for technical support. We thank T. Ando, S. Koizumi, and T. Teraji for their assistance with this study.

This study was financially supported by the NEDO Uncharted Territory Challenge 2050 (Project No. JPNP14004), JSPS KAKENHI (Grant No. JP22H01962), and Advanced Research Infrastructure for Materials and Nanotechnology in Japan (ARIM) (Proposal No. JPMXP1223NM5196).

Competing Interests

The authors declare that they have no competing financial interests.

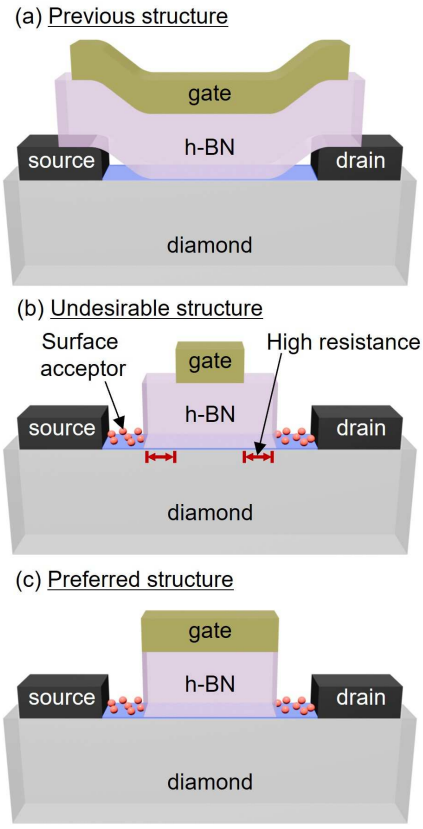

FIG. 1. Schematic of diamond FETs with h-BN gate insulators. (a) Structure fabricated in our previous studies, (b) an undesirable structure, and (c) a preferred structure.

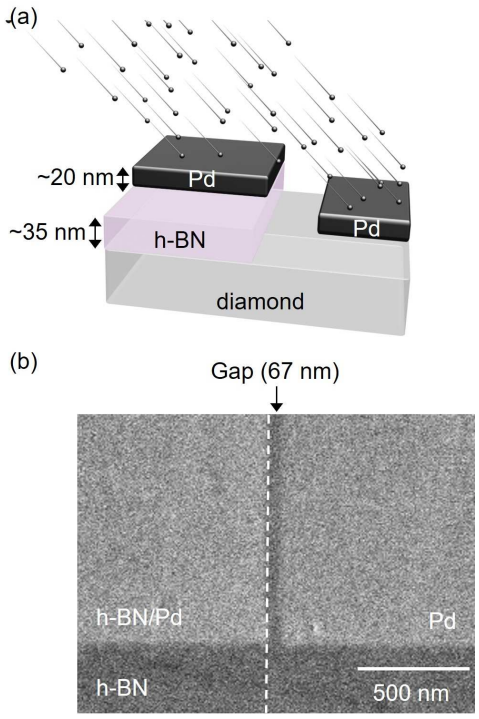

FIG. 2. (a) Schematic of the oblique-angle deposition of Pd. The resist is not shown here for clarity. (b) SEM image of the Pd film deposited at an angle of 45° on diamond/h-BN. Although h-BN is not visible in the SEM image, it is present in the left of the vertical dashed line. The thicknesses of the h-BN and Pd films are 35 and 20 nm, respectively. A charge dissipation agent (Espacer 300Z) was coated to prevent charge accumulation during the SEM observation.

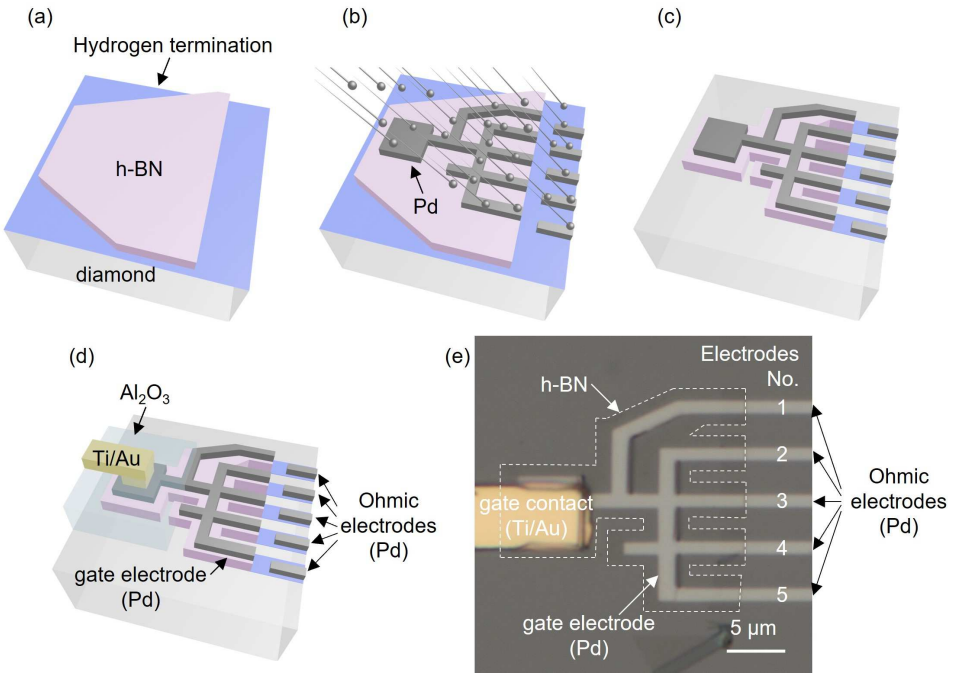

FIG. 3. (a–d) Schematic of the FET fabrication process. (a) h-BN is transferred to hydrogen-terminated diamond. (b) Pd is deposited at an angle of 45°. The resist with the electrode patterns is not shown here for clarity. (c) h-BN is etched into a Hall-bar shape. (d) Al_2O_3 is deposited, and holes are formed via wet etching of Al_2O_3. Although Al_2O_3 is deposited on the entire surface in the actual device, only a part of the deposited Al_2O_3 is shown here . Ti/Au is deposited as a lead. (e) Optical microscopic image of the diamond FET fabricated in this study.

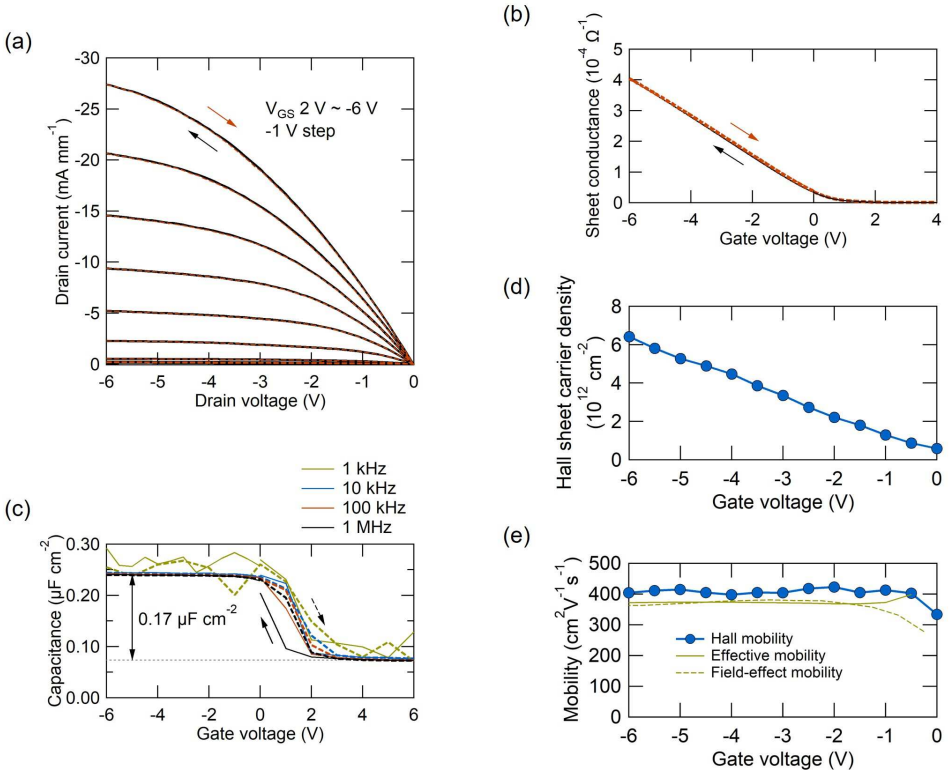

FIG. 4. Electrical characteristics of the fabricated diamond FET with a self-aligned gate electrode. (a) Output characteristics, (b) transfer characteristics, and (c) C–V curve. Gate voltage dependence of the (d) carrier density and (e) mobility. The measurements were performed at 300 K (a, b, d, and e) or at room temperature (c).