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Full Length Article

Patternable laser-oxidized Ta_2O_5 dielectric and TaS_2 contact for optimizing subthreshold swing of MoS_2 field-effect transistors

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ABSTRACT

Recent progress has achieved a high on-current density and a low contact resistivity for *n*-type field-effect transistors using two-dimensional (2D) semiconductors such as MoS_2 and WSe_2. However, other issues with device parameters remain unresolved, such as the use of complementary transistors with a single 2D semiconductor, environmental packaging, and dielectric layers. Integrating an optimal dielectric and ideal interfacial contact for mass production will play a crucial role in future electronics designs. Here, we demonstrate patternable laser oxidation to convert TaS_2 into Ta_2O_5 as an ultra-flat dielectric layer, having been evidenced by energy-dispersive X-ray spectroscopy, nano-X-ray absorption near-edge structure, and atomic force microscopy. With this patternable conversion, we also demonstrate the implementation of TaS_2 as contact electrodes on the MoS_2 channel material. The Ta_2O_5 layer reveals a dielectric constant of ~15.98 and a breakdown field of ~5.5 MV/cm. A high on-current density of ~34.7 μA/μm is achievable in Bi-contacted devices at a channel length of 1.0 μm. Moreover, the TaS_2-contacted MoS_2 transistors on Ta_2O_5 present an extremely low subthreshold swing of ~59.8 mV/dec and a minimal hysteresis of ~0.15 V. This indicates the superior feature of the Ta_2O_5 dielectric through patternable laser oxidation while keeping an ultra-flat interfacial surface.

1. Introduction

Since the successful demonstration of single-layer MoS_2 transistors [1], layered structures of transitional metal dichalcogenides (TMDs) such as MoS_2, WS_2, and WSe_2 have been implemented to build high-performance electronics [2–5]. The few-layer TMDs were alternatively applied to gas sensors [6], biosensors [7], optical sensors [8], and optoelectronics [9]. Among all layered TMDs, MoS_2 was more popular and thoroughly researched. For example, the intrinsic scatterings in the FET channel of few-layer MoS_2 were previously identified and investigated in detail [10], implying an important issue for making high-performance FETs. Most recently, the high performance of few-layer TMD field-effect transistors (FETs) was especially boosted by choosing better metal electrodes and contact processing [2,11]. It was demonstrated that the yttrium-doping lowered the contact resistance to 69 Ω μm, and that the on-current density reached 1.22 mA/μm for FETs with a gate length of 10 nm [11]. In addition to the contact issue, there are other environmental conditions, like gate dielectrics, device structures, and complementary FETs, leading to modulation of several key indicators of mobilities, subthreshold swings, and hysteresis for

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few-layer MoS_2 FETs [12].

In earlier studies, severe challenges existed when conventional silicon processing technologies were applied to TMDs. For example, atomic layer deposition (ALD) was a mature ultrathin-film preparation technique for high-κ dielectrics in semiconductor technology. However, growing uniform high-κ films on TMDs suffered physical difficulties [13]. In the earlier stage, hexagonal boron nitride (*h*-BN) was introduced as a single dielectric layer or a secondary layer above the substrate. Using *h*-BN significantly improved electron transport in the channel and boosted device performances of TMD FETs [10,14,15]. It implied necessary conditions of atomically flat and dangling-bond-free surfaces, thereby reducing electron scattering for carriers in TMD channels. However, the dielectric constant of the *h*-BN dielectric is ~4.0, which is much lower than other high-κ materials. Recent studies have turned to converting two-dimensional (2D) TMDs, such as TaS_2 and HfS_2, into ultra-flat oxide layers [16,17]. TaS_2 was oxidized using a hot plate in the ambient atmosphere, and the dielectric constant of Ta_2O_5 was estimated to be ~15.5 [16]. HfS_2 was selectively photo-oxidized by laser irradiation, and the dielectric constant of HfO_x was evaluated to be ~15 [17]. Additionally, other oxidation approaches, such as oxygen plasma [18], ozone exposure [19], and oxidation scanning probe lithography [20], were implemented to oxidize TMDs.

The van der Waals contact plays another important role for high-performance FETs. Recent literature has indicated that the thermal evaporation for metal electrode deposition leads to the generation of numerous defects and chemical bonding [21]. The defects and bonding resulted in the defect-induced gap states (DIGS) and metal-induced gap states (MIGS) that could further lead to Fermi-level pinning (FLP) [22–24]. To avoid the creation of DIGS and MIGS, it was proposed that the transfer electrode [21,25,26], van der Waals contact [27–29], and semimetal contact [2] techniques be applied to the preparation of metal electrodes. Graphene, several TMDs, like NbS_2 and TaS_2, and MXene were either inserted between the metal and TMD channel or used as contact electrodes [25,30–32]. Employing these 2D featured materials and van der Waals contact nature significantly avoids difficulties from DIGS, MIGS, and FLP, thus boosting device performances of TMD FETs.

In this study, we integrate the ultra-flat dielectric layer of Ta_2O_5 and the van der Waals contact of TaS_2 to boost the device performance of MoS_2 FETs. Selective area oxidation using a patternable laser writing is performed after the van der Waals TaS_2 contacting electrode is placed without any photolithography procedures. This approach ensures a clean interface without photoresist residues, giving an ultra-flat dielectric layer and a low hysteresis for FETs. The device structure and selective-area laser patterning exhibit a high potential for mass production and scalability for future electronics manufacturing.

2. Method

2.1. Device fabrication

Four-probe TaS_2 and MoS_2 FETs were fabricated on heavily p-doped Si substrates with a 300 nm SiO_2 layer as the back-gate dielectric. Contact electrodes were patterned via electron beam lithography (EBL) and formed by thermal evaporation of 50 nm Au. The Ta_2O_5 parallel plate capacitor adopted a metal-insulator-metal (MIM) configuration. A 50 nm Au bottom electrode was first deposited on a SiO_2 substrate. A few-layer TaS_2 flake was exfoliated and transferred onto the electrode, then oxidized into Ta_2O_5 by 532 nm laser irradiation. The selective oxidation was carried out using a laser with a power density of 28 mW/μm^2, exposure time of 1 s per spot, and spot size of ~300 nm in diameter. The oxidation was performed by raster scanning across the surface with a step of ~500 nm, and the scanning procedure was repeated 10 times to ensure uniform oxidation. Finally, a 50 nm Au top electrode was deposited. Both bottom and top electrodes were defined by EBL and deposited by thermal evaporation. The MoS_2 FETs incorporated a high-κ dielectric layer of Ta_2O_5. The fabrication began by defining a trench using EBL and etching it to a depth of 50 nm with a buffered oxide etch (BOE) solution. This trench was filled with a Ti/Au (10/40 nm) layer to make the embedded gate. Next, a TaS_2 flake was transferred and patternable laser-oxidized to form Ta_2O_5 using the same oxidation parameters as the MIM capacitors. A few-layer MoS_2 flake was transferred and served as the channel material. Source and drain electrodes were formed using thermally evaporated Au (100 nm), Bi/Au (30/50 nm), or unoxidized TaS_2 flakes defined during the laser oxidation step. The bulk MoS_2 crystal was purchased from SPI Co., while the TaS_2 bulk crystal was provided by Prof. Ching-Hwa Ho (NTUST, Taiwan).

2.2. Electrical properties measurements

The transfer characteristics of the FETs were measured using high-precision electrometers (Keithley 6430 and 2400, Tektronix), a voltmeter (Keithley 2000, Tektronix), and a probe station (TTPX, Lake Shore Cryotronics Inc.) under a high-vacuum environment. The FET behavior was assessed using a two-terminal and four-terminal configuration. In the two-terminal configuration, the drain-source voltage (V_{DS}) was fixed at 1 V, and the transfer current was recorded with the Keithley 6430 while the back-gate voltage was swept using the Keithley 2400. For the four-terminal configuration, a fixed voltage was applied to the outer electrodes, and the transport current was measured with the Keithley 6430, while the voltage drop between the inner electrodes was monitored using the Keithley 2000. The back-gate voltage was controlled by the Keithley 2400. The sheet Conductivities of the MoS_2 and TaS_2 flakes were extracted from the four-terminal configuration. The dielectric properties of the Ta_2O_5 capacitor were characterized by *C–V* measurements conducted under high-vacuum conditions at room temperature using a precision current–voltage analyzer (B1500A, Keysight). A voltage sweep ranging from +1 V to −1 V was applied across the Ta_2O_5 capacitor, and measurements were performed at three distinct frequencies (1, 3, and 10 kHz).

2.3. Material characterization

The crystal phase and lattice constant of 1T-TaS_2 were determined by X-ray diffraction (XRD) analysis (D2 PHASER, Bruker). The TaS_2 crystal was finely ground into powder and analyzed using Copper K_α radiation (1.5418 Å) and the detector system (LYNXEYE XE-T, Bruker). Nano-X-ray absorption near-edge structure (nano-XANES) (BL21A, Taiwan Photon Source (TPS)) was employed to investigate the transformation of TaS_2 into Ta_2O_5 by analyzing the Ta L_3-edge spectra. Further details for the nano-XANES are provided in the **Supplementary material**. The thicknesses of TaS_2, Ta_2O_5, and MoS_2 were measured using an atomic force microscope (AFM, SPA-300HV, Seiko Instruments Inc.) operated in tapping mode with AFM tips (PPP-RT-FMR, Nano sensors). The AFM tips had a radius of curvature of <10 nm, a resonance frequency of 75 kHz, and a force constant of 2.8 N/m. The cross-section specimen was prepared through dual beam focused ion beam (Dual Beam FIB, Helios 5 Dual Beam, Thermo Fisher Scientific Inc.). Platinum and amorphous carbon layers were first deposited for surface protection. Subsequently, 30 kV ion milling and lift-out with a micromanipulator were performed to obtain thin lamellae, which are affixed onto a TEM grid. The cross-sectional images and energy-dispersive spectrometer (EDS) analysis were obtained at 200 keV by high-resolution scanning transmission electron microscopy (HR-STEM, JEM-2800F, JEOL Ltd.)

3. Experimental results and discussions

Fig. 1**(a)** and 1**(b)** exhibit optical microscope images of four-probe FETs with TaS_2 and MoS_2 flakes, respectively. The inset to Fig. 1**(a)** presents the AFM measurement of the line profile indicated as a dashed line on the SEM image. It reveals the thickness of ~8 nm (9 layers) for the TaS_2 flake. On the other hand, the 3-layer thickness of the MoS_2 flake shown in Fig. 1**(b)** is estimated using the optical contrast measurement.

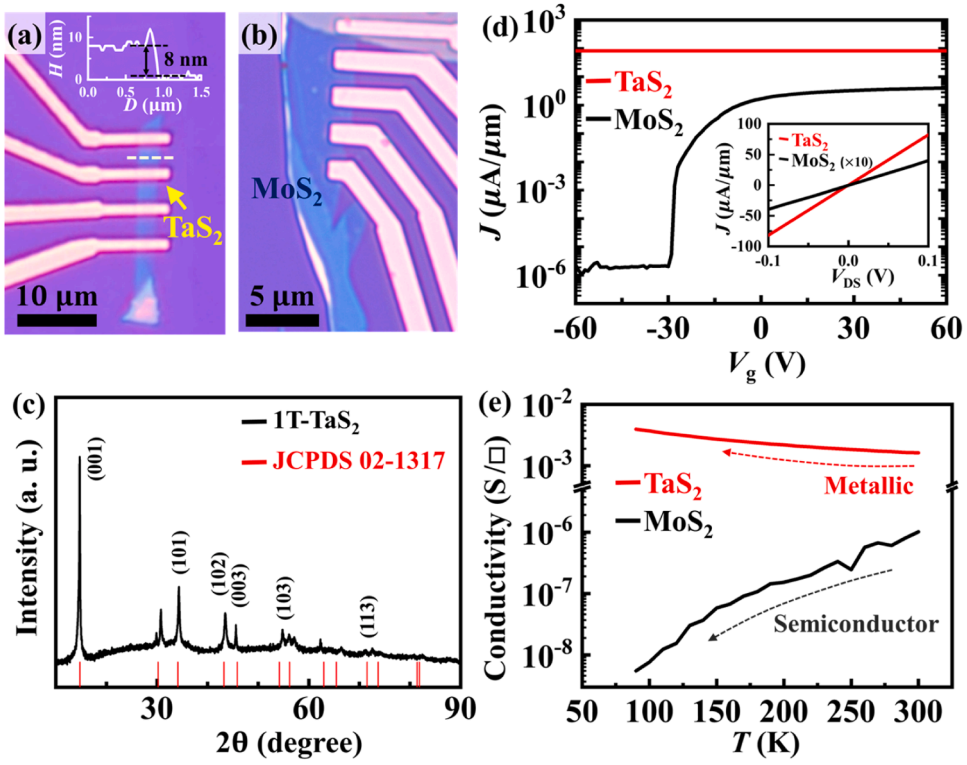

Fig. 1. (a) Optical micrograph with a scale bar for the 9-layer thick 1T-TaS_2 device on the 300-nm thick SiO_2 substrate. The inset displays the line profile of the white dashed segment marked in Fig. 1**a**. (b) Optical microscope of the 3-layer thick MoS_2 FET device on the SiO_2 substrate. (c) XRD spectrum of the 1T-TaS_2 bulk with the standard pattern of red peaks from the JPCDS card No. 02-0137. (d) Current densities as a function of the back-gating voltage, V_g, for the 1T-TaS_2 and the MoS_2 FET devices at a bias voltage of 0.1 V using the source and drain for the two-probe measurement. The inset shows current-voltage (I-V) curves of the 1T-TaS_2 and the MoS_2 FET devices at the V_g of 60 V using the two-probe measurement. The current densities of the MoS_2 FET device are magnified to be 10 times larger. (e) Sheet conductivities as a function of temperature for the 1T-TaS_2 and the MoS_2 FET devices at V_g of 60 V using four-probe measurement.

The crystalline structure of the layered TaS_2 bulk is further characterized by XRD. The XRD spectrum shown in Fig. 1**(c)** with marked lattice planes corresponds to the JCPDS card No. 02-1317, indicating the crystalline phase of 1T-TaS_2 with lattice constants calculated to be $a = 3.341$ and $b = 5.990\text{Å}$. Fig. 1**(d)** presents the TaS2 and MoS2 FET device transfer curves, as shown in Fig. 1**(a)** and 1**(b)** using two-probe measurements at a source-drain voltage (V_{DS}) of 0.1 V and back-gating voltages (V_g) ramping from −60 to 60 V. The TaS_2 FET exhibits a high channel current of 82.38 μA/μm that exposes negligible variation of current densities with regard to the V_g. In contrast, the MoS_2 FET shows an n-type behavior with an on-off ratio of $\sim 10^7$, an on-current density of 3.98 μA/μm, and a mobility of 82.2 $cm^2V^{-1}s^{-1}$. The inset in Fig. 1**(d)** shows linear current-voltage behaviors to confirm an Ohmic contact for TaS_2 and MoS_2 FETs. Fig. 1**(e)** illustrates temperature behaviors of the sheet conductivities of TaS_2 and MoS_2 flakes at the V_g of 60 V using the four-probe measurement. In contrast to the semiconducting feature of the MoS_2 flake, the TaS_2 flake offers a metallic character with a high sheet conductivity of 1.62 mS/ϒ at a temperature of 300 K. The high conductivity of TaS_2 flakes manifests itself as ideal contact electrodes for MoS_2 FETs. The concept is checked and confirmed in **Figure S1** in the **Supplementary material**.

The few-layered TaS_2 flake is area-selectively converted to TaO_x using programmable laser irradiation in the ambient atmosphere. It is attributed to laser-induced photothermal heating, which activates the oxidation of TaS_2 with oxygen and moisture in air, thereby forming amorphous TaO_x in the irradiated region while keeping other regions of TaS_2 intact. Fig. 2**(a)** shows an optical image of a TaS_2 flake on a Si substrate before laser-induced oxidation. A specified area of $2\,\mu m \times 2\,\mu m$ is patterned by laser writing, and the result is presented in Fig. 2**(b)**. The oxidation area, marked by an orange frame, reveals a faded color, indicating material transformation. The transformation is inspected using nano-XANES spectra for the determination of the valence state of Ta atoms. The Ta L_3-edge nano-XANES spectra are displayed in **Fig. S2 in the Supplementary material**. After laser oxidation, a blue shift of the spectrum is clearly observed, which is in line with previous studies of XANES spectra of TaS_2 and Ta_2O_5 and offering clear evidence of the valence state transformation from Ta^{4+} to Ta^{5+} [33,34]. In addition to material conversion, Fig. 2**(c)** reveals a thickness variation before and after laser-induced oxidation, where the thicknesses are measured by AFM. The flake thickness decreases to ~68 % of its original thickness (see the slope in Fig. 2**(c)**). The thickness of Ta_2O_5 ranges from 4.8 to 9.8 nm and can be controlled according to the initial thickness of the TaS_2 flake. AFM topography further reveals that the laser-oxidized Ta_2O_5 possesses an ultra-flat surface with a root-mean-square (RMS) roughness of ~0.812 nm, compared to ~0.700 nm for the pristine TaS_2 flake. Notably, in comparison with Ta_2O_5 films deposited using conventional techniques, the laser-oxidized Ta_2O_5 achieves superior flatness. The comparisons are presented in detail in **Fig. S3 and Table S1 in the Supplementary material**.

The electrical properties of TaS_2 flakes are measured before and after oxidation. Fig. 2**(d)** shows current-voltage (I-V) curves of TaS_2 and Ta_2O_5, corresponding to the optical images of the devices displayed in **Figs. S4(a)** and **S4(b)** in the **Supplementary material**. After laser-induced oxidation on a selective area, the sheet resistivity largely changes from 770 Ω/□ to 370 MΩ/□, indicating a conversion from the metallic TaS_2 to insulating Ta_2O_5. Further, the capacitive properties and breakdown electric fields are investigated. The inset to Fig. 2**(e)** shows the scheme of the metal-insulator-metal device structure and the electrical circuit connection for the capacitive property measurements. Fig. 2**(e)** depicts areal capacitance (C_{ox}) as a function of back gate voltage at three different frequencies from 1 kHz to 10 kHz. The

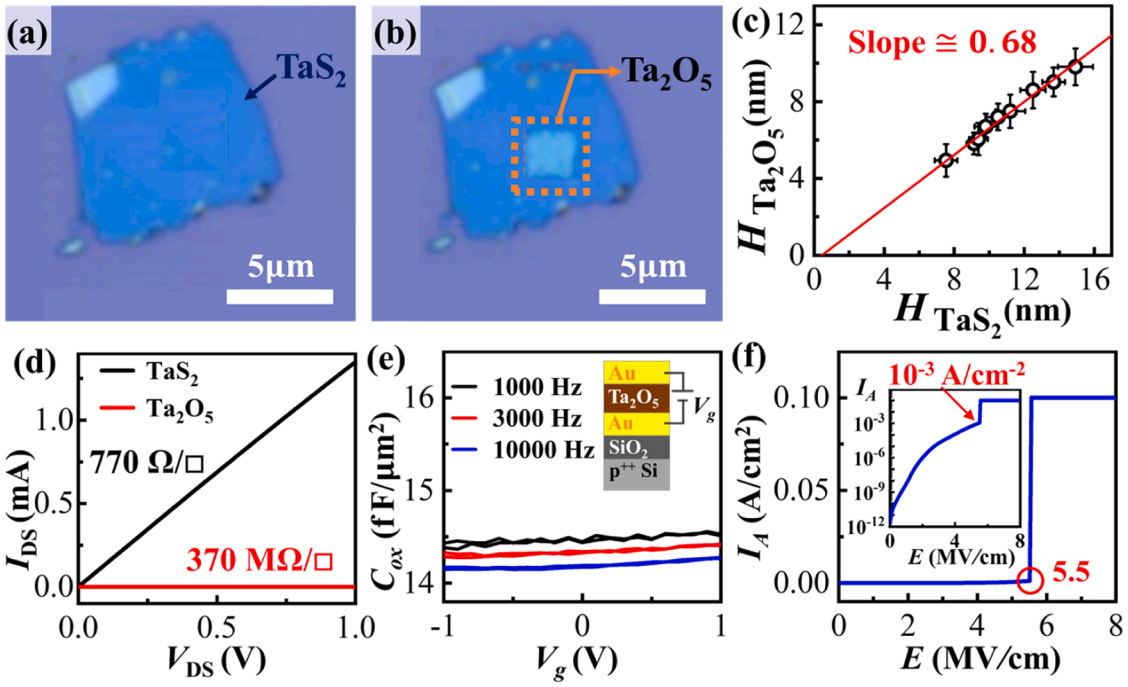

Fig. 2. Optical micrographs with scale bars of a few-layered TaS_2 flake (a) and after (b) laser-patterning oxidation. The orange dashed rectangle indicates the area illuminated by the 532-nm laser. (c) Thickness of the oxidized TaS_2 flake (Ta_2O_5 flake) as a function of its original TaS_2 thickness. The red solid line presents the best linear least-squares fitting to the data, giving a slope of ~0.68. (d) Current as a function of voltage using the two-probe measurement for the same TaS_2 flake before and after laser-induced oxidation. The sheet resistivities are evaluated as about 770 Ω and 370 MΩ for the original TaS_2 and the oxidized Ta_2O_5 flake, respectively. (e) Areal capacitance as a function of gating voltage for a 9.8-nm thick Ta_2O_5 flake measured at frequencies of 1, 3, and 10 kHz. The inset illustrates the device structure and connecting circuit. (f) Areal current density as a function of electric field for the Ta_2O_5 flake. The breakdown field of ~5.5 MV/cm at the pre-breakdown current density of ~0.001 A/cm^2 is marked. The inset offers the same graph with the current density on a logarithmic scale.

dielectric constant (κ) of Ta_2O_5 is evaluated from the areal capacitance according to the equation $C_{ox} = \kappa\varepsilon_0/t$, where ε_0 is the vacuum permittivity of electric fields. The evaluated dielectric constant is in the range from 15.98 to 15.68, revealing a very small change regarding gating voltages and frequencies. Fig. 2**(f)** presents the areal current as a function of the electric field and gives the breakdown electric field of ~5.5 MV/cm at a current density of ~0.001 A/cm^2 for Ta_2O_5. The inset to Fig. 2**(f)** provides a view of the electric field behavior on a logarithmic scale.

To demonstrate patternable laser oxidation, we make MoS_2 FETs with an embedded gate electrode and a Ta_2O_5 layer. The Ta_2O_5 layer is converted from a specific thickness of a TaS_2 flake through patternable laser-induced oxidation. Fig. 3**(a)** shows a schematic diagram of the embedded-gate MoS_2 FET. The source/drain contact electrode is directly deposited on the surface of the MoS_2 flake. Fig. 3**(b)** presents a typical optical image of a MoS_2 FET (Device MS-TaO-Au3) with a Ta_2O_5 dielectric layer and directly contacted Au electrodes. All represented devices with physical parameters and device performances are listed in **Table S2** in the **Supplementary material**. The MoS_2 FET in Fig. 3**(b)** consists of a 7-layer-thick MoS_2 flake and a 6.0-nm-thick Ta_2O_5 layer. The transfer curves, current density (J) as a function of V_g, in linear and logarithmic scales for the Device MS-TaO-Au3 after annealing at 170 °C in a high vacuum (<10^{-6} Torr) for 30 min are shown in Fig. 3**(c)**. The measurements are carried out at the source-drain voltage (V_{DS}) of 1 V with V_g ranging from −2 to 1 V at room temperature. The on-current density is ~3.6 $\mu A/\mu m$ at V_g of 1 V, where the device channel length (L) is ~4.0 μm On the logarithmic scale, the minimum subthreshold swing (SS) is calculated to be ~62.2 mV/dec at 300 K from the slope of the green linear fitting line in the subthreshold region, according to $1/SS = d(\log J)/dV_g$ [35]. A more detailed analysis of the annealing temperature and the SS as a function of current density is provided in **Figs. S5** and **S6(a)** in the **Supporting Information**. The field-effect mobility (μ) of ~1.43 cm^2/V s is obtained from the current density in linear scale using the equation of $\mu = (dJ/dV_g)(LC_{ox}/V_{DS})$, where dJ/dV_g is obtained from the slope of the blue linear fitting line in the linear scale. The C_{ox} of 15.98 is used in the calculation (see description of Fig. 2**(e)**). The linear scale in Fig. 3**(c)** further gives the evaluation of the threshold voltage (V_{th}) of about −0.6 V, which is the intercept of the linear fitting (the blue dotted line) and the zero current density. In addition, the corresponding gate leakage current (I_g) is below 1.4 × 10^{-14} A/μm, which is the minimum detection limit of the current meter and shown as the gray dotted line in Fig. 3**(c)**. To assess the interface quality of the Ta_2O_5 layer, we perform the hysteresis loop measurements of the transfer curve. The hysteresis in the transfer curve for Device MS-TaO-Au3 is about 0.15 V (see **Fig. S7** and corresponding descriptions in the **Supplementary material**).

The importance of the van der Waals contact and the capability of the patternable laser-induced oxidation are mentioned previously in the introduction. The concept has materialized as presented in Fig. 4**(a)**. The insert provides atomic structures of the scheme for the TaS_2 contacts on both the MoS_2 channel and the Au electrode. Only the specified region in dark brown of the TaS_2 flake is selectively oxidized and converted to the Ta_2O_5 dielectric layer. Fig. 4**(b)** shows the top-view optical micrograph of the Device MS-TaO-TaS1, and Fig. 4**(c)** displays the corresponding transfer curves measured after annealing at 170 °C for 30 min. With the TaS_2 used as a van der Waals contact, the on-current density increased to ~6.3 $\mu A/\mu m$, and the mobility is ~4.83 cm^2/V s, where the device channel length is ~4.0 μm In addition, the subthreshold swing is a little bit lowered to be ~59.8 mV/dec with a hysteresis of ~0.15 V at 300 K, and the detailed analysis of the SS as a function of current level is provided in **Fig. S6(b)** in the Supporting Information. Notably, this value is close to the thermodynamic limit in theory, which can be expressed as $SS_{limit} = (k_BT/q)\ln(10) \approx 59.526$ mV/dec, where k_B is the Boltzmann constant, $T = 300$ K is the temperature and q is the charge. The

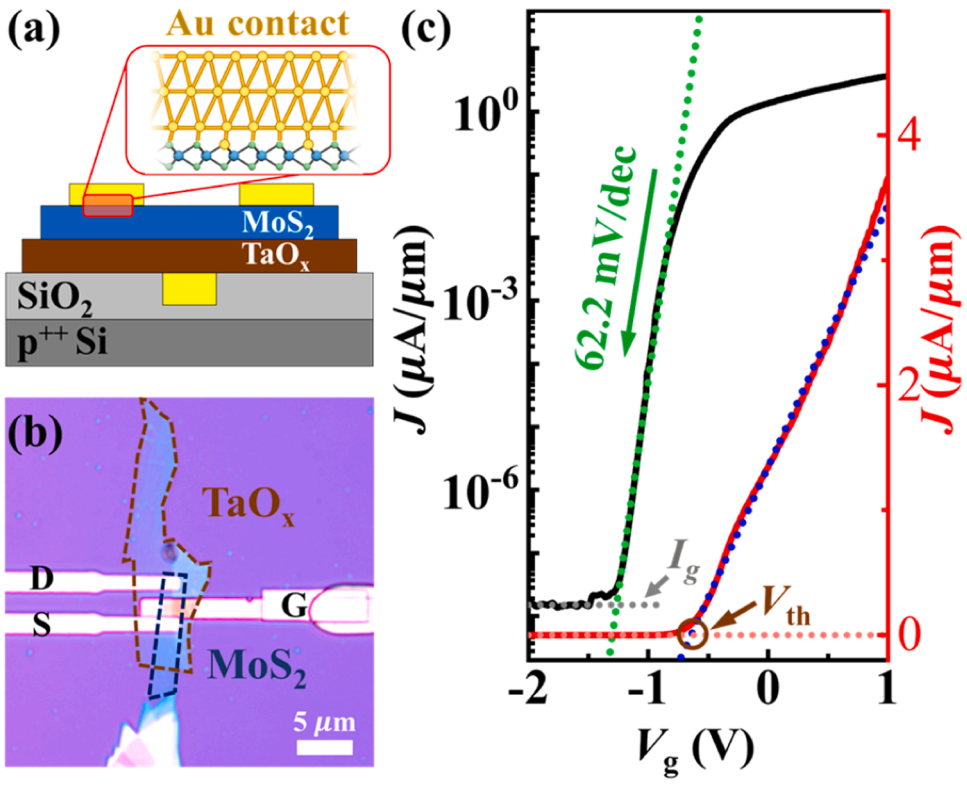

Fig. 3. (a) Schematic diagram of the MoS_2 FET device with Au as a metal contact and Ta_2O_5 as a dielectric. (b) Optical micrograph of the Device MS-TaO-Au3 of Au-contacted MoS_2 FET on the Ta_2O_5 dielectric. The dark brown dashed frame indicates the Ta_2O_5 dielectric, which is below the MoS_2 flake (marked by the blue dashed frame). The source, drain, and gating electrodes are labeled by S, D, and G characters, respectively. (c) Current density as a function of embedded gating voltage for the Device MS-TaO-Au3. The corresponding gate leakage current (I_g) is shown as the gray dotted line on the logarithmic scale. The threshold voltage (V_{th}) is denoted, and the subthreshold swing is estimated to be ~62.2 mV/dec.

performance metrics and parameters of other devices are summarized in**Table S2** of the **Supplementary Material**. On average, the TaS_2 contacted MoS_2 FETs show higher current densities as compared with Au contacted MoS_2 FETs. To further explore the contact issue in the MoS_2 FET devices, we further make devices with a direct metal contact, while the Bi is selected to replace the Au metal contact. Device MS-TaO-Bi2 is the Bi-contacted MoS_2 FET, and it reveals an on-current density of ~34.7 μA/μm at V_{DS} of 1 V with channel length of 1.0 μm It also reveals an *SS* value of 68.7 mV/dec at a low V_{DS} of 0.1 V. The tendency of lower *SS* value is observed at a low driving V_{DS}. The corresponding gate leakage current is below 1.3×10^{-14} A/μm, indicated by the gray dotted line in Fig. 4**(c)**. Table 1 summarizes the *SS* values for most of TMD FETs with several different dielectric materials. It is noted that the dielectric of Ta_2O_5 achieves the lowest *SS* value. This work also presents the benefits of controllable thickness and patternable oxidation for converting TaS_2 to an ultra-flat Ta_2O_5 layer. On the other hand, we also make MoS_2 FETs with other dielectric materials, such as SiO_2, Si_3N_4, and *h*-BN, for comparison. Transfer curves of MoS_2 FETs on dielectrics of Ta_2O_5, *h*-BN, SiO_2, and Si_3N_4 are displayed in **Figs. S8(a)–S8(d)**, and the device performances are summarized in **Fig. S9** and **Table S3** in the **Supplementary material**. In comparison to other dielectrics, the Ta_2O_5 dielectric for FETs reveals the lowest interface trap states of 3.23×10^{-11} $eV^{-1}cm^{-2}$. The MoS_2 FETs on the Ta_2O_5 dielectric exhibit the lowest *SS* value and the smallest hysteresis, all confirming the superior feature of the Ta_2O_5 dielectric layer.

The cross-sectional scanning transmission electron microscope (STEM) with energy-dispersive X-ray spectroscopy (EDS) mapping for elemental analyses is implemented to check the dielectric layer of Ta_2O_5. Fig. 5**(a)** shows the optical micrograph of Device MS-TaO-TaS1. The red line indicates where the section specimen of the cross-sectional area is prepared by a focused ion beam (FIB). The corresponding STEM image of the section specimen, consisting of the source, drain electrodes, and the embedded gate electrode, is presented in Fig. 5**(b)**. The area marked in the red rectangle is closely inspected and shown as a high-resolution STEM image in Fig. 5**(c)**. Regions i and ii represent the contact and embedded back electrodes, respectively. Region iii displays the MoS_2 channel, TaS_2 flake, and Ta_2O_5 between SiO_2 and Pt. High-resolution STEM images of regions close to the contact and gate electrodes are exhibited in **Figs. S10(a)** and **S10 (b)**, respectively. The STEM image of the area close to the gate region shows the MoS_2 on Ta_2O_5 (**Fig. S10(a)**), while that of the area close to the contact region reveals the unoxidized TaS_2 used as a van der Waals contact electrode (**Fig. S10 (b)**). The remaining Regions v and vi in Fig. 5**(c)** mark the protection layers of Pt and amorphous carbon for the FIB cross-sectioning. Figs. 5 **(d)** and 5**(e)** display EDS elemental mapping for Regions i and ii, respectively. Fig. 5**(d)** shows Ta and S elements distributed in the same depth, which indicates the TaS_2 contact electrode. In contrast, Fig. 5**(e)** shows clear oxygen elements near the gate electrode, where the TaS_2 flake is oxidized to Ta_2O_5 layer. The detailed depth distributions of individual elements are provided in Figs. 5**(f)** and 5**(g)** for the contact and gate regions, respectively. The depth distributions of Ta and O elements offer curves for the calculation of areas under the curves, which confirms again the ratio of approximately 2 to 5 for Ta and O elements in Ta_2O_5.

4. Conclusions

We have demonstrated patternable oxidation to convert a 1T-TaS_2 flake to an ultra-flat Ta_2O_5 dielectric layer with a thickness of 5–6 nm. The patternable capability leads to the fabrication of either direct metal- or 2D TaS_2 van der Waals-contacted MoS_2 FETs. The dielectric properties of Ta_2O_5 are characterized to reveal its dielectric constant κ of ~15.98 and its breakdown electric field of ~5.5 MV/cm. The nano-

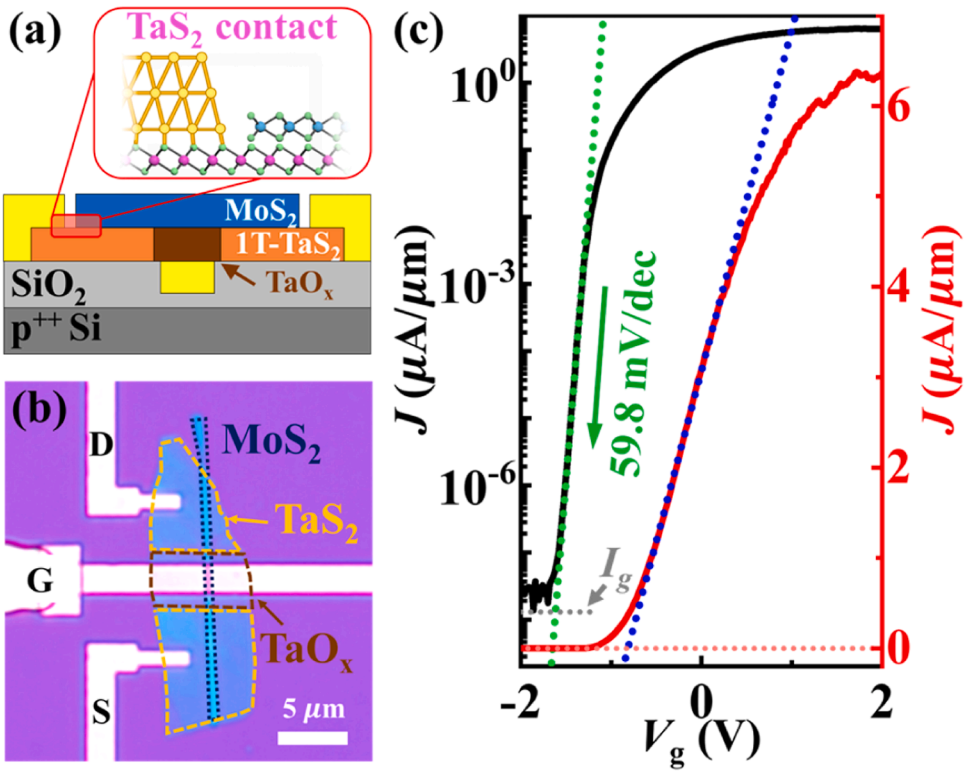

Fig. 4. Schematic diagram of the MoS_2 FET device with TaS_2 as a metal contact and Ta_2O_5 as a dielectric. (b) Optical micrograph of the Device MS-TaO-TaS1 of TaS_2-contacted MoS_2 FET on the Ta_2O_5 dielectric. The dark brown, blue, and orange dashed frames point to the Ta_2O_5 dielectric, MoS_2 flake, and TaS_2 flake. (c) Current density as a function of embedded gating voltage for the Device MS-TaO-TaS1. The corresponding gate leakage current (I_g) is shown as gray dotted line on the logarithmic scale. The subthreshold swing is evaluated as ~59.8 mV/dec.

Table 1
SS values of TMD FETs from our work in comparison with others' results. TG, BG, SG, and DG are the abbreviations of top gate, back gate, single gate, and double gate. *Vertical-channel FET.

TMD	Dielectric	T_{ox} (nm)	L (μm)	W (μm)	Gate	*SS* (mV/dec)	Refs.
3L-MoS_2	Ta_2O_5	5.5	4	0.5	SG	59.8	Our work
9L-MoS_2	Ta_2O_5	31	5	5	SG	61	[16]
MoS_2	*h*-BN	4	0.009	2	SG	93	[36]
2L-MoS_2	ZrO_2	5.8	0.5	2.5	SG	65	[37]
3L-WS_2	HfO_2	2.8	0.04	-	SG	67.1	[38]
4L-MoS_2*	HfO_2	10	0.0087	-	SG	73	[39]
MoS_2	Gd_2O_5	8.5	3	4	SG	61.5	[40]
Bi_2O_2Se	Bi_2SeO_5	5	10.4	34.3	SG	75	[41]
1L-MoS_2	PTCDA/HfO_2 (TG)	3	2.4	5.2	DG	60	[42]
	Al_2O_3 (BG)	30					
7L-MoS_2	*h*-BN (TG)	8.9	8	8	DG	65.5	[43]
	h-BN (BG)	8.4					

XANES spectra and the STEM equipped with depth distribution of Ta and O elements are used to determine the ratio of 2 to 5 in the Ta_2O_5 dielectric layer. Further, the STEM images present the ultra-flat Ta_2O_5 layer as well as the perfect van der Waals contact of TaS_2 on the MoS_2 channel. The Bi-contacted MoS_2 FET on the Ta_2O_5 dielectric shows a high on-current density of ~34.7 $\mu A/\mu m$ at a channel length of 1.0 μm In addition, the TaS_2-contacted MoS_2 FET on the Ta_2O_5 dielectric presents the lowest *SS* value of 59.8 mV/dec and the smallest hysteresis of 0.15 V. The van der Waals contact features a damage-free 2D channel surface and the prevention of the Fermi level pinning. Comparing the Ta_2O_5 to SiO_2, Si_3N_4, and *h*-BN dielectrics, the MoS_2 FET on the ultra-flat and thin Ta_2O_5 dielectric possesses the lowest *SS* value, the lowest interface trap states, and the smallest hysteresis, indicating the superior feature of its dielectric properties for making 2D FETs.

CRediT authorship contribution statement

Kuan-Cheng Lu: Writing – original draft, Validation, Methodology, Investigation, Conceptualization. **Pen-Yuan Shih:** Investigation, Data curation. **Pin-Hsien Lin:** Investigation, Data curation. **Shih-Hao Wu:** Investigation, Data curation. **Kimitoshi Kono:** Resources. **Wen-Bin Jian:** Writing – review & editing, Validation, Supervision, Resources, Project administration, Funding acquisition, Conceptualization. **Yu-Han Lin:** Data curation. **Yo-Yao Ho:** Data curation. **Ching-Hwa Ho:** Resources. **Shin-Yuan Wang:** Data curation. **Chao-Hsin Chien:** Resources. **Ching-Yu Chiang:** Resources. **Shu-Jui Chang:** Resources. **Yu-Che Huang:** Resources. **Kenji Watanabe:** Resources. **Takashi Taniguchi:** Resources. **Kazuhito Tsukagoshi:** Resources. **Chenming Hu:** Resources.

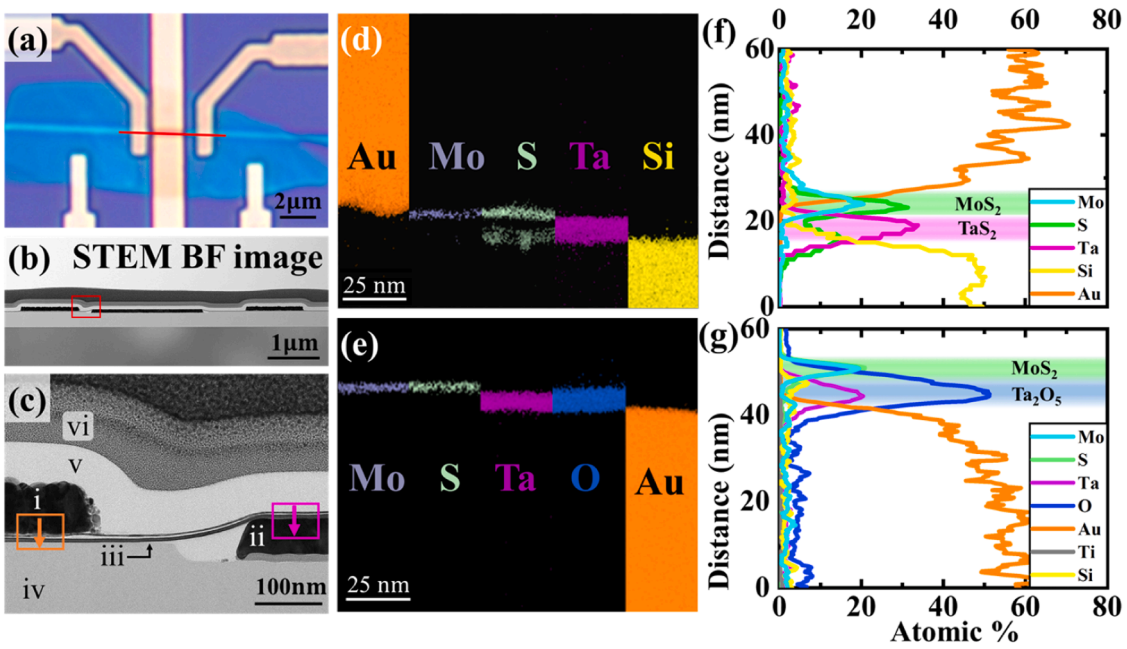

Fig. 5. Optical micrograph of the Device MS-TaO-TaS1 of TaS_2-contacted MoS_2 FET on the Ta_2O_5 dielectric. (b) Bright field image of the cross-sectional STEM for the red line indicated in Fig. 5(a). (c) High-resolution STEM image of the area denoted by the red frame in Fig. 5(b). The symbols for the regions are the contact electrode (i), the gate electrode (ii), the channel of $MoS_2/TaS_2(Ta_2O_5)$ (iii), the substrate of SiO_2 (iv), the Pt metal (v), and the amorphous carbon (vi). (d) EDS mapping of the contact electrode (Region i in Fig. 5(c)). The elements Au, Mo, S, Ta, and Si are colored in orange, light blue, green, purple, and yellow, respectively. (e) EDS mapping of the gate electrode (Region ii in Fig. 5(c)). The elements Mo, S, Ta, O, and Au are colored in light blue, green, purple, deep blue, and orange. (f) Line profile of the EDS mapping for Region i marked by the orange frame. The sections of MoS_2 and TaS_2 are colored in green and pink. (g) Line profile of the EDS mapping for Region ii marked by the purple frame. The sections of MoS_2 and Ta_2O_5 are colored in green and blue, respectively.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Wen-Bin Jian reports financial support was provided by National Science and Technology Council Taiwan. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Supplementary materials

Supplementary material associated with this article can be found, in the online version, at doi:10.1016/j.apsadv.2026.100955.

Data availability

Data will be made available on request.

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