Reliability Challenges in Equivalent-Oxide-Thickness Scaling with High-κ Er_2O_3 Dielectrics on two-dimensional MoS_2 Field-Effect Transistors

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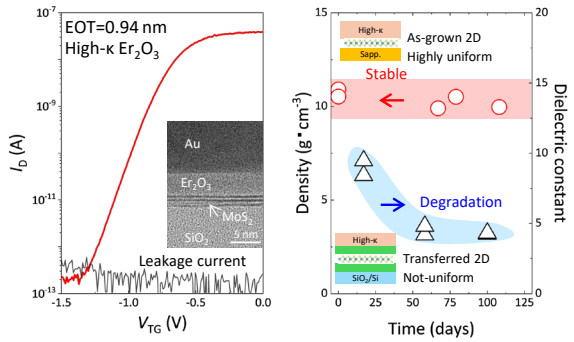
ABSTRACT

The integration of high-κ films with two-dimensional (2D) semiconductors offers a pathway to advance metal-oxide-semiconductor technology scaling. While reliability studies on gate stacks with 2D semiconductors have focused on device performance instabilities, the stability of bulk dielectric properties, particularly for ultrathin high-κ films on 2D semiconductors, remains underexplored. This work demonstrates the scalability of high-κ Er_2O_3 on mechanically-transferred MoS_2, achieving an equivalent oxide thickness below 1 nm. However, the critical issue: a time-dependent degradation of the dielectric constant, which persists despite various passivation methods, is identified. Notably, this instability is absent when the high-κ film is deposited on the clean surface of MoS_2 grown on a sapphire substrate, revealing that the

degradation originates from suboptimal surface conditions of the 2D semiconductor rather than the dielectric itself. These findings highlight the necessity of addressing 2D material surface effects to fully realize the potential of ultrathin high-κ dielectrics in future device applications.



KEYWORDS: MoS_2, high-κ Er_2O_3, dielectric constant, leakage current, reliability

Reducing the equivalent oxide thickness (EOT) of high-κ gate oxides has been a widely adopted strategy to enhance electrostatic integrity and mitigate short-channel effects in Si technology.[1] So far, the conventional metal/high-κ gate stacks on Si have achieved EOT values below 0.5 nm,[2–4] with the lowest EOT of 0.25 nm achieved using cubic HfO_2 with κ of 40 and a physical thickness of 2.4 nm.[4] The emergence of two-dimensional (2D) semiconductors has sparked interest in integrating high-κ materials on 2D platforms,[5] since the successful scaling of EOT on 2D materials offers the potential to overcome the performance limitations of conventional Si technology.[6] This is attributed to the enhanced electrostatic integrity arising from their atomic-scale thickness.

Recent advancements have demonstrated EOT scalability through the utilization of transfer techniques, a distinctive feature inherent to 2D materials.[7–12] For instance, single-crystalline Al film was deposited onto a separate graphene substrate, and upon detachment, the Al surface underwent natural oxidation, forming a high-quality, single-crystalline Al_2O_3 insulator with a thickness of 1.25 nm. This oxide was subsequently transferred onto a 2D

material to serve as a top-gate insulator, achieving an EOT of 0.77 nm and an interface state density (D_{it}) of less than 10^{10} $cm^{-2}eV^{-1}$.[9] These findings offer valuable insights into gate stack design. However, in the context of integration, it is anticipated that the variability introduced by the transfer process will become increasingly significant, highlighting the advantages of conventional deposition methods. Although atomic layer deposition (ALD) has been extensively employed for depositing high-κ oxides onto 2D materials,[13–16] substantial reductions in thickness remain hindered by the need for a buffer layer.

We have developed a novel direct deposition system for high-κ Er_2O_3, utilizing thermal evaporation in a differential-pressure type chamber,[17] as shown in **Figure S1a**. Er_2O_3 possesses remarkable chemical stability under ambient conditions, primarily due to its single +3 oxidation state, coupled with a high dielectric constant (15–20) and a sufficiently wide bandgap (~6 eV), characteristics akin to those of HfO_2. Consequently, by selecting Er_2O_3 and MoS_2, it is feasible to achieve an analogous band alignment to that of the HfO_2/Si interface, as illustrated in **Figure S1b**. This alignment holds a significant promise in terms of electrical reliability, particularly in terms of mitigating gate leakage currents. Thermally evaporated rare-earth oxides, which successfully attained an EOT of 1.1 nm with Er_2O_3 at a physical layer thickness of 5.3 nm on MoS_2-based field-effect transistors (FETs),[17] demonstrate significant potential to fulfill the evolving demands for further EOT scaling. The reliability challenges inherent to high-κ/2D material stacks are pivotal for their practical deployment in electronic devices,[18,19] Intrinsic and extrinsic defects at or near the high-κ/2D interface represent critical factors contributing to device performance instability. These defects are closely associated with physical and device properties such as D_{it},[20–27] threshold voltage (V_{th}) shifts,[28–30] and hysteresis, which depend upon the capture and emission time constants under an applied electric field.[31] Additionally, time-dependent dielectric breakdown (TDDB) results from defect generation and diffusion within the oxide layers.[32] While these properties exhibit clear field-dependent characteristics, one

crucial yet underexplored parameter is the dielectric constant. Notably, the hydration nature of Er_2O_3, like many other rare-earth oxides, is suspected to exacerbate instability when employed as a dielectric layer. This consideration suggests that the bulk stability of dielectrics, particularly their interactions with environmental factors such as moisture,[33] warrants further investigation. Addressing and mitigating these stability challenges is essential for enhancing the reliability of high-κ/2D stacks in advanced electronic applications.

In this study, we successfully achieved an EOT of 0.94 nm in top-gate MoS_2 FETs by reducing the physical thickness of Er_2O_3 to 3.5 nm, resulting in low operating voltage and excellent leakage current characteristics. However, extensive device fabrication revealed significant fluctuations in the dielectric constant when the thickness of Er_2O_3 was reduced below 5 nm, accompanied by degradation over time, implying a potential involvement of moisture. This paper examines the effects of moisture during the device fabrication process and the influence of atmospheric moisture after fabrication and discusses the electrical reliability of high-κ top-gate dielectrics. Furthermore, the origin of the dielectric degradation phenomenon was explored by comparing the dielectric properties obtained from capacitance-voltage (*C*-*V*) measurements of Er_2O_3 deposited on various substrates.

The most effective approach for achieving EOT scaling involves the thinning of the dielectric layer. Due to the extremely slow Er_2O_3 deposition rate at approximately 3 pm/s, precise control over the layer thickness is possible, enabling a range from 1 to 20 nm by adjusting the deposition duration. Previous research employing a 5.3-nm Er_2O_3 layer has demonstrated the scalability of the EOT approach down to 1.1 nm.[17] Here, we demonstrate EOT scaling in dual-gate bilayer MoS_2 FET with 3.5-nm Er_2O_3, as shown in **Figure 1a, b**. The details of device fabrication method can be seen in the section of **Materials and methods** in Supporting Information. The I_D-V_{TG} curves reveal that the MoS_2 channel can be effectively modulated within 1 V top-gate bias (V_{TG}) with an on/off current ratio exceeding 10^6, indicating

the high capacitance of top-gate dielectric. The V_{th} is approximately –1.3 V for back gate voltage (V_{BG}) = 0 V, indicating slight electron doping in the channel through the top-gate integration. The two-terminal carrier mobility (μ), extracted using the Y-function method,[34] is approximately 7 cm^2/Vs. This relatively low μ value may be attributed to contact resistance and scattering from remote phonons in high-κ dielectric,[35] as defect formation during high-κ dielectric deposition is effectively mitigated in this low kinetic energy deposition process. The cross-sectional transmission electron microscopy (TEM) of typical Er_2O_3 top gate devices shown in **Figure 1c** reveals the uniform Er_2O_3 film and its amorphous nature.

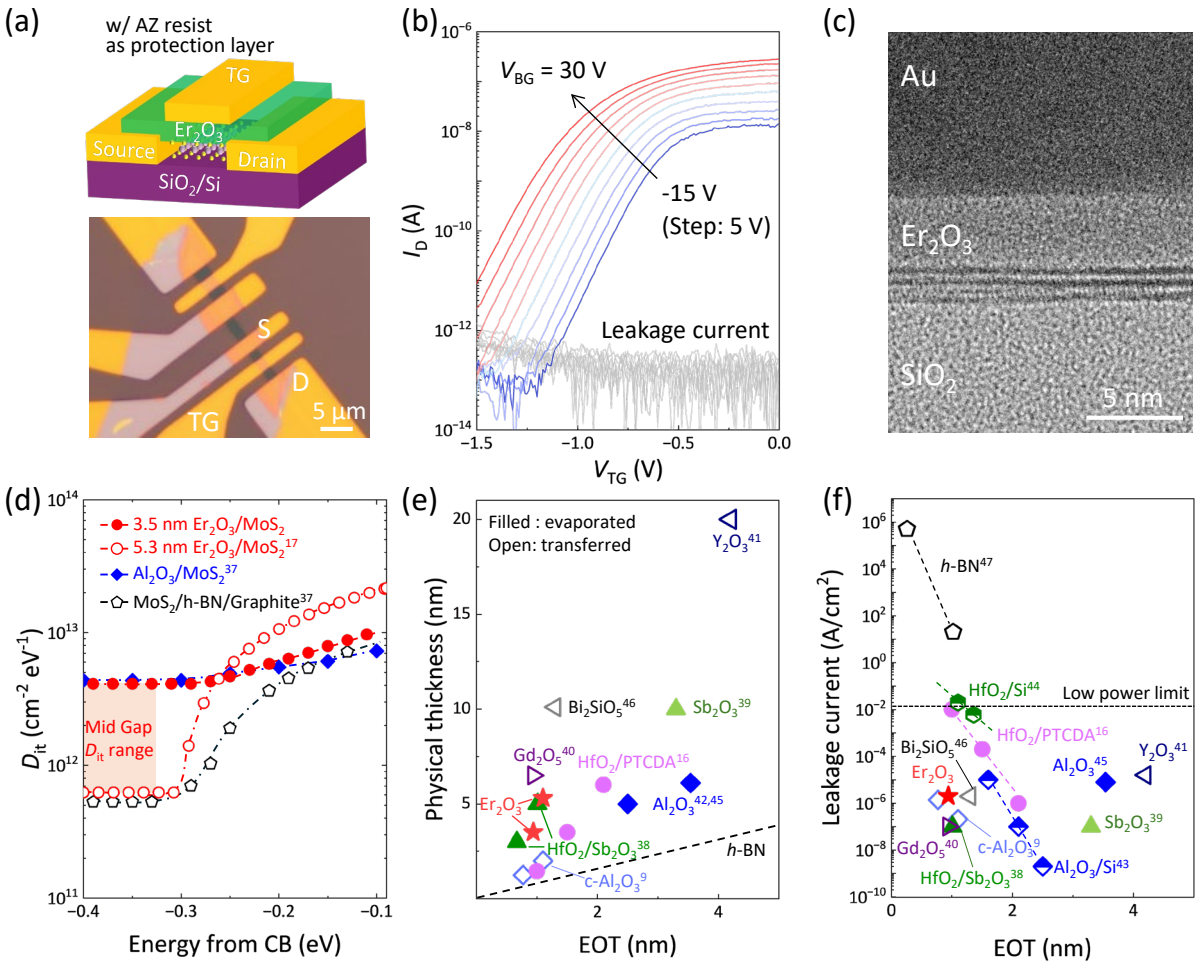


Figure 1 (a) Schematic and optical image of Er_2O_3 top-gate bilayer MoS_2 FET. (b) I_D-V_{TG} characteristics of 3.5-nm Er_2O_3 top-gate MoS_2 FET with EOT = 0.94 nm at V_D = 0.1 V. (c) Cross-sectional image of typical top-gate Er_2O_3 on bilayer MoS_2. (d) D_{it} distribution as a function of energy below the conduction band for a 3.5-nm Er_2O_3 top-gate MoS_2 FET. Other gate stack data is also included. Benchmark of (e) physical thickness

and (f) leakage current density at V_{TG} = 1 V as a function of EOT for recent advanced high-κ materials. The top gate device data is only shown here.

The capacitance of the top gate (C_{TG}) is extracted by the capacitive coupling between V_{TG} and V_{BG}, utilizing the relationship $V_{TG}/V_{BG} = -C_{BG}/C_{TG}$,[36] as 3.68 μm/cm^2, where back gate capacitance (C_{BG}) is estimated based on 90 nm SiO_2, leading to the scaling of the EOT down to 0.94 nm (**Figure S2a**). The dielectric constant extracted for a 3.5-nm-thick Er_2O_3 is approximately 14.5, slightly lower than that observed in 5.3-nm-thick Er_2O_3.[17] The low leakage current (~2×10^{-13} A) suggests good insulating properties even for the physical thickness of 3.5 nm, attributed not only to the large band offset but also to minimal pinholes in Er_2O_3 films. The D_{it}, extracted from *I-V* characteristics by considering the carrier statistics through the quantum capacitance (C_Q),[37] indicates that the interface quality between 3.5-nm Er_2O_3 and MoS_2 is comparable to that of Al_2O_3 formed by ALD, as shown in **Figure 1d**. The relatively large D_{it} aligns with the large subthreshold swing (*S.S.*) of 121 mV/dec, despite the large C_{TG}, as detailed in **Figure S2b**. To date, the best D_{it} achieved by Er_2O_3 deposition is on the order of 6×10^{11} cm^{-2} at the energy of –0.4 eV from conduction band edge.[17] Through the present study, it was revealed that the variation of D_{it} was in the range from 6×10^{11} to 5×10^{12} cm^{-2}eV^{-1}. The variability in D_{it} appears to be inevitable due to the strain in MoS_2 introduced during the Er_2O_3 deposition, which will be discussed later.

A sufficient budget for the physical thickness of high-κ oxide is crucial for further EOT scaling. To assess Er_2O_3 as a potential dielectric for further EOT scaling, we benchmarked the physical thickness and leakage current density of recently developed advanced high-κ materials, including their stacks, as a function of EOT,[9,16,38–47] as shown in **Figure 1e-f**. In the context of the data presented for top-gate devices, it is noteworthy that filled circles represent deposited oxides on top of 2D materials, while open circles denote transferred oxides. *h*-BN is not a viable candidate due to direct tunneling dominating as the EOT approaches 1 nm. Other crystalline

oxide insulators, including Al_2O_3,[9] Y_2O_3,[41] and Gd_2O_5,[40] demonstrate potential due to their high dielectric constants arising from their crystalline nature. However, challenges remain in the transfer processes for device integration and precise control of thickness. In contrast, the current state-of-the-art EOT scaling, based on conventional ALD-HfO_2 seeded by PTCDA[16] and Sb_2O_3,[38] achieves an EOT of 1 nm while satisfying the low standby power requirement (leakage current density < 1.5×10^{-2} A/cm² at V_{TG} = 1 V). Compared to these deposited oxides, it is suggested that Er_2O_3 offers additional potential for physical thickness reduction.

To further scale the EOT, the physical thickness of Er_2O_3 was reduced to 2.8 nm. However, as shown in **Figure 2a**, the dielectric constant for the 2.8-nm-thick Er_2O_3 on MoS_2 FETs experienced a substantial reduction to less than 5, compared to the maximum value of 14.5 observed for the 3.5-nm-thick Er_2O_3. Note that these data were obtained for monolayer and bilayer MoS_2 FFTs and all devices were fully protected by 1.3-μm-thick photoresist (AZ1500). Given that the reliability of ultrathin high-κ dielectrics on 2D MoS_2 remains a significant concern, this study focuses on the variations in the dielectric constant of Er_2O_3 in MoS_2 FETs. First, the temporal evolution of the dielectric constant was examined. As shown in **Figure 2a**, the dielectric constat diminished by nearly 50% after more than 50 days of storage in a vacuum desiccator. This reduction is independent of the Er_2O_3 thickness. Conversely, *S.S.* improved over time, as shown in **Figure 2b**, likely due to the relaxation of strain in MoS_2 introduced during Er_2O_3 deposition since defect states of S vacancies in MoS_2 cannot be recovered with time.[17,37] This is further supported by low-temperature photoluminescence (PL) spectra (**Figure S3**), which reveal that the deposition process does not adversely affect the intrinsic properties of MoS_2. In conventional high-κ/Si systems, a reduction in top gate capacitance alongside an improvement in the interface is often attributed to the formation of an interfacial layer. However, the cross-sectional TEM image in **Figure 1c** shows no evidence of such a layer, suggesting that attributing the reduction in dielectric properties to interface degradation may be unwarranted.

Instead, the bulk properties of ultrathin high-κ dielectrics, particularly rare-earth metal oxides, are known to exhibit poor resistance to water exposure, as observed in La_2O_3[48] and Y_2O_3.[49] Therefore, the reaction between Er_2O_3 and water thus warrants further investigation.

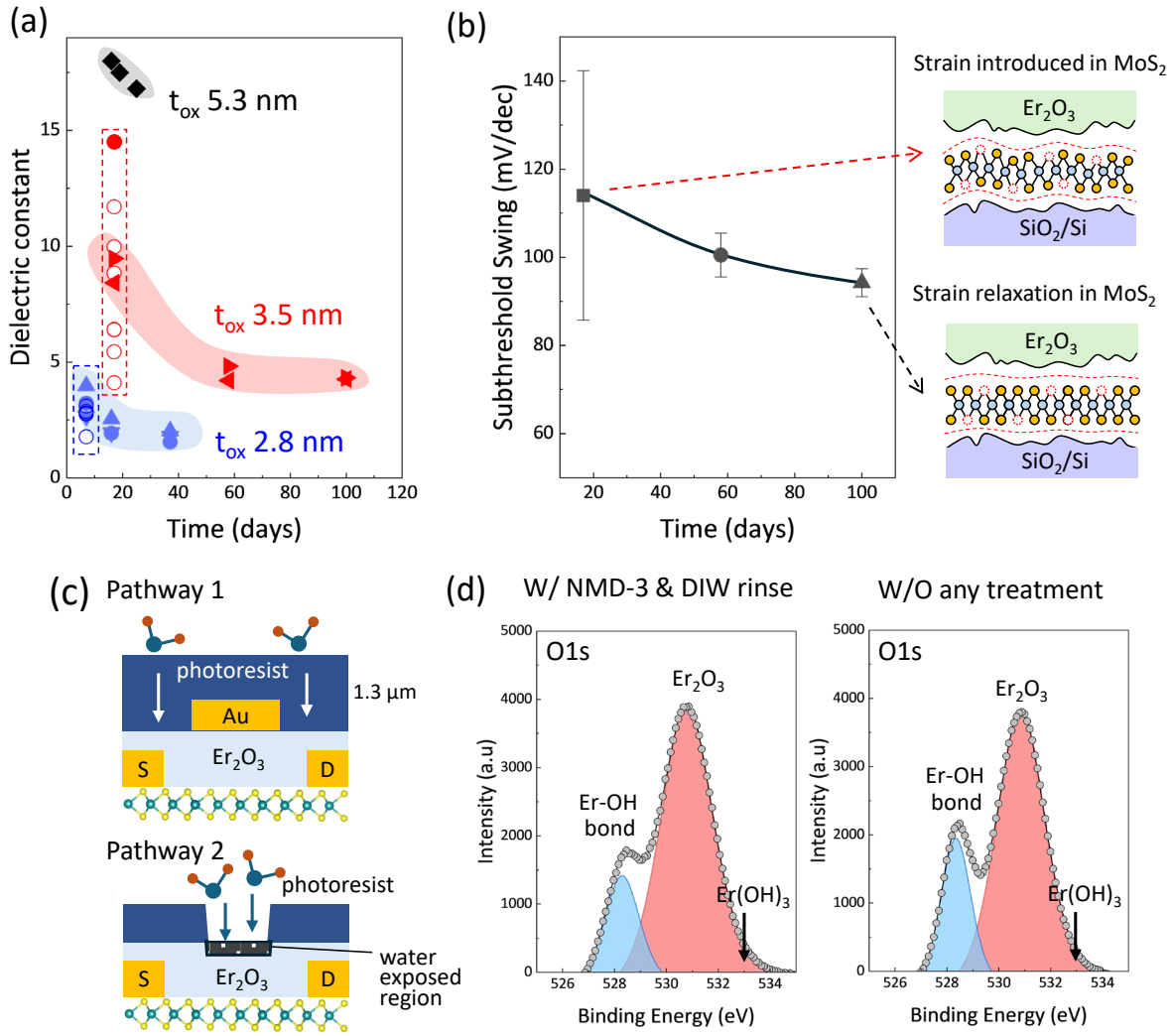


Figure 2 (a) Dielectric constant and (b) subthreshold swing of Er_2O_3 top-gate MoS_2 FETs swing as a function of time. Open circle represents dielectric constant extracted from devices gated by 3.5-nm (red) and 2.8-nm (blue) Er_2O_3. The solid circle for 3.5-nm (red) is the best data, which is shown in Figure 1b. The hatchings and solid line are used as eye guide. (c) Two hydration pathways for the reduction of dielectric constant; one is water penetration through the passivation layer from the ambient air, the other is exposure to DIW during photolithography process. (d) XPS spectra of O1s for 5.7-nm Er_2O_3 film on SiO_2/Si substrates.

Two potential hydration pathways contributing to the degradation of Er_2O_3 during device

fabrication and subsequent photoresist passivation are considered here, as illustrated in **Figure 2c**. Pathway 1 involves the penetration of air or water through the photoresist passivation layer after device fabrication, while Pathway 2 pertains to direct exposure to water during the photolithography process for top-gate metal formation, wherein the NMD-3 developer comprises approximately 97% water. To investigate the hydration effects on Er_2O_3 top-gate films, 5.7-nm-thick Er_2O_3 films deposited on SiO_2/Si substrates were deliberately immersed in the developer for 20 seconds and in deionized water (DIW) for 30 seconds, simulating the photolithography process. Subsequently, the chemical composition of Er_2O_3 was analyzed using X-ray photoelectron spectroscopy (XPS). In the O1s spectra presented in **Figure 2d**, peaks at approximately 531 eV and 528 eV correspond to oxidation products of Er_2O_3 and Er–OH bonds, respectively.[50,51] However, the hydroxide of $Er(OH)_3$, typically observed around 533 eV due to surface hydration,[52,53] was not detected in either sample. Notably, even after storing the Er_2O_3 films on SiO_2/Si substrates in a vacuum desiccator and in ambient air for one month, the hydroxide peak at 533 eV did not appear, as shown in **Figure S4**. These findings suggest that the stability of Er_2O_3 films cannot be assessed solely through surface chemical analysis using XPS.

Next, the degradation of Er_2O_3 was systematically examined through electrical measurements utilizing metal-oxide-semiconductor capacitors (MOSCAPs) with an Au/7.2-nm Er_2O_3/SiO_2/*p*-Si structure, where the acceptor concentration in Si substrate is approximately 5×10^{15} cm^{-3}. Note that the SiO_2 thickness was reduced to 5 nm to accurately extract the dielectric constant of Er_2O_3 by minimizing the contribution of capacitance of SiO_2 (C_{SiO2}) to the total capacitance, as shown by the equivalent circuit in the inset of **Figure 3a**. To elucidate the effects of water exposure on Er_2O_3 during device fabrication, both dry and wet methodologies were employed for the formation of top gate metal in MOSCAPs, as shown in **Figure S5**. The dry method utilized a metal mask, whereas the wet method involved photolithography. *C-V*

measurements were conducted to assess the impact of water exposure on the dielectric constant of Er_2O_3. As shown in **Figure 3a**, a significant reduction in accumulation capacitance at negative V_{TG} was clearly observed when the wet process was applied, leading to a degradation of the dielectric constant from approximately 12 to 8. This observation indicates that electrical measurements have greater sensitivity to the hydration of Er_2O_3 than surface chemical analysis by XPS. Furthermore, it is confirmed that the photolithography process is a key factor contributing to the reduction in the dielectric constant of Er_2O_3, suggesting that alternative patterning processes that avoid water usage during development are highly desirable.

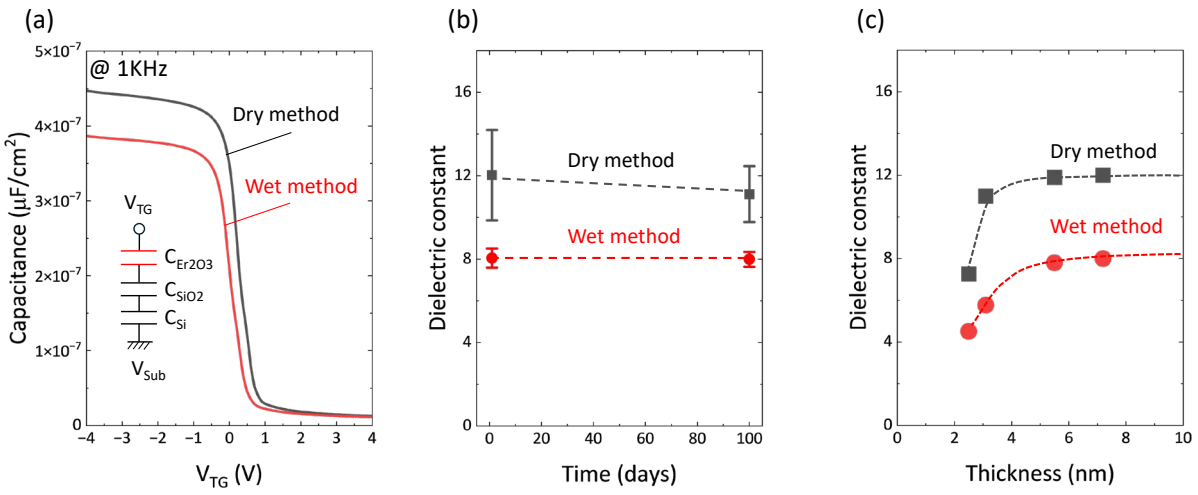


Figure 3 (a) *C-V* characteristics of 7.2-nm Er_2O_3 on 5-nm SiO_2/Si substrates under dry and wet fabrication processes. The inset shows equivalent circuit for the gate stack on Si substrates. (b) Dielectric constant of 7.2-nm Er_2O_3 on 5-nm SiO_2/Si substrates as a function of time. (c) Dielectric constant of Er_2O_3 on 5-nm SiO_2/Si substrates as the function of Er_2O_3 thickness.

To ascertain whether the long-term stability issues are predominantly attributable to hydration effects, the fabricated MOSCAPs were deliberately stored under ambient air conditions. The dielectric constant was subsequently monitored over time through *C-V* measurements. It is noteworthy that no photoresist protection was applied to the *C-V* devices for either wet or dry methodologies. While the dielectric constant of Er_2O_3 in top-gate MoS_2

FETs exhibited a degradation of nearly 50% after more than 50 days, as depicted in **Figure 2a**, **Figure 3b** clearly demonstrates minimal degradation for both wet and dry methodologies even after 100 days. This observation suggests that hydration of Er_2O_3 is not the primary cause of the long-term degradation of its dielectric constant. Furthermore, when the physical thickness of Er_2O_3 was reduced in MOSCAPs, a corresponding reduction in the dielectric constant was observed for both cases, as shown in **Figure 3c**. However, the extent of this reduction was comparable between the wet and dry methods, again indicating that hydration itself does not have a significant impact. The reduction of the dielectric constant at nanoscale thicknesses has been observed in other insulators [54–56] and could be attributed to the formation of a dead layer originating from the existence of a depolarization field[54,55] or electric field penetration into the metal electrode.[57] Therefore, this reduction in the dielectric constant of Er_2O_3 with decreasing physical thickness is suggested to be driven by intrinsic issues related to the dead layer at the metal/insulator interface. Based on the aforementioned experiments, it should be emphasized that Er_2O_3 films deposited on SiO_2/Si substrates exhibit almost no variation in physical properties and long-term stability, in contrast to Er_2O_3 films on MoS_2.

To further enhance the stability and performance of Er_2O_3 top-gate MoS_2 FETs, it is imperative to implement a water-free device fabrication process as well as appropriate passivation methods. However, as summarized in **Figure S6**, various attempts did not improve their stability and performance. The critical question now concerns the origin of the degradation of high-κ dielectrics on 2D materials, especially in contrast to their superior long-term stability on SiO_2/Si substrates. Other data on dielectric constant of 3.5-nm and 2.8-nm Er_2O_3 extracted from many devices is additionally plotted by open circles at the initial measurement day in **Figure 2a**, indicating the considerable variation. This variation was serious when the Er_2O_3 thickness was reduced from 5.3 nm. The best data shown in **Figure 1** is shown by solid red circle. It is suggested that the observed reduction in dielectric constants with decreasing

physical thickness is not attributable to intrinsic factors such as depolarization fields or electric field penetration into the metal electrode, but rather to extrinsic influences. While water-free device fabrication utilizing an electron beam (EB) lithography enhances leakage performance, it does not yield any improvement in the dielectric constant. The most plausible explanation for these extrinsic issues is that the surface condition of the 2D material plays a crucial role in determining the dielectric properties, surpassing the influence of other factors. As shown in **Figure S8**, as far as monolayer MoS_2 is transferred on SiO_2/Si substrate via mechanical exfoliation and subsequent device fabrication, its surface is not atomically smooth due to the bubble formation and not clean due to contamination such as resist residue.[58] These extrinsic issues will critically affect the quality of Er_2O_3 films, that is, dielectric properties and their long-term stability. Therefore, wafer-scale 2D materials without any transfer process should be utilized to realize reliability study of high-κ gate stack on 2D materials.

To demonstrate the universality of the degradation mechanism, a high-κ stack composed of HfO_2/Er_2O_3 was integrated onto a clean, full-cover monolayer MoS_2 grown on a 2-inch sapphire substrate using the metal-organic chemical vapor deposition (MOCVD) method.[59] The superior uniformity with roughness root mean square (RMS) of ~0.16 nm for the MoS_2 surface on the sapphire substate is clearly observed in **Figure 4a** and **Figure S9**. Although the nominal thickness for the buffer-layer Er_2O_3 deposited via thermal evaporation and ALD-HfO_2 are ~1 nm and ~10 nm, respectively, the precise thickness of the HfO_2/Er_2O_3 stack was determined to be 10.7 nm via grazing incidence X-ray reflectivity (GIXR) measurements. The refractive index, which is correlated with the dielectric constant, was extracted using spectroscopic ellipsometry. To ensure accuracy, the ellipsometry data for the MoS_2/sapphire substrate were first obtained prior to the deposition of the HfO_2/Er_2O_3 stack, and this data was subsequently employed as the substrate reference for fitting the structural model for the $HfO_2/Er_2O_3/MoS_2$/sapphire system (**Figure S10**). Controlled experiments were conducted with two configurations: the HfO_2/Er_2O_3

stack on a bare sapphire substrate and the HfO_2/Er_2O_3 stack on a $MoS_2/SiO_2/Si$ substrate, where monolayer MoS_2 was transferred from the sapphire substrate to the SiO_2/Si substrate via the conventional polymethyl methacrylate (PMMA) transfer method (RMS ~1.6 nm).[60] As shown in **Figure 4a**, the refractive index of the HfO_2/Er_2O_3 stack on the MoS_2/sapphire substrate remains nearly constant at around 1.9 across the measurement wavelength range of 800 to 1700 nm. This value agrees well with the refractive index of the HfO_2/Er_2O_3 stack on the sapphire substrate and reported values for HfO_2 on Si (111)[61] (shown as a black dotted line). In contrast, for the HfO_2/Er_2O_3 stack on the $MoS_2/SiO_2/Si$ substrate, the extracted refractive index significantly deviated from the expected values based on the analytical model. This discrepancy can be attributed to the rough surface and contaminants present on the MoS_2 film, as schematically shown in the inset of **Figure 4a**, which were introduced during the transfer process. These imperfections likely hindered the accurate analysis of the refractive index for the HfO_2/Er_2O_3 stack. Furthermore, **Figure 4b** shows the density of the HfO_2/Er_2O_3 stack, extracted via GIXR measurements for both HfO_2/Er_2O_3 stacks on MoS_2/sapphire and sapphire substrates, demonstrating superior stability over time, even after 100 days. According to the Clausius-Mossotti relation, which correlates density with the dielectric constant, this observed stability strongly supports the assertion that the uniformity and cleanliness of the MoS_2 surface significantly influence the dielectric properties of the high-κ films. The degradation mechanism is further illustrated in **Figure S11** and supported by GIXR measurement shown in **Figure S12.**

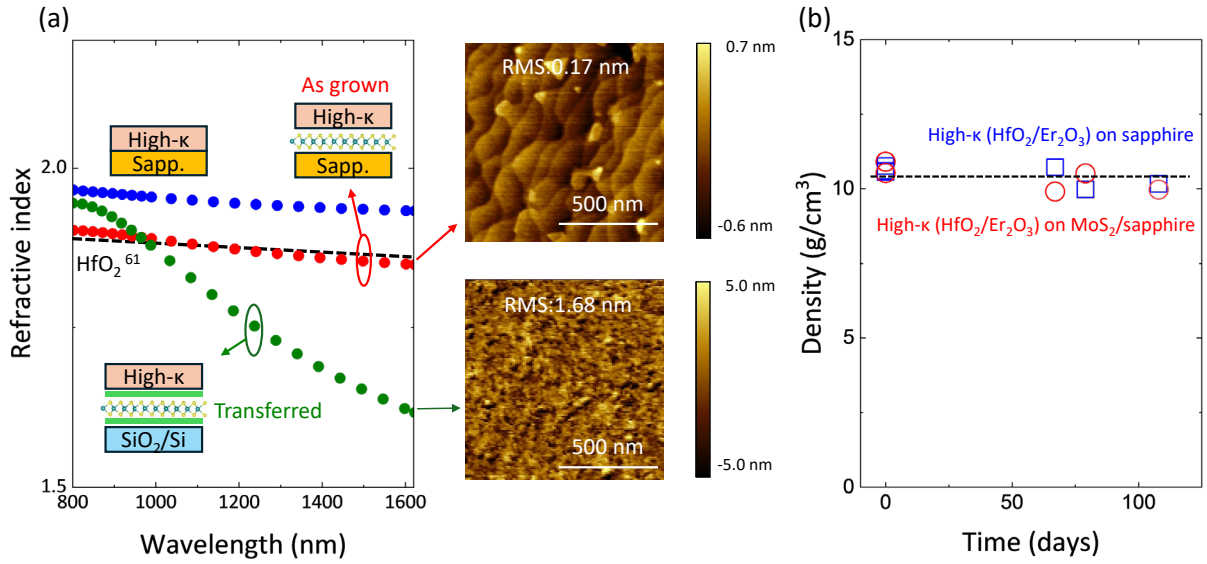


Figure 4 (a) Refractive indices of three different samples extracted using spectroscopic ellipsometry: the HfO_2/Er_2O_3 stack on a bare sapphire substrate (blue), the HfO_2/Er_2O_3 stack on a clean MoS_2 grown on a sapphire substate (red), and the HfO_2/Er_2O_3 stack on transferred $MoS_2/SiO_2/Si$ substrate (green). The dotted black line represents the reference data from HfO_2 on Si.[61] The AFM images compare the surfaces of MoS_2 grown on a sapphire substrate by MOCVD and MoS_2 transferred to the SiO_2/Si substate. (b) Density of the HfO_2/Er_2O_3 stack on MoS_2/sapphire substrate (red open circle) and on sapphire substrate (blue open rectangle) as a function of time.

Reducing the physical thickness of Er_2O_3 to 3.5 nm enabled an EOT of 0.94 nm in top-gate MoS_2 FETs, thereby achieving low operation voltages and superior leakage current characteristics. However, extensive device fabrication revealed significant variations in the dielectric constant and observed degradation over time when the Er_2O_3 thickness was reduced below 5 nm, indicating potential hydration effects. In contrast, *C-V* studies on $Er_2O_3/SiO_2/Si$ substrates demonstrated long-term stability despite the wafer-involved fabrication processes employed. Water-free fabrication techniques and the application of appropriate passivation layers did not prevent the degradation of dielectric properties, implying that the primary cause of long-term degradation in Er_2O_3 on MoS_2 may be attributed to the suboptimal surface conditions of MoS_2 transferred onto SiO_2/Si substrates. Indeed, the long-term stability was demonstrated when the high-κ film was deposited on the clean surface of MoS_2 grown on a

sapphire substrate by MOCVD. These surface conditions are crucial in determining device performance, offering valuable insights for the future development of 2D devices.

ASSOCIATED CONTENT

Supporting Information.

The Supporting Information is available free of charge on the ACS Publications website at DOI: XXX.

Experimental details including material and methods, schematics of high-κ Er_2O_3 deposition system and band alignment with MoS_2, EOT and *S.S*. extraction, LT-PL spectrum of monolayer MoS_2 before and after high-κ Er_2O_3 deposition, XPS O1s spectrum for Er_2O_3 after 1 month storage in vacuum and ambient air, illustration of MOSCAPs fabrication method, methodology to avoid the hydration of Er_2O_3, I_D-V_{TG} characteristics for Er_2O_3/MoS_2 FET passivated by different passivation layer and surface morphology of transferred MoS_2, fitting of amplitude and phase difference measured by Ellipsometry, schematic illustration of degradation mechanism and the XRR spectrum of high-κ deposition on transferred and as grown MoS_2.

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Notes

The authors declare no competing financial interests.

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Supporting Information

Reliability Challenges in Equivalent-Oxide-Thickness Scaling with High-κ Er_2O_3 Dielectrics on two-dimensional MoS_2 Field-Effect Transistors

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MATERIALS AND METHODS

Device fabrication. Monolayer MoS_2 were transferred to a 90-nm SiO_2/n^+-Si substrate through the mechanical exfoliation technique using a polydimethylsiloxane (PDMS) sheet. A 1-nm Ni/40 nm Au electrodes were deposited in ultra-high vacuum condition (10^{-8} Pa) utilizing electron beam evaporation for Ni and a K-cell for Au. The MoS_2 channel geometry was defined via CF_4 plasma etching. A 3.5-nm Er_2O_3 layer was deposited on top of the MoS_2 channel at a partial oxygen pressure (P_{O2}) of 10^{-2} Pa, with the erbium metal heated to 1140°C at 10^{-5} Pa within a differential-pressure type chamber, as shown in **Supplementary Figure S1a**, achieving a deposition rate of approximately 3 pm/s. Subsequently, a 40-nm Au film was deposited as the top gate metal. To mitigate degradation from atmospheric exposure, three different passivation layers were employed: First is 1.3 μm-thick photoresist (Merck AZ1500(20 cP)), spin-coated onto the device. Second is *h*-BN, transferred onto the channel region of the top-gated devices using a dry transfer method with PDMS and an alignment system. Third is 1-μm-thick Parylene-C, deposited at 0.1 Torr at room temperature using a customized deposition system. Alternatively, the HfO_2 was deposited in a hot wall ALD chamber[1,2] at 200°C with Tetrakis (ethylmethylamido) hafnium (TEMAHf), H_2O, and N_2 as the precursor, oxidant, and purge gas, respectively. The pulse time for TEMAHf/H_2O is 0.5 s/0.1 s, respectively.

Characterization. The XPS analysis was performed using the JPS-9010MC (JEOL) system. Raman spectroscopy was performed with a Horiba LabRAM HR-800 system equipped with a 488 nm excitation laser. To determine the thickness of Er_2O_3 on SiO_2/Si substrates, GIXR measurements were carried out using Cu Kα radiation at 9kW with a Rigaku SmartLab. AFM measurements were conducted with a 42 N/m Si cantilever on an Asylum Research Cypher HV at room temperature. Ellipsometry measurements were conducted using a rotating compensator ellipsometer M-2000U (Woollam) with incident angles of 50°, 60°, and 70°, measured simultaneously. TEM images were acquired at an acceleration voltage of 200 kV using a JEM-ARM200F to confirm the quality of the interfaces of MoS_2/Er_2O_3 and Er_2O_3/Au and the crystallinity of Er_2O_3. *I–V* and *C–V* measurements were conducted in a vacuum prober at room temperature using Keysight B1500 and 4980A LCR meters, respectively.

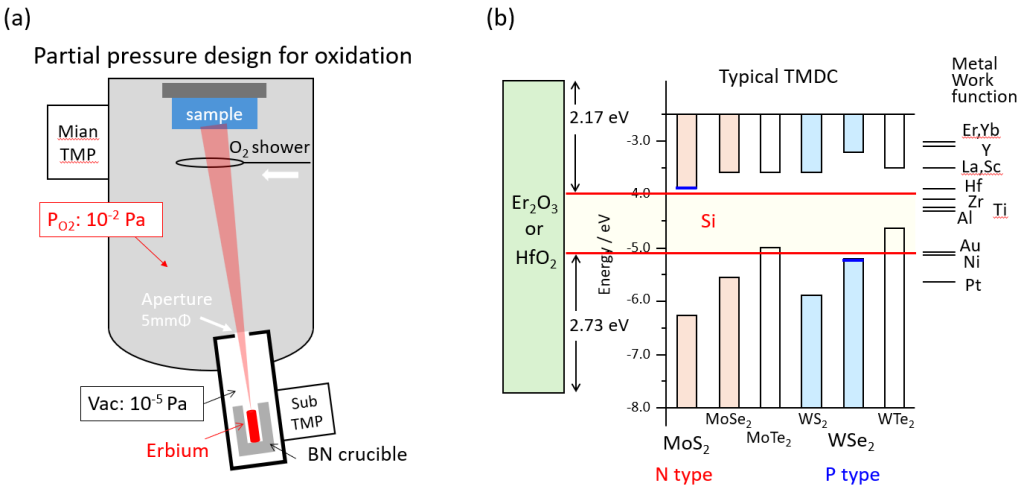

Figure S1 (a) Differential-pressure type chamber customized for Er_2O_3 deposition. (b) Band alignment of HfO_2 to Si and typical TMDC semiconductors.

Note: The chambers were initially maintained in an ultrahigh vacuum of 5×10^{-8} Pa or less. Then, oxygen was introduced only in the main chamber, and the oxygen partial pressure (P_{O2}) was kept at $P_{O2} = 10^{-2}$ Pa, while the vacuum level in the sub chamber for Er can be maintained at a high vacuum level of 10^{-5} Pa. Finally, the Er metal in the sub-chamber was heated to 1140°C for Er_2O_3 deposition. More detailed information, please see our previous publication.[3]

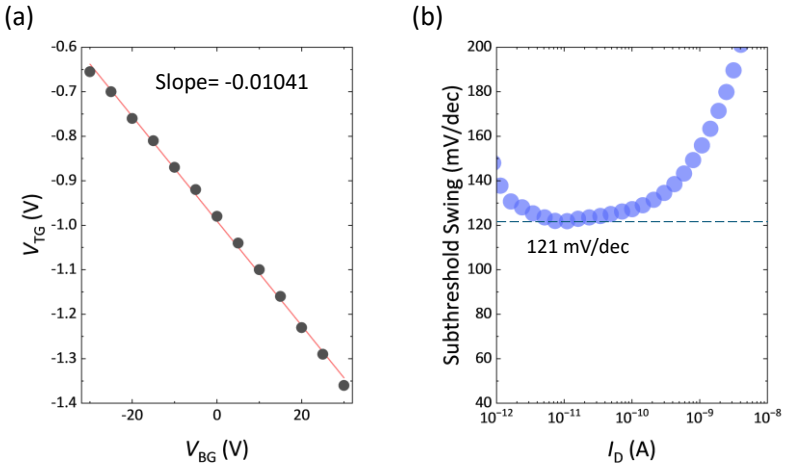

Figure S2 (a) V_{th} for the V_{TG} sweep as a function of the V_{BG} extracted from **Figure 1b**. Based on the capacitive coupling of V_{TG} and V_{BG} through $V_{TG}/V_{BG} = -C_{BG}/C_{TG}$, C_{TG} was determined as 3.68 μm/cm^2 because of $C_{BG} = 0.038$ μFcm^{-2} for a 90 nm thickness of SiO_2. (b) Subthreshold swing of 3.5-nm Er_2O_3/MoS_2 dual gate FET with EOT = 0.94 nm at $V_{BG} = 0$ V.

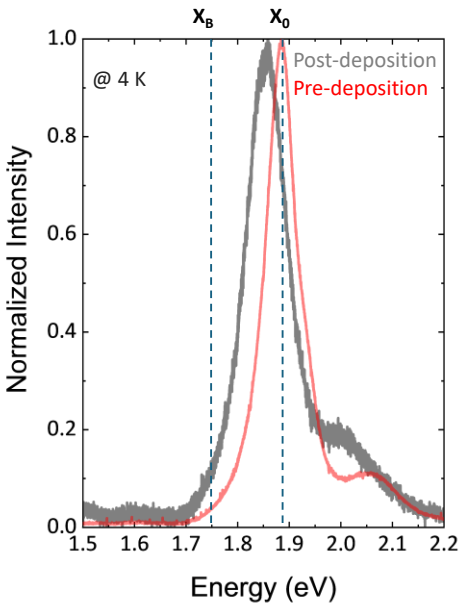

Figure S3 Low-temperature PL spectra of pre- and post-deposition of 2-nm Er_2O_3 on monolayer MoS_2. The measurement temperature was 4 K. Recent studies have indicated that defect-bound excitons can serve as reliable indicators of defect levels, particularly those associated with sulfur vacancies.[4–7]The intensity of the exciton peak may vary with gate voltage, as the exciton, rather than the trion, appears to be bound to the defect. Nevertheless, low-temperature PL remains a valuable tool even in the absence of an applied bias, as the exciton can still be observed. By comparing the low-temperature PL spectra of monolayer MoS_2 before and after high-κ deposition, no significant increase in the defect peak around 1.75 eV was observed, suggesting that the deposition process does not adversely affect the intrinsic properties of MoS_2.

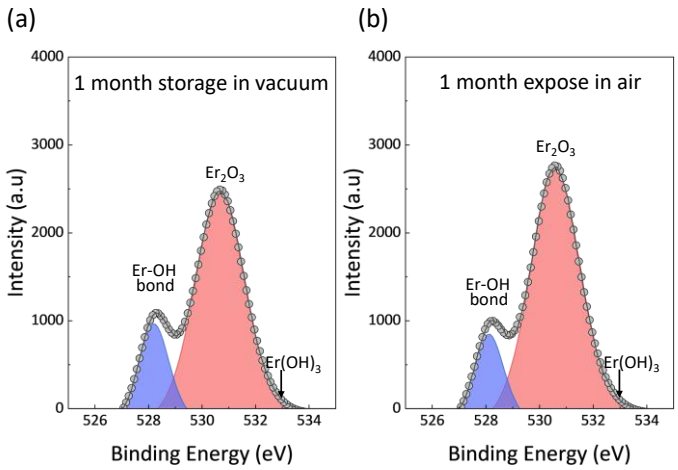

Figure S4 XPS O1s spectra of 5.7-nm Er_2O_3 deposited on SiO_2/Si substrates measured after one month storage (a) in vacuum, (b) in ambient air.

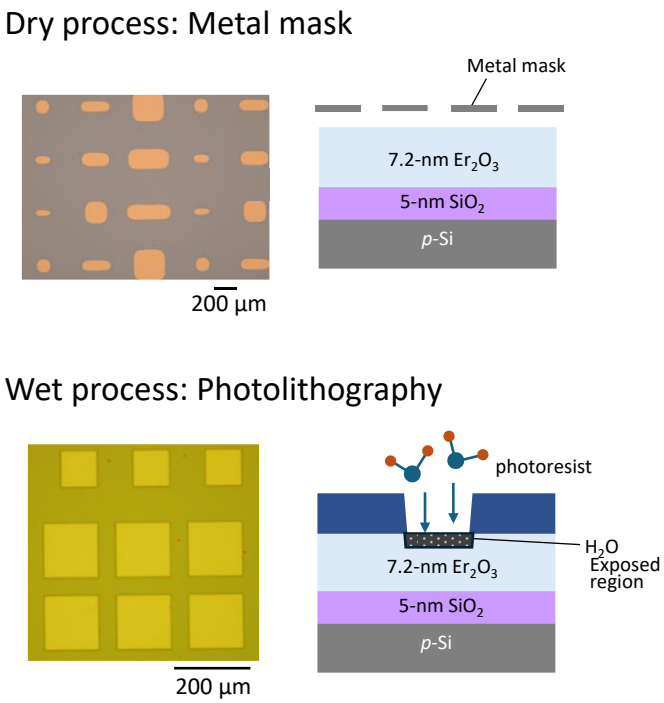

Figure S5 Illustration of dry and wet processes for MOSCAP fabrication.

(a)

Film	Cytop	PMMA	Parylene-C	*h*-BN
formation method	Spin-coating	Spin-coating	PVD	transferred
Formation temperature(°C)	200°C	110°C	RT	RT
Water vapor transmission rate (g·m/m²·day)	3×10^{-4}	5.6×10^{-2}	8×10^{-5}	1.8×10^{-10}

(b)

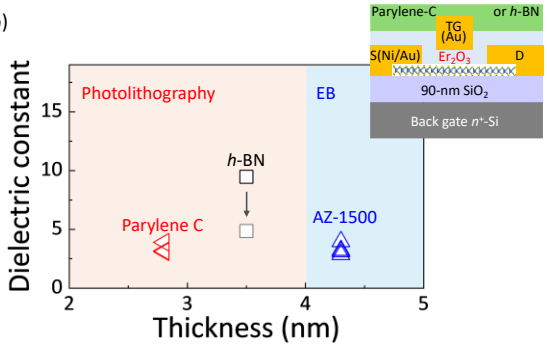

Figure S6 (a) Methodology to avoid the hydration of Er_2O_3. Table summarized the water vapor transmission rate for several passivation materials.[8] (b) Dielectric constant o Er_2O_3 on MoS_2 passivated by *h*-BN, Parylene-C and fabricated by EB lithography. The inset shows schematic illustration of device structure with passivation.

Note: In this study, to effectively prevent water transmission into Er_2O_3, the *h*-BN as well as the parylene-C was utilized as the passivation layer, as schematically shown in the inset of **Figure S6b**, since their water vapor transmission rates are three orders of magnitude lower than that of conventional resist material such as polymethyl methacrylate (PMMA). On the other hand, to avoid hydration during the photolithography process, electron beam (EB) lithography was applied, employing a water-free developer composed of pentyl acetate and methyl isobutyl ketone (MIBK) and isopropyl alcohol (IPA). **Figure S6b** summarizes the dielectric constants extracted from devices employing different passivation layers and fabrication methods, showing that dielectric constants are still low and are independent of the passivation method. The degradation was found for *h*-BN passivated device, while other Parylene-C passivated and EB fabricated devices exhibited no further degradation over time due to exceptionally low initial values (Not shown here). Detailed results are shown in the Supporting Information of **Figure S7**.

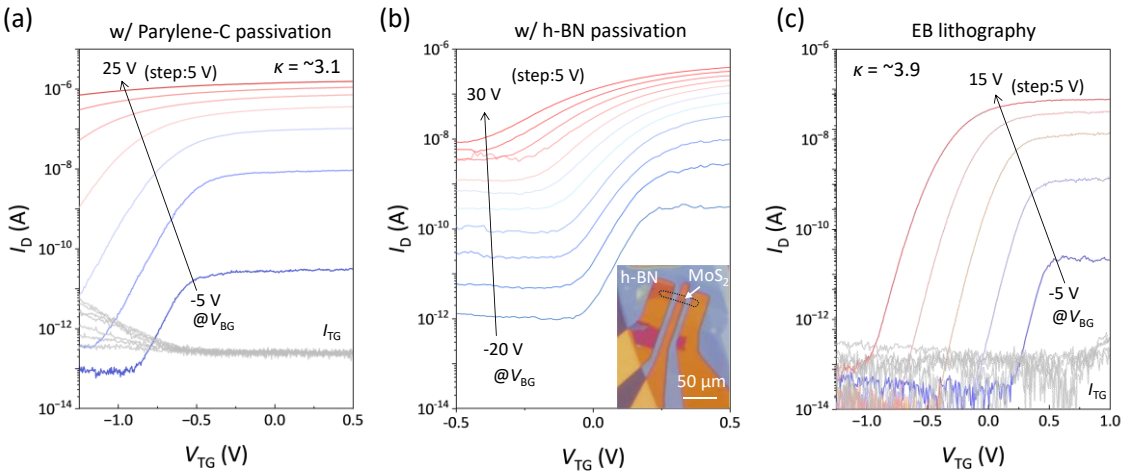

Figure S7 Examples of the devices characterized in **Figure S6b** include: (a) a Parylene-C-passivated 2.8-nm Er_2O_3/MoS_2 dual-gate FET, (b) an *h*-BN-passivated 3.5-nm Er_2O_3/MoS_2 dual-gate FET, and (c) a 4.3-nm Er_2O_3/MoS_2 dual-gate FET fabricated via EB lithography.

Note: In case of the parylene-C passivated MoS_2 FET with 2.8-nm top gate Er_2O_3, as shown in **Figure S7a**, the dielectric constant was found to be extremely low, at approximately 3.1. Therefore, even after the prolonged stored duration, the degradation was not observable. Moreover, the *h*-BN-passivated MoS_2 FET with 3.5 nm top gate Er_2O_3, as shown in **Figure S7b**, shows that the dielectric constant of Er_2O_3 degraded from approximately 9.47 to 4.86 after approximately 100 days of storage in vacuum, following a trend similar to that in **Figure 2a**. On the other hand, MoS_2 FET gated with 4.3 nm Er_2O_3 was fabricated using EB lithography, as shown in Supporting Information of **Figure S7c**. the dielectric constant was found to be extremely low, at approximately 3.9, immediately after fabrication. No degradation of dielectric constant was observed for devices fabricated by EB lithography method.

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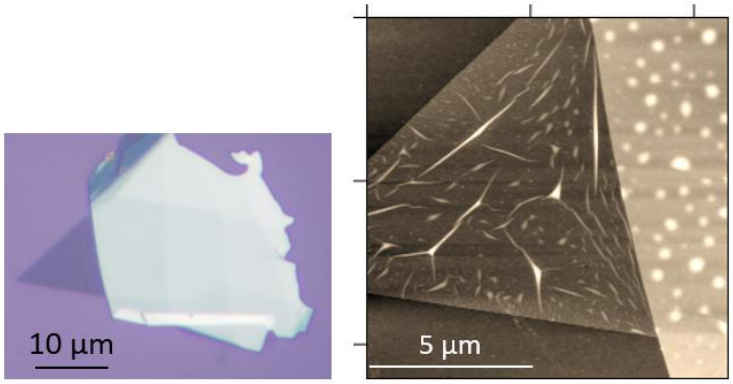

Figure S8 AFM image of mechanically exfoliated monolayer MoS_2 transferred onto SiO_2/Si substrate using PDMS.

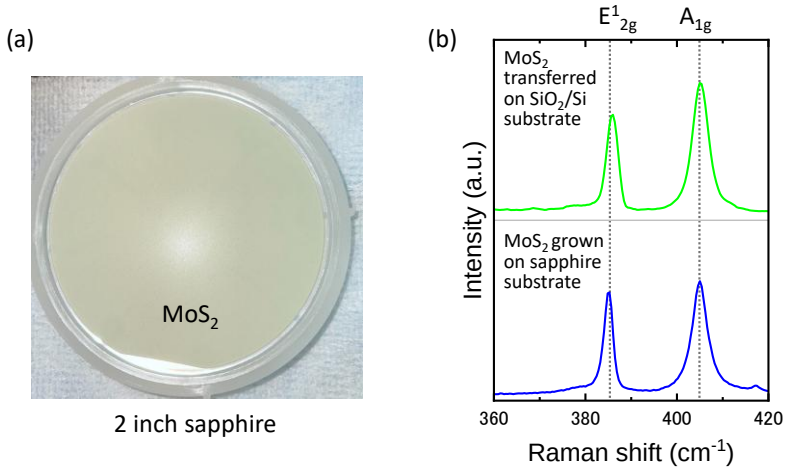

Figure S9 (a) Photograph of wafer-scale monolayer MoS_2 grown on a 2-inch sapphire substrate. The monolayer MoS_2 was grown on a 2-inch sapphire substrate via MOCVD, utilizing MoO_2Cl_2 and H_2S as precursors in an N_2 carrier gas.[9] The growth temperature was 950°C, and the growth time was 1 hour. (b) Raman data for MoS_2 grown on a sapphire substrate and MoS_2 transferred onto a SiO_2/Si substrate. No significant difference is observed between the two samples.

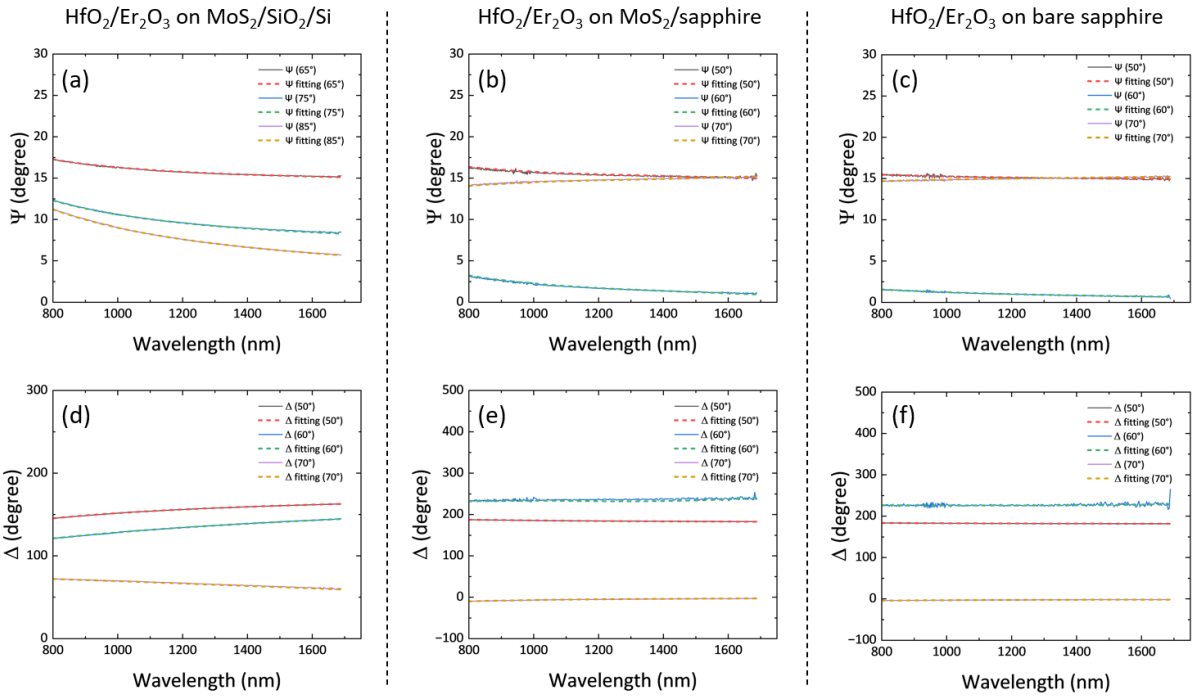

Figure S10 Ellipsometry parameters, amplitude ratio Ψ and phase difference Δ as a function of incident wavelength for three different samples. The solid and dotted lines represent the measured data and fitting curves, respectively. (a,d) HfO_2/Er_2O_3 stack on the $MoS_2/SiO_2/Si$ substrate, (b,e) HfO_2/Er_2O_3 stack on the MoS_2/sapphire substrate, (c,f) and HfO_2/Er_2O_3 stack on the sapphire substrate. The nominal thicknesses for HfO_2 and Er_2O_3 are 10 nm and 1 nm, respectively, while the actual thicknesses of the three HfO_2/Er_2O_3 stacks, determined by GIXR measurements, are 12.9 nm, 10.7 nm, and 10.45 nm in order. Ellipsometry was performed at three different incident angles: 50°, 60°, and 70°, for each sample. Using these three data sets, the refractive index (n), shown in **Figure 5a**, was calculated by fitting the data, based on Cauchy's dispersion equation: $n(\lambda) = A + B/\lambda^2 + C/\lambda^3$, where A, B, and C are fitting parameters. As clearly seen, all the fitting curves in **Figure S8(a~f)** agree well with the experimental data, confirming that the calculation of $n(\lambda)$ in **Figure 5a** was performed accurately.

Nevertheless, $n(\lambda)$ for the HfO_2/Er_2O_3 stack on the $MoS_2/SiO_2/Si$ substrate, as shown in **Figure 5a**, significantly deviated from the expected values based on the analytical model. This discrepancy can be attributed to the rough surface and contaminants present on the MoS_2 film, as schematically shown in the inset of **Figure 5a**, which were introduced during the transfer process. The presence of these contaminants is further supported by the fact that the thickness (12.9 nm) of the HfO_2/Er_2O_3 stack was much greater than the nominal thickness (11 nm). These imperfections likely hindered the accurate analysis of the refractive index for the HfO_2/Er_2O_3 stack on the $MoS_2/SiO_2/Si$ substrate.

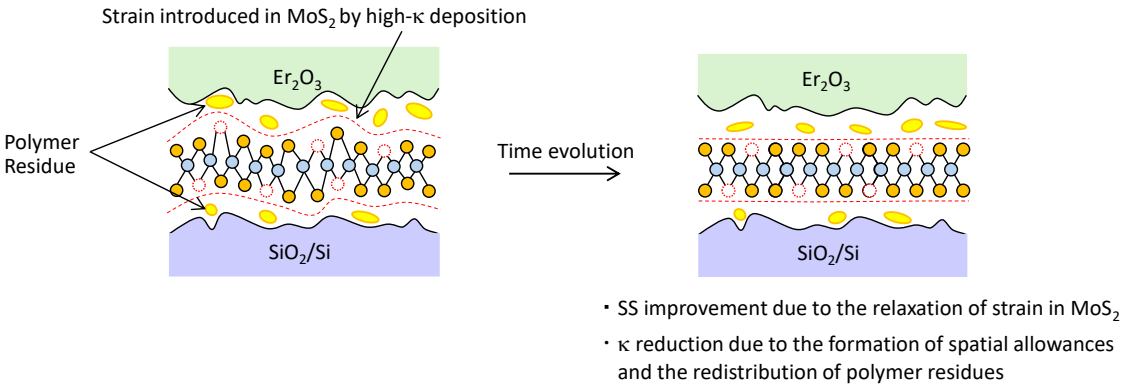

Figure S11 Schematic illustration of instability mechanism of Er_2O_3/MoS_2 system caused by the mechanical transfer process.

Note: The polymer residues work as a low-κ layer and are distributed heterogeneously across different flakes, thereby inducing substantial variations in device performance. In this context, mechanical strain is introduced into MoS_2 through high-κ deposition and the formation of bubbles during the mechanical transfer process. Notably, the subthreshold swing value improved over time, indicating that the strain was progressively alleviated. Conversely, the dielectric constant decreased over time. These observations imply that a "spatial allowance" was formed as shown in the following figure, facilitated by the redistribution of low-κ polymer residues during the relaxation of mechanical strain, which contributed to the observed reduction of the dielectric constant. Ultimately, an equilibrium state is attained as a result of the interplay between the release of mechanical strain and the redistribution of polymer residues.

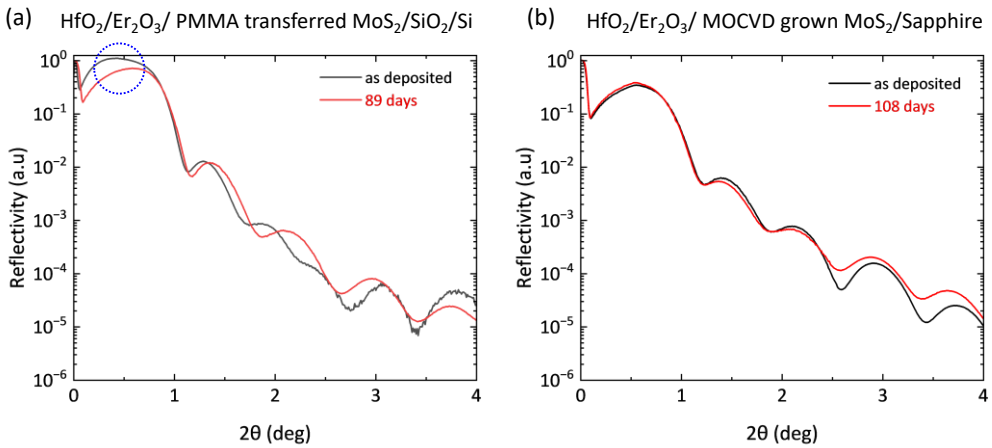

Figure S12 X-ray reflectivity spectrum of 10-nm HfO_2/2-nm Er_2O_3 on (a) PMMA transferred MoS_2 on SiO_2/Si substrate, (b) as grown MOCVD MoS_2 on sapphire substrate. Black line represents sample measured just after ALD-HfO_2 deposition; red line represents aged sample measured after long time aging in vacuum storage.

Note: To investigate whether this is a universal property of high-κ/2D systems, we deposited a 10-nm ALD-HfO_2 layer, buffered by a 2-nm Er_2O_3 layer, on MoS_2 that had been transferred onto a SiO_2/Si substrate from a sapphire substrate using PMMA as a transfer medium. For comparison, an identical gate stack was deposited on as-grown MoS_2 on sapphire substrate. As shown in **Figure S12a**, the GIRX spectra compare the sample measured immediately after deposition (black line) and after being stored in vacuum for 89 days (red line). The reflectivity at the initial small angle exhibits variations, as highlighted by the dotted blue circle, likely due to alterations in the surface roughness of high-κ film. Moreover, the reflectivity between 1.5° and 2.5° clearly exhibits changes in periodicity over time. After 89 days of aging, the XRR spectrum becomes more periodic, suggesting a significant modification in the spatial redistribution of undesired contaminants between the high-κ film and MoS_2, along with the relaxation of strain in MoS_2. In contrast, the GIXR spectra for high-κ stacked on uniform MoS_2 grown on sapphire substrates (**Figure S12b**) show exceptional reproducibility, demonstrating the stability of the interface. These findings imply that the instability observed may be a issue affecting a wide range of high-κ/2D systems, unless the uniformity of the 2D material is carefully ensured.

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