Journal of Applied Physics

RESEARCH ARTICLE | OCTOBER 30 2019

Materials issues and devices of α- and β-Ga_2O_3

Elaheh Ahmadi ; Yuichi Oshima

J. Appl. Phys. 126, 160901 (2019)
https://doi.org/10.1063/1.5123213

Journal of Applied Physics PERSPECTIVE scitation.org/journal/jap

Materials issues and devices of α- and β-Ga_2O_3

Cite as: J. Appl. Phys. **126**, 160901 (2019); doi: 10.1063/1.5123213
Submitted: 7 August 2019 · Accepted: 3 October 2019 ·
Published Online: 30 October 2019

View Online Export Citation CrossMark

Elaheh Ahmadi[1,a)] and Yuichi Oshima[2]

AFFILIATIONS

[1]Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan 48109, USA
[2]Optical Single Crystals Group, National Institute for Materials Science, Tsukuba, Ibaraki 3050044, Japan

[a)]**Email:** eahmadi@umich.edu

ABSTRACT

Ga_2O_3 is an ultrawide bandgap semiconductor with a bandgap energy of 4.5–5.3 eV (depending on its crystal structure), which is much greater than those of conventional wide bandgap semiconductors such as SiC and GaN (3.3 eV and 3.4 eV, respectively). Therefore, Ga_2O_3 is promising for future power device applications, and further high-performance is expected compared to those of SiC or GaN power devices, which are currently in the development stage for commercial use. Ga_2O_3 crystallizes into various structures. Among them, promising results have already been reported for the most stable β-Ga_2O_3, and for α-Ga_2O_3, which has the largest bandgap energy of 5.3 eV. In this article, we overview state-of-the-art technologies of β-Ga_2O_3 and α-Ga_2O_3 for future power device applications. We will give a perspective on the advantages and disadvantages of these two phases in the context of comparing the two most promising polymorphs, concerning material properties, bulk crystal growth, epitaxial growth, device fabrication, and resulting device performance.

I. INTRODUCTION

Semiconductor power devices are now widely used for virtually every single electric power conversion device and, therefore, improving the efficiency of the power devices is of crucial importance for global energy savings. About 13% of generated electricity today is wasted through switching and conversion. Today's commercial high-power semiconductor devices are dominantly Si-based. However, in the past few decades, gallium nitride (GaN) and silicon carbide (SiC) have emerged as desirable candidates to replace Si in high power applications for high-frequency operation, efficiency enhancement, compactness, and weight reduction. These materials are characterized by a bandgap of approximately 3.3 eV, significantly wider than silicon's bandgap of 1.12 eV, allowing the use of high electric fields and thus high voltages with low associated losses. In the case of SiC power devices, for example, it is estimated that 300×10^6 barrels of crude oil can be saved, and 83×10^6 tons of CO_2 gas emission can be suppressed per year by 2050.[1] The power device related market is expected to reach $22 billion by 2024,[2] which would be a great benefit to the semiconductor industry. Servicing the electrification of the automobile is already one of the fastest growing segments of the electronics industry. Nonetheless, producing large scale, cost-effective, and high quality GaN and (to a lesser extent) SiC substrates remains the major challenge in the development roadmap of power electronics based on these wide bandgap materials.

There is an urgent need for new semiconductor devices to be operated in the multiple kilovolts range for power electronics applications in many advanced systems, including distributed grid systems, electric vehicles, high-speed trains, and industrial automation. Due to the limited availability of semiconductor switches of ≥10 kV, transformers are currently used to step down high voltages (HVs), which will be switched and then stepped back up to the desired HV. Recently, ultrawide bandgap (UWB) semiconductors including Ga_2O_3, diamond, high Al content AlGaN, and AlN have drawn a great deal of interest in the research community for HV applications beyond those accessible with GaN and SiC. Figure 1 demonstrates the material properties of these semiconductors along with those for GaN and 4H-SiC.

Considering only the material properties, diamond is the most promising semiconductor for future high-power applications due to its wide bandgap, high thermal conductivity, and high electron and hole mobility. However, it possesses a number of serious challenges which need to be addressed before diamond can be considered for any practical application. These challenges include unavailability of large-scale and dislocation free diamond substrates in addition to

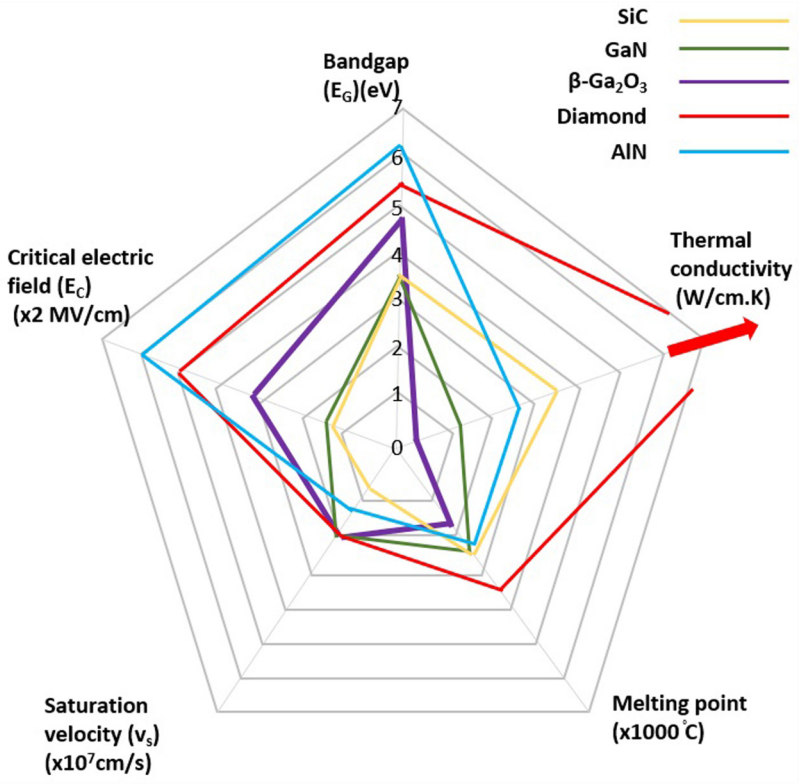

FIG. 1. Diagram comparing material properties of wide bandgap semiconductors. Note that the melting point of GaN is obtained from molecular dynamics simulations[138] and SiC is actually the decomposition temperature.

high ionization energies of *n*-type (570 meV for phosphorous) and *p*-type (380 meV for boron) dopants in diamond.

High Al-content AlGaN channel MESFETs on AlN substrates or templates have been proposed for high power applications. However, this material system suffers from low electron mobilities due to alloy scattering and low thermal conductivity, in addition to challenges with producing large-scale AlN substrates. AlN-on-sapphire templates are commercially available. However, similar to GaN-on-sapphire templates, they suffer from high threading dislocation density which makes them unsuitable for AlN-based vertical devices.

Ga_2O_3, the target material of this article, is an ultrawide bandgap semiconductor with a bandgap energy of 4.5–5.3 eV (depending on its crystal structure), which is much greater than those of conventional wide bandgap semiconductors such as SiC and GaN (3.3 eV and 3.4 eV, respectively). Therefore, Ga_2O_3 is promising for future power device applications, and further high-performance is expected compared to those of SiC or GaN power devices, which are currently in the development stage for commercial use. Ga_2O_3 crystallizes into various structures. Among them, promising results have already been reported for the most stable β-Ga_2O_3 and for α-Ga_2O_3, which has the largest bandgap energy of 5.3 eV (The material properties of these two different phases are listed in Table I). In this article, we overview state-of-the-art technologies of β-Ga_2O_3 and α-Ga_2O_3 for future power device applications. We will give a perspective on advantages and disadvantages of these two phases in the context of comparing the two most promising polymorphs, concerning material properties, bulk crystal growth, epitaxial growth, device fabrication, and resulting device performance.

II. BULK CRYSTAL GROWTH

Availability of high-quality native substrates is a critical factor to grow high-quality epilayers, which are essential to realize high-performance semiconductor devices. Most of the wide bandgap semiconductor crystals, such as GaN, SiC, diamond, etc., cannot be grown from the melt and, therefore, they were only heteroepitaxially grown on largely lattice-mismatched foreign substrates at the early stage of development in contrast to the conventional semiconductors such as Si and GaAs. However, the realization of bulk substrates by a vapor phase growth technique has enabled the growth of high-quality homoepitaxial layers and paved the way to the commercialization of GaN and SiC devices.[3–5] Needless to say, the importance of substrates also applies for Ga_2O_3 to fully exploit the superior potential. In this section, we overview the current status and technical issues of substrates used to grow Ga_2O_3 epilayers.

A. β-Ga_2O_3 substrates

Fortunately, as oppose to other wide bandgap semiconductors, β-Ga_2O_3 bulk crystals can be grown from the melt and high-quality single crystal substrates are commercially available. This feature, in addition to the large bandgap, makes β-Ga_2O_3 a very attractive candidate for power device applications. However, it was not easy to

TABLE I. A comparison between the material properties and technological maturity of β- and α-Ga_2O_3.

	β	α
Crystal structure	Monoclinic(β-gallia)	Corundum
E_g	4.8 eV	5.3 eV
Electron mobility (est.)	200 cm^2/V s	200 cm^2/V s
E_{br} (est.)	6.5 MV/cm	9.5 MV/cm
ε	10	10 (est.)
BFOM	1231	3844
Thermal conductivity	0.27 W/cm K [010] 0.11 W/cm K [100]	No report
Substrate	β-Ga_2O_3 (melt-grown) Available ∼ ϕ2 in., R&D ∼ ϕ6 in. Currently expensive	Sapphire Available ∼ ϕ6 in. cheap
Epitaxial growth technique	MBE, HVPE, MOCVD, Mist-CVD, PLD, etc.	Mist-CVD, HVPE, MOCVD
Dislocation density	$<10^3$ cm^{-2}	Typical: 10^{10} cm^{-2} ELO: $<5\times10^6$ cm^{-2}
Surface roughness of epilayers	Macro step, need CMP	Smooth under SEM
$(Al_xGa_{1-x})_2O_3$	$x<18\%$	No limitation
n-type doping	Si, Ge, Sn	Si, Ge, Sn
p-type doping	N (deep acceptor 1 eV)	No report
Hetero-pn-junction	NiO (FCC crystal structure)	α-Ir_2O_3, α-Rh_2O_3
SI	Fe	No report

produce twin-free β-Ga_2O_3 wafers with a diameter large enough for practical use because of the strong cleavage nature, and such β-Ga_2O_3 wafers have been realized only recently.[6] In this part, we overview the features, present status, and technical issues of the representative melt growth techniques of bulk β-Ga_2O_3 crystals.

1. EFG method

At present, edge-defined film fed growth (EFG) is the most successful bulk growth technique of β-Ga_2O_3. Currently, (010) wafers up to 25×25 mm^2, ($\bar{2}$01) wafers up to 2 in., and (001) wafers up to 4 in., both Sn-doped *n*-type conductive and Fe-doped semi-insulating, are commercially available from Novel Crystal Technologies, Inc.

In the EFG method, a board-shaped β-Ga_2O_3 crystal is grown on top of an iridium dye with narrow slits, through which the Ga_2O_3 melt is supplied by capillarity [Fig. 2(a)].[7,8] The melt area can be much smaller than that of other melt growth techniques, and, therefore, it is possible to minimize the dissociation and evaporation of the melt. The crystal shape is controlled by the shape of the dye. The growth atmosphere needs to be controlled appropriately ($N_2/O_2=98\%/2\%$ for example) to minimize the iridium loss by oxidation. The growth rate is up to a few dozen cm/day. The pulling direction is usually [010] in order to suppress twinning and seed blistering. Therefore, the area of EFG-grown (010) wafers is limited to approximately 25×25 mm^2 although numerous promising results have been reported on the substrates. In contrast, β-Ga_2O_3 wafers with a principal crystal plane in the [010] zone are scalable. Indeed, 6-in. (001) wafers have been demonstrated by Novel Crystal Technologies, Inc. Note that the β-phase has a monoclinic crystal structure and, therefore, mutually orthogonal planes and directions do not have the same indices except for (010) and [010].

n-type conductivity has been controlled mainly by Sn doping.[8] Ge doping is difficult because of the high vapor pressure of GeO_2. Although N_d-N_a decreases by O_2 annealing after the growth to remove residual strain, N_d-N_a can be recovered to be virtually identical to the donor concentration by N_2 annealing.[8] The mechanism has not been clarified yet, but N_2 annealing could introduce oxygen vacancies, and it is likely that an impurity–vacancy complex consisting of a dopant element and oxygen vacancies acts as a shallow donor.

In general, dislocations in the semiconductor material can deteriorate the device performance. Experimental results suggested that dislocations in β-Ga_2O_3 can be current leakage paths.[9] Dislocation density in EFG-grown β-Ga_2O_3 has been reported to be $\sim10^3$ cm^{-2},[8] which is much lower than that in halide vapor phase epitaxy (HVPE)-grown GaN substrates. It should be examined if this dislocation density is low enough for power device applications. Note that the allowable dislocation density strongly depends on the device design and the drive conditions. In addition to dislocations, rod-shaped voids also exist in EFG-grown β-Ga_2O_3 crystals with a density of $\sim10^2$ cm^{-2}.[10] The diameter of the void is around 100 nm, and the length is 15 μm or more. These voids are believed to be formed by the evaporation of metallic impurities in the crystal. The influence of these voids on the device performance has not been clarified yet, but the inner surface of such a void could be a current leakage path.

As described above, the EFG method is very promising. However, the production cost needs to be reduced substantially in order to put EFG-grown β-Ga_2O_3 wafers into practical use. A key technology for the cost reduction should be the suppression of the iridium loss, although the realization needs a breakthrough.

2. Czhochralski method

The Czhochralski (Cz) method is one of the most representative melt-growth techniques, which is widely used for the mass production of semiconductor crystals such as Si, Ge, GaAs, etc.[11] Figure 2(b) shows the principle of the Cz method. The growth of 2-in. β-Ga_2O_3 bulk crystals has been demonstrated,[12,13] and 1-in. semi-insulating (010) β-Ga_2O_3 wafers are commercially available from Kyma Technologies and SYNOPTICS.

In the Cz method, the melt surface area is much greater than that of EFG, therefore evaporation and dissociation of the Ga_2O_3 melt are more significant. The amount of metal Ga produced by dissociation increases with increasing crucible diameter, being enough to damage the iridium crucible by forming eutectic or intermetallic GaIr phases.[14] The dissociation is suppressed by increasing the oxygen partial pressure of the growth atmosphere; however, oxidization of the iridium crucible will be further enhanced. Thus, a breakthrough is required to realize the mass production of large-diameter (4–6 in.) β-Ga_2O_3 wafers by the Cz method for power device applications.

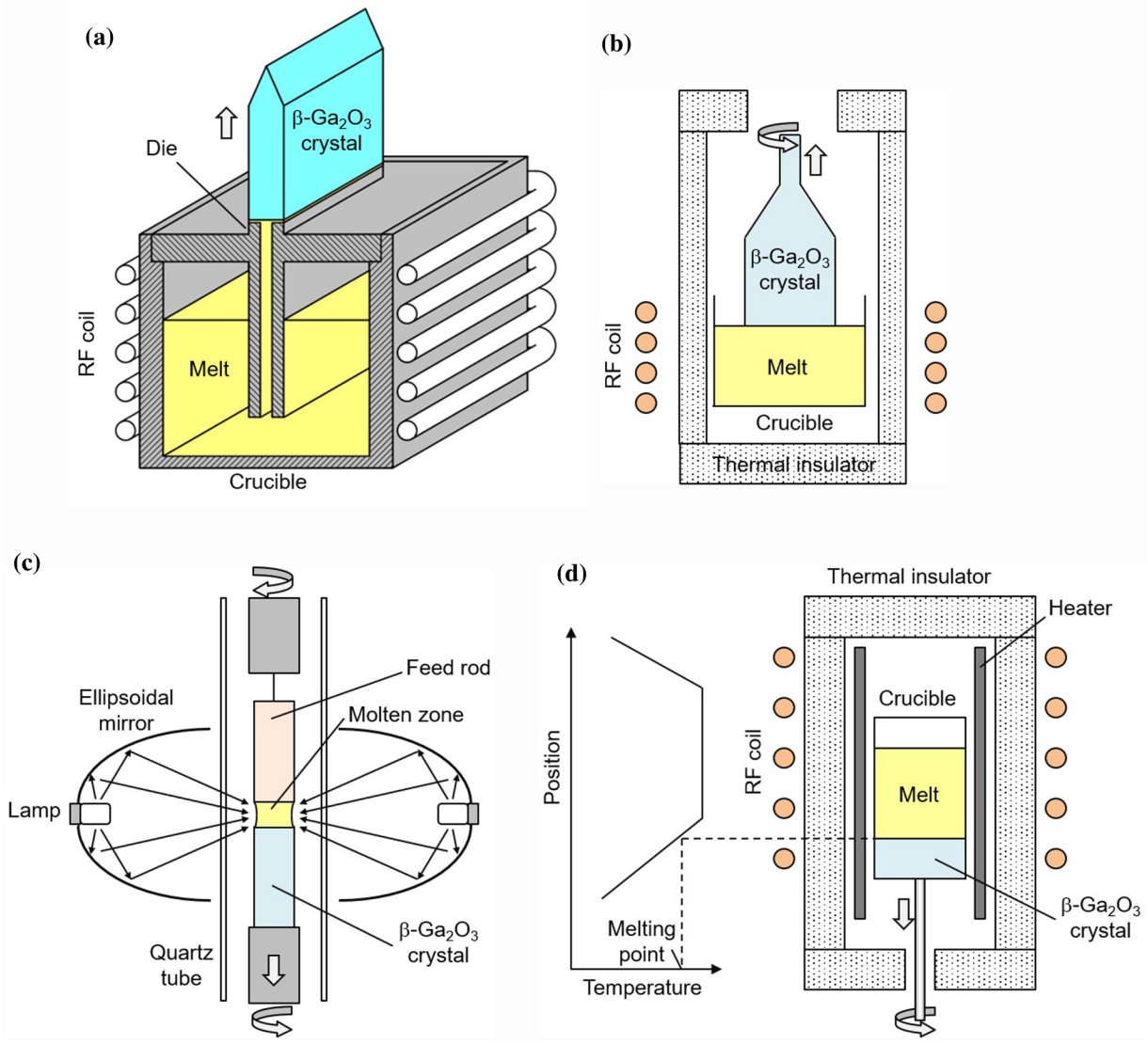

FIG. 2. Schematic of (a) EFG, (b) CZ, (c) FZ, and (d) VB melt growth techniques suitable for the growth of bulk β-Ga_2O_3.

3. Floating zone method

The first demonstration of β-Ga_2O_3 wafers with a practical diameter was carried out using the floating zone (FZ) method.[6] In the FZ method, the β-Ga_2O_3 single crystal rod is grown from the Ga_2O_3 melt supported between the polycrystalline feed rod and the grown single crystal by surface tension [Fig. 2(c)]. The FZ method does not use a crucible, and, therefore, high-purity crystals can be grown. *n*-Type conductivity is controlled by intentional Si or Sn doping.[15,16] The growth can be carried out under high oxygen partial pressure without the crucible oxidization problem. However, the large-diameter growth is difficult because of the small hot zone and high temperature gradient owing to lamp heating.

4. Vertical Bridgman method

The first application of the vertical Bridgman (VB) method to β-Ga_2O_3 was demonstrated by Hoshikawa *et al.*, and they reported the growth of 1-in. (100) β-Ga_2O_3 bulk crystals with a dislocation density as low as $10^3\,cm^{-2}$.[17] In the VB method, the β-Ga_2O_3 crystal is grown by one-way solidification of the Ga_2O_3 melt in a Pt/Rh alloy crucible slowly passing through a temperature gradient in a vertical furnace [Fig. 2(d)]. The shape of the bulk crystal follows that of the crucible. The VB method can be cost-effective because the growth is carried out in air and the crucible material is reusable. In principle, the VB method should be advantageous to grow large-scale bulk crystals since the growth is carried out in a

gentle temperature gradient. Thus, the VB method is promising for the mass production of large-diameter β-Ga_2O_3 wafers at a reasonable cost although the VB technology remains in its infancy and further development is required.

B. Substrates for α-Ga_2O_3

α-Ga_2O_3 is meta-stable at ambient pressure, and the melt growth is not possible just like SiC, GaN, diamond, etc. Accordingly, α-Ga_2O_3 films need to be grown heteroepitaxially. Currently, only sapphire has been reported as a substrate for α-Ga_2O_3. Fortunately, large-diameter sapphire wafers up to 6 in. are mass-produced mainly for nitride LEDs and commercially available at a reasonable price. However, the dislocation density of an α-Ga_2O_3 epilayer is typically as high as 10^{10} cm^{-2} because of the large lattice mismatch, if no measure is taken.[18]

As described in Sec. III B 2, the rapid growth of α-Ga_2O_3 is possible by HVPE at a growth rate over 100 μm/h.[19] It would, therefore, be possible to produce freestanding α-Ga_2O_3 wafers in a similar way of producing freestanding GaN wafers, i.e., growing a thick α-Ga_2O_3 layer by HVPE and removing the base substrate after the growth.

α-Ga_2O_3 is more stable than β-Ga_2O_3 at high pressures, and β-Ga_2O_3 turns into α-Ga_2O_3 under 20–22 GPa or higher at ambient temperature.[20] Therefore, it is expected to be possible to grow α-Ga_2O_3 crystals from the NaOH flux under 4.4 GPa at 1000 °C using β-Ga_2O_3 powder as the raw material.[21] In future, such a high-pressure flux method could be utilized to produce bulk α-Ga_2O_3 single crystals, similar to that now being used for diamond.

III. EPITAXIAL GROWTH

In order to realize high-performance Ga_2O_3 power devices, it is essential to establish epitaxial growth techniques which produce high-quality Ga_2O_3 films with controlled electrical conductivity at a reasonably high growth rate. Although most of the epitaxial growth techniques currently being investigated for Ga_2O_3 are based on those proven to be effective for other conventional semiconductors, they need to be tailor-made to fit the nature of Ga_2O_3. In this section, we overview the features, achievements, and technical issues of epitaxial growth techniques for Ga_2O_3.

A. Epitaxial growth of β-Ga_2O_3

In most cases, β-Ga_2O_3 films for power device applications are grown homoepitaxially since high-quality native substrates are available as described in Sec. II A, (010) and (001) substrates are most frequently used. On (010), relatively smooth epilayers can be grown at a rapid growth rate although the wafer size is limited. (001) wafers are scalable and the epi growth rate on (001) is reasonable, however, the surface morphology tends to be rough. Therefore, it is not easy to grow an abrupt interface and the CMP process is required prior to the device fabrication. (100) wafers should also be scalable, but the epi growth rate is extremely low and twin boundaries are easily introduced although twinning can be suppressed to some degree by using miscut substrates.[22] ($\bar{2}$01) epilayers also suffer from stacking fault. In conclusion, (010) and (001) are the realistic choices at present. In the following part, we overview the most frequently reported growth techniques for β-Ga_2O_3, i.e., molecular beam epitaxy (MBE), HVPE, and metalorganic vapor phase epitaxy (MOVPE).

1. MBE

Plasma-assisted MBE and Ozone-MBE have been reported. Higher growth rates can be achieved in ozone-MBE compared with those in plasma-assisted MBE. Nevertheless, in ozone-MBE, the growth apparatus needs to be designed so that the ozone injection nozzle is close to the substrate surface and ozone gas can reach the surface during its short lifetime. The relationship between the growth rate and crystal orientation has been studied in detail. The growth rate is the fastest on (010) and much slower on cleavage planes such as (100) and (001).[23] The growth rate is suppressed and becomes even negative under Ga-rich growth conditions because of the formation of volatile sub-oxide Ga_2O.[24,25] The negative growth (etching) can be utilized as a cleaning technique of the β-Ga_2O_3 substrate surface prior to the film growth.[26]

The β-$(Al_xGa_{1-x})_2O_3$ solid solution can also be grown, although the Al composition is limited because the stable structure of Al_2O_3 is not the β-gallia structure. The solubility limit increases with increasing growth temperature.[27] However, the Al composition is less than 20%[28] because the MBE growth temperature is usually limited to less than 700 °C to suppress the decomposition of β-Ga_2O_3 in a vacuum.

The residual carrier concentration of an Uunintentionally doped (UID) β-Ga_2O_3 epilayer is reported to be less than $\sim 7 \times 10^{15}$ cm^{-3}.[29] The primary residual donor is believed to be Si coming from an ambient environment and the quartz parts used in the plasma source. Intentional *n*-type conductivity control is possible using mainly Sn- or Ge-doping.[30] β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 modulation-doped FETs (MODFETs) have already been demonstrated,[26,31,32] and the 2DEG channel mobility has been reported to be as high as 143 cm^2/V s at RT.[32]

The biggest drawback of MBE for commercial applications is that the growth rate is very low and, therefore, not suitable for the growth of thick drift layers of vertical power devices. MBE could be still useful for lateral devices.

2. HVPE

Currently, HVPE currently gives the highest growth rate of β-Ga_2O_3 as a vapor phase growth technique and it is possible to grow over a few dozen μm/h under atmospheric pressure.[33,34] In addition, the influence of carbon impurity can be minimized upon n^- doping control since carbon-free precursors are used. Thus, HVPE is promising for growing thick drift layers with high productivity. At present, (001) β-Ga_2O_3 homoepitaxial wafers with an n^- layer are commercially available from Novel Crystal Technologies.

Figure 3(a) shows the principle of HVPE. $GaCl_x$ is used as the Ga precursor in the HVPE of β-Ga_2O_3. $CaCl_x$ is produced by the chemical reaction between metal Ga and HCl gas upstream in the reactor. O_2 is used as the oxygen precursor in many cases while H_2O was also reported.[35] In any case, the equilibrium constant of the chemical reaction to produce Ga_2O_3 is much greater than that of GaN-HVPE. Therefore, special attention should be paid to suppress the parasitic gas-phase reaction when the precursors are supplied at high partial pressures upon rapid growth. The homoepitaxy of β-Ga_2O_3 has been reported mainly on (001) and

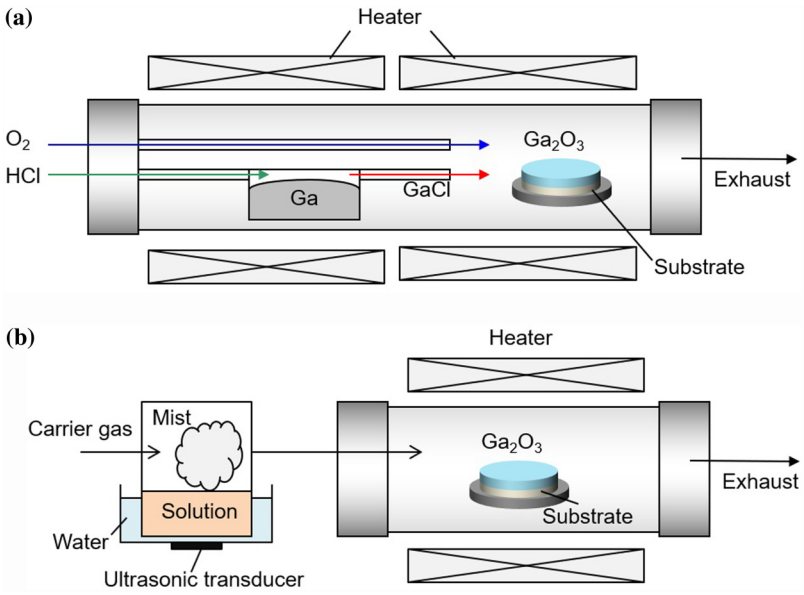

FIG. 3. Schematic of (a) HVPE and (b) mist-CVD systems used for the epitaxial growth of α- and β-Ga_2O_3.

(010).[33,35–37] On both (001) and (010), macrosteps develop strongly when a thick film is grown.[35,36]

In general, HVPE-grown crystals tend to have relatively high incorporation of Si impurity from the quartz reactor because Si-included gas is released when hydrogen-included gas is in contact with quartz at high temperatures. On the other hand, the residual Si concentration needs to be low enough for precise conductivity control. In order to remove hydrogen-included gas from the system, it is effective to use Cl_2 gas instead of HCl gas for $GaCl_x$ synthesis and to use O_2 gas rather than H_2O as the oxygen precursor. As a result, the residual carrier concentration can be suppressed to less than 10^{13} cm^{-3}.[36] Other than Si, Cl impurity is also detected at a concentration of ~10^{16} cm^{-3}.[35] Experimentally, Cl has been reported to be electrically inactive in β-Ga_2O_3,[36] although Cl is predicted to be a shallow donor.[38] However, careful investigation should be continued to check whether Cl could affect the electrical properties under specific conditions. Intentional Si doping has been carried out using $SiCl_4$ as a dopant source and it is possible to control the net carrier concentration in the 10^{16} cm^{-3} range.[39]

In order to mass-produce β-Ga_2O_3 epi wafers for power device applications by HVPE, it is essential to develop a large-scale multiple-wafer apparatus. A planetary reactor or a close coupled showerhead reactor should be employed to secure in-wafer/wafer-to-wafer uniformity because the growth rate decay along the gas flow direction is fast in HVPE of β-Ga_2O_3. Reducing the reactor pressure is also an effective option.

3. MOVPE

MOVPE is the most widely used epitaxial growth technique for the mass production of III-V compound semiconductor epi wafers. MOVPE of β-Ga_2O_3 has been investigated using TMGa, TEGa, and $Ga(DPM)_3$ as gallium precursors, and O_2, and H_2O as oxygen precursors. Equilibrium constants of chemical reactions to produce Ga_2O_3 by MOVPE are much greater than those of GaN, and the parasitic gas-phase reaction easily occurs especially upon rapid growth. Accordingly, the MOVPE of β-Ga_2O_3 is carried out at a reduced reactor pressure in many cases. A close coupled reactor is also effective to minimize the parasitic reaction and high growth rates up to 10 μm/h have been demonstrated.[40]

In general, MOVPE-grown epilayers tend to include carbon impurities originated from the metalorganic compound precursors. Carbon is predicted to be a shallow donor in β-Ga_2O_3,[41] and the concentration should be reduced for precise n^- control in drift layers. Promisingly, the carbon concentration in a MOVPE-grown UID β-Ga_2O_3 film was reported to be less than the detection limit of SIMS (~2×10^{16} cm^{-2}).[42] Intentional *n*-type conductivity control by Si doping is possible and carrier concentrations between 10^{15} ~ 10^{20} cm^{-3} are reported.[42–46] In a recent report, a high-purity Si-doped β-Ga_2O_3 film with a net carrier concentration of 2.5×10^{16} cm^{-3} has been demonstrated, and the bulk electron mobility was as high as 184 cm^2/V s at RT.[42] Note that the growth rate of the β-Ga_2O_3 film was relatively low, less than 1 μm/h. It should be assessed whether such high purity and large mobility can be maintained at higher growth rates.

The MOVPE growth temperature of β-Ga_2O_3 can be higher than that of MBE because the reactor pressure is much higher. The high growth temperature raises the solubility limit of β-$(Al_xGa_{1-x})_2O_3$, and the growth of β-$(Al_xGa_{1-x})_2O_3$ with $x > 40\%$ has been demonstrated at >800 °C.[43] The β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 super lattice with abrupt interfaces can also be grown.[43]

As described above, the combination of high growth rates (much higher than that possible by MBE) and the possibility of growing abrupt heterointerfaces, which is difficult by HVPE, makes MOVPE very promising for mass production of β-$(Al_xGa_{1-x})_2O_3$

epiwafers. Although the residual carrier concentration is higher than that of the HVPE-grown film at present, the bulk electron mobility is excellent. Scalability of the growth apparatus should be better than that of MBE and HVPE. MOVPE has great potential to play a leading role in the mass production of β-Ga_2O_3 epiwafers for power device applications in future.

B. Epitaxial growth of α-Ga_2O_3

As explained in Sec. II B, α-Ga_2O_3 is needed to be grown heteroepitaxially. Sapphire can be utilized as the substrate, which leads to very high dislocation densities due to the large lattice mismatch, if no measure is taken. The epitaxial growth has been reported mainly on *c*-plane substrates, but the growth on other crystal planes such as *a*, *m*, and *r* is also possible. In this section, we review the current status of mist-CVD, HVPE, MOVPE, and MBE, which are mainly reported as the growth techniques for α-Ga_2O_3.

1. Mist-CVD

In the mist-CVD technique, the aqueous solution of precursors is ultrasonically atomized and the mist is transferred together with a carrier gas onto the heated substrate surface to grow Ga_2O_3 [Fig. 3(b)].[47] The growth is usually conducted under atmospheric pressure. Gallium (III) acetyl acetonate or $GaCl_3$ is used as the Ga source, and H_2O is the primary oxygen source. HCl is sometimes added to the aqueous solution to improve the precursor solubility. Isomorphic α-Ga_2O_3 is obtained by growing at sufficiently low temperatures in the range of 500–600 °C on a sapphire substrate. The use of the $GaCl_3$ precursor enables a larger growth rate as high as 4.5 μm/h.[48]

The α-$(Al_xIn_yGa_{1-x-y})_2O_3$ solid solution can be grown by adding aluminum(III) acetyl acetonate and/or indium(III) acetyl acetonate in the aqueous solution.[49] α-$(Al_xGa_{1-x})_2O_3$ can be grown with no Al composition limitation, and wide range bandgap control (5.3–8.8 eV) has been demonstrated.[49] Although the low thermal stability of α-Ga_2O_3 (usually ~500 °C) is a drawback, alloying with α-Al_2O_3 dramatically improves the thermal stability. α-$(Al_xGa_{1-x})_2O_3$ with only $x < 1\%$ was reported to be stable up to 800 °C.[50] α-$(In_yGa_{1-y})_2O_3$ can be grown without phase separation when $y = 0\%$ –8% and $y = 67\%$ –70%.[49]

Mosaicity of α-Ga_2O_3 grown on (0001) sapphire by mist-CVD is characterized by a very narrow tilt angle and a broad twist angle. FWHMs of x-ray rocking curves of *0006* and $10\bar{1}2$ diffractions measured in symmetric and skew-symmetric geometries were 20–60 arcsec and 1000–2000 arcsec, respectively,[47,51] suggesting that the dislocations having an edge component are dominant. The plan-view TEM observation revealed that the total dislocation density is ~10^{10} cm^{-2}, which is much higher than that in a GaN film grown on the sapphire substrate (typically ~10^9 cm^{-2}). The dislocation density can be reduced to ~ 6×10^8 cm^{-2} by bending the dislocations using the interfacial strain of the α-$(Al_xGa_{1-x})_2O_3$ super lattice.[48] The epitaxal lateral overgrowth (ELO) is also effective, and the dislocation density in the laterally grown wing region was reported to be less than 1×10^7 cm^{-2}.

Impurity concentrations in mist-CVD-grown α-Ga_2O_3 were very high when the method was first applied to α-Ga_2O_3. For example, $[H] = 2 \times 10^{19}$ cm^{-3}, $[C] = 1 \times 10^{19}$ cm^{-3}, $[Si] = 9 \times 10^{18}$ cm^{-3}, etc.[51] At present, the purity has been much improved [for example, $[H] = 2 \times 10^{17}$ cm^{-3}, $[C] < D.\ L.\ (7 \times 10^{16}$ $cm^{-3})$][52] mainly by improving the precursor purity. Si concentration and residual carrier concentration have not been disclosed recently. In a mist-CVD reactor, the quartz surface is exposed to high partial pressure of H_2O which leads to Si contamination in the growth environment. Therefore, the mist-CVD-grown α-Ga_2O_3 films typically have high unintentional Si concentration, which is needed to be reduced to enable the precise control of carrier concentration.

n-type doping control is conducted by adding a dopant source such as tin(II) chloride dehydrate in aqueous solution, and the carrier concentrations in the range of 1×10^{17}–3×10^{19} cm^{-3} have been reported.[18,51,53] Carrier mobility in Sn-doped *c*- and *m*-plane films has been reported to be 24 $cm^2/V\,s$ ($n = 2 \times 10^{18}$ cm^{-3}) and 60 $cm^2/V\,s$ ($n = 1 \times 10^{18}$ cm^{-3}), respectively.

Although it is difficult to achieve *p*-type conductivity in α-Ga_2O_3, corundum-structured *p*-type α-Ir_2O_3 and α-Rh_2O_3 are available.[50] α-Ir_2O_3 was reported to exhibit clear *p*-type conductivity with $\mu = 2.3$ $cm^2/V\,s$ when $p = 1 \times 10^{21}$ cm^{-3}. The small lattice mismatch between α-Ir_2O_3 and α-Ga_2O_3 (~ 0.3%) would be advantageous to form a hetero *pn*-junction and to growth of α-$(Ir_xGa_{1-x})_2O_3$ solid solutions for bandgap tuning. Normally-off MOSFETs using a novel *p*-type corundum semiconductor were demonstrated in 2018 by FLOSFIA and Kyoto University.

As described above, the mist-CVD technique has achieved promising results and is cost-effective due to the simple growth apparatus. However, mist-CVD is a relatively new technique and has not been applied to mass-production of semiconductor epiwafers. In order to utilize the mist-CVD for commercial production, it is necessary to realize the multiwafer large-scale growth apparatus, and the realization requires a steady effort to accumulate basic technical knowledge and know-hows.

2. HVPE

HVPE can be utilized to grow not only β-Ga_2O_3 but also high-purity α-Ga_2O_3 at high growth rates. The growth principle for α-Ga_2O_3 is similar to that of β-Ga_2O_3. Isomorphic α-Ga_2O_3 can be grown on a *c*-plane sapphire substrate when the growth temperature is sufficiently low (typically 500–600 °C).[19] The growth rate increases with increasing growth temperature under fixed precursor supply, which suggests that the growth occurs under the influence of the chemical reaction rate. Nonetheless, the growth rate increases with increasing precursors supply, reaching over 100 μm/h with maintaining a specular surface.

The structural quality of HVPE-grown α-Ga_2O_3 is similar to that of a mist-CVD-grown film, but the tilt angle tends to be larger (~100 arcsec) probably because of the un-optimized nucleation process. The dislocation density measured by plan-view TEM is typically ~10^{10} cm^{-2}. ELO can also be done by HVPE to reduce the dislocation density down to less than 5×10^6 cm^{-2} in laterally grown wing regions.[54] It is also possible to perform facet-initiated ELO (FIELO), which can reduce the dislocation density not only in wing regions but also above mask windows by bending the dislocations by inclined facets.[54] The rapid growth by HVPE is advantageous to achieve island coalescence in the ELO process especially when a small fill factor mask (wide mask and small windows) is

used and, therefore, the dislocation density can be reduced effectively.

The residual Si concentration in an HVPE-grown UID α-Ga_2O_3 film can be less than the detection limit of SIMS (3×10^{15} cm^{-3}, for example),[55] in spite of the existence of H_2 gas as the by-product of the chemical reaction between Ga metal and HCl gas to synthesize GaCl, probably because of the low growth temperature. Cl impurity has also been detected, and the concentration is typically $\sim 1 \times 10^{16}$ cm^{-3}.[55] The residual carrier concentration in UID α-Ga_2O_3 films has not been reported yet, but the film is virtually semi-insulating.

n-type conductivity control is possible by doping donor impurities, such as Ge.[54] Ge is expected to substitute Ga sites causing smaller strain than other donor impurities such as Si and Sn with larger ionic radius. The $GeCl_4$ melt (the melting point is ~−50 °C) is used as a dopant source and the doping is performed by introducing the vapor into the HVPE reactor by means of the conventional bubbling technique. High Ge concentrations ([Ge] = 2.5×10^{19} cm^{-3}, for example) can be achieved without the broadening of XRC-FWHM. The electron mobility of a Ge-doped α-Ga_2O_3 film has been reported to be as high as 28 $cm^2/V\,s$ when $n = 3 \times 10^{19}$ cm^{-3}, which is much higher than that of Sn-doped mist-CVD-grown films (4 $cm^2/V\,s$ when $n = 2 \times 10^{19}$ cm^{-3}, for example). The resistivity of the Ge-doped film was 8.6 mΩ cm, which is much smaller than that of commercially available conductive SiC wafers.

The significance of the HVPE technique which can effectively improve the crystal quality by ELO combined with the rapid growth, is quite large for meta-stable α-Ga_2O_3, which needs to be grown on largely lattice-mismatched substrates. The realization of freestanding α-Ga_2O_3 wafers by HVPE can also be expected, as it happened in GaN industry. Although a large-scale reactor needs to be developed for commercial use, there is a great deal of flexibility in the reactor design; cost-effective high-throughput systems can be built since the growth temperature for α-Ga_2O_3 is relatively low.

3. MOVPE and MBE

Promising results have been reported for β-Ga_2O_3 using MOVPE and MBE, however, the growth of α-Ga_2O_3 by these growth techniques is still at the stage of investigating growth conditions to grow pure-phase α-Ga_2O_3.

In the case of MOVPE, it was reported that the polymorph of Ga_2O_3 on sapphire can be changed from β-Ga_2O_3 to ε-Ga_2O_3, and then to a mixture of ε-Ga_2O_3 and α-Ga_2O_3 by increasing the addition of HCl gas. However, isomorphic α-Ga_2O_3 has not been achieved yet.[56]

In the case of MBE, thickness of isomorphic α-Ga_2O_3 on sapphire is limited. The maximum thickness has been reported to be approximately 0.3 nm on the *c*-plane, 14 nm on the *a*-plane, and 200 nm on the *m*-plane.[57,58]

It is not clear at present why the growth window of MOVPE and MBE is very narrow. The mechanism of the phase selection in these growth techniques needs to be clarified experimentally and theoretically, and the growth conditions should be improved accordingly.

IV. DEVICE FABRICATION AND CHARACTERIZATION

Although promising results have been achieved on the epitaxial growth of α-Ga_2O_3 on sapphire via, mainly, mist-CVD and HVPE, there are only a few reports[52,59,60] on α-Ga_2O_3-based electronic devices. FLOSFIA demonstrated the first vertical Schottky barrier diodes (SBDs) on thin-film corundum-structured gallium oxide (α-Ga_2O_3) grown on sapphire substrates by the MIST EPITAXY technique.[52] Taking advantage of the misfit dislocations and strain accumulated between the α-Ga_2O_3 layer and the sapphire substrate, the epistructure was then lifted off the sapphire substrate and mounted on a heat sink (Fig. 4). The ability to peel off α-Ga_2O_3 from sapphire not only simplifies back-side Ohmic contact deposition but is also of crucial importance to efficiently remove the heat from the device. The latter is of particular interest in the Ga_2O_3 community as this material suffers from very low thermal conductivity. The SBDs exhibited an on-resistance and breakdown voltage of 0.1 mΩ cm^2 and 531 V (SBD1) or 0.4 mΩ cm^2 and 855 V (SBD2), respectively. FLOSFIA also reported the first normally off Ga_2O_3 MOSFETs in 2018 fabricated on the α-Ga_2O_3 film grown on sapphire.[61] They demonstrated a gate threshold voltage of 7.9 V using a novel *p*-type corundum semiconductor which functions as an inversion layer. Dang *et al.*[59] fabricated MESFETs on α-Ga_2O_3 thin films grown on sapphire by mist-CVD. They used AgO_x as a Schottky gate contact. The rectification ratio and reverse breakdown voltage of typical SDs were 6×10^6 and 19.6 V,

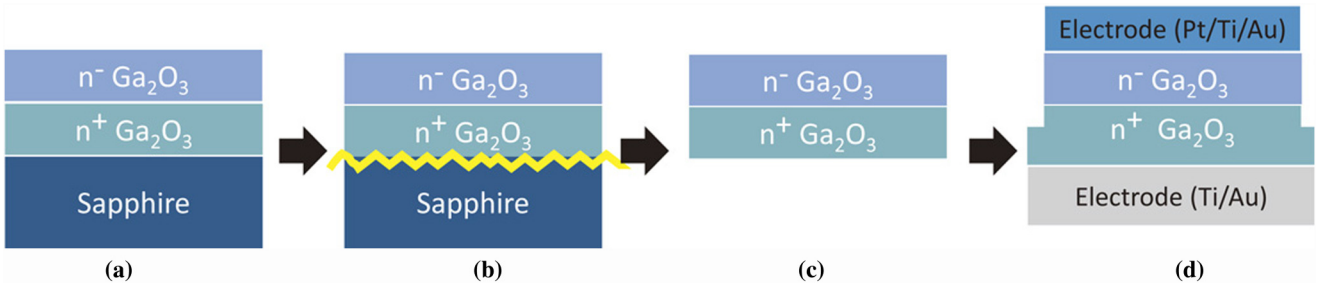

FIG. 4. Schematic demonstrating fabrication steps of the Schottky diode on α-Ga_2O_3. Reproduced with permission from Oda *et al.* Appl. Phys. Express **9** 021101 (2016), Copyright 2016 The Japan Society of Applied Physics.

respectively. The ON/OFF ratio of the corresponding transistors was 2×10^7.

On the other hand, electronic devices based on β-Ga_2O_3 have shown marked progress, including MOSFETs,[62–64] MODFETs,[65–67] FinFETs,[68–71] and SBDs[72–74] on β-Ga_2O_3 substrates facilitated by the availability of substrates. In the following, we will discuss the progress that has been made so far to develop some of the necessary processing steps for device fabrication, including ion implantation, Ohmic contact, Schottky contact, and dry etching. We will then overview various device structures and their characteristics.

A. Building blocks for device fabrication

1. Ohmic contact

Borrowing from GaN technology, Ti/Au has been commonly used as an Ohmic contact in Ga_2O_3-based electronic devices.[75–79] Yao *et al.*[80] investigated different metals (Ti, In, Ag, Sn, W, Mo, Sc, Zn, and Zr) as electrical contacts with *n*-type single-crystal β-Ga_2O_3 ($\bar{2}01$) substrates and studied the impact of annealing temperature up to 800 °C (in flowing Ar). Their studies confirmed that, among all the studied metals, Ti contacts with an Au capping layer were ohmic with the lowest resistance after annealing at 400 °C for 1 min. However, the contacts degraded when annealed above 500 °C. Recently, interfacial reactions and interdiffusion of Ti/Au ohmic contacts with a tin-doped single-crystal β-Ga_2O_3 (010) substrate have been investigated.[81] These studies concluded that the ohmic properties of the Ti/Au metal stack on Ga_2O_3 are attributed to the interdiffusion of Ti and Au and the resulting thin Ti-TiO_x layer, which helps band alignment.

2. Schottky contact

Ni and Pt have been commonly used as the Schottky contact in Ga_2O_3-based devices,[29,73,74,82–84] although other metals including Cu, W, and Ir have been studied as well.[85,86] Studying various wet chemical treatments on the electrical behavior (e.g., barrier heights and ideality factors) of Ni-β-Ga_2O_3 Schottky diodes concluded that the pretreatment with organic solvents followed by HCl, H_2O_2, and DI water results in the most favorable characteristics. Schottky diodes with five different Schottky metals (W, Cu, Ni, Ir, and Pt) were fabricated and little dependence of Schottky barrier height on the metal work function was observed.[85]

Ahmadi *et al.*[29] studied the Schottky contact of Ni on β-$(Al, Ga)_2O_3$ upon varying the Al content from 1 to 13%. The Schottky barrier height and ideality factor were extracted from the I-V measurements. They observed that the apparent Schottky barrier height has similar values for different compositions of β-$(Al_xGa_{1-x})_2O_3$ for the samples studied. This behavior was attributed to the lateral fluctuation in the alloy's composition, with the barrier height determined by the lowest Al composition material.

3. Ion implantation

Development of Si ion implantation in β-Ga_2O_3 has enabled low-resistance ohmic contacts.[71,74,87–89] Sasaki *et al.*[90] studied Si-ion implantation doping with concentrations ranging from 1×10^{19} cm^{-3} to 1×10^{20} cm^{-3} in β-Ga_2O_3. The impact of annealing temperature on the activation of implanted Si atoms was investigated and shown that for concentrations below 5×10^{19} cm^{-3}, a high electrical activation efficiency above 60% was obtained after annealing at a relatively low temperature in the range of 900–1000°C. Contact resistance and resistivity as low as 4.6×10^{-6} Ω cm^2 and 1.4 mΩ cm, respectively, were achieved for the sample with an implanted-Si concentration of 5×10^{19} cm^{-3}.

Implantation of Mg and N of β-Ga_2O_3 as deep acceptor dopants has been also explored.[91] A significant diffusion of Mg atoms was observed when annealed at temperatures above 900 °C, whereas N diffusion was negligible when annealed up to 1100 °C. It was also shown that Mg implantation induces more damage in the β-Ga_2O_3 crystal structure in comparison with N implantation. Though holes were not observed with Mg and N implantation, carrier compensation in bulk *n*-type substrates implanted with Mg or N was observed as evidenced by current blocking in *n*-"*p*"-*n* structures, where "*p*" represents the implanted region.

Mg/N implantation was used to form a current blocking layer (CBL) in planar-gate current aperture vertical Ga_2O_3 MOSFETs.[89,92] In these device structures, Si-implantation was used under source/drain to reduce the contact resistance. Mg implantation was used in the first-generation devices,[92] which led to poor off-state device characteristics as well as a reduced peak extrinsic transconductance. Moreover, the device could not be fully pinched-off. These nonidealities were attributed to the diffusion of Mg at high temperatures. In the next generation,[89] N-implantation was utilized to form the CBL. Well behaved devices with an on-current density of 0.42 kA/cm^2, an $R_{on,sp}$ of 31.5 m cm^2, an ID on/off ratio larger than 10^8, and small I_D dispersion were demonstrated.

4. Dry etching

Chlorine-based dry etching of β-Ga_2O_3 has been studied by several groups.[93–98] Hogan *et al.*[99] compared Chlorine-based Reactive ion etching (RIE) and inductively coupled plasma (ICP) etching techniques. The impact of RF power and chamber pressure on the etch rate and surface roughness for three crystallographic planes, i.e., (100); (010); and ($\bar{2}01$) was investigated by RIE, and moderate etch rates (<20 nm/min) were achieved. Higher etch rates with smoother surface morphology were demonstrated using ICP, perhaps due to the much higher plasma densities and uniformities possible with plasma powers beyond those realized by RIE. They also utilized ICP to study the etch rate of β-Ga_2O_3 (010) with different gas chemistries, including BCl_3, BCl_3/SF_6, CF_4/O_2, and BCl_3/O_2, and a maximum etch rate of 43.0 nm/min was achieved by BCl_3. Zhang *et al.*[96] also studied the ICP (ICP-RIE) etching of β-Ga_2O_3 ($\bar{2}01$) in BCl_3/Ar chemistry and demonstrated etch rates above 150 nm/min using an RIE/ICP power combination of 60 W/900 W. They showed that adding Ar to BCl_3 did not change the etch rate significantly till it reaches a BCl_3/Ar flow rate of 25/15 sccm. Further increase in the Ar flow rate reduced the etch rate, which was unexpected. Ar+ ions can help to remove the etch products and create active sites for chemical etching, which should lead to higher etch rates. However, since BCl_3 produces heavy BCl^{2+} and BCl^{3+} ions that participate in physical etching, meaning BCl_3 by itself provides both chemical and physical etch components in the plasma and, therefore, the addition of Ar may not result in an improvement of the etch rate and merely dilutes the plasma chemistry.

The impact of BCl_3/Ar ICP etching of β-Ga_2O_3 ($\bar{2}01$) on the quality of Ni Schottky contacts was also studied.[93,94,97,98] It was shown that electrically active damage introduced during etching negatively affected the Schottky barrier height and diode ideality factor. The low power etching conditions (150 W of 2 MHz ICP source power and 15 W rf of 13.56 MHz chuck power) which resulted in an etch rate of 12 nm/min, had minimal impact on the reverse breakdown voltage (6% reduction) and the diode ideality factor (increased from 1.00 to 1.06). The barrier height reduced from 1.2 eV to 1.01 eV. In contrast, high power etch conditions (400 W ICP and 200 W rf) resulting in an etch rate of 70 nm/min, significantly damaged the surface and reduced the reverse breakdown voltage by 35%. In addition, the high power etch reduced the barrier height to 0.86 eV and increased the ideality to 1.2. The same group later investigated the effect of annealing before and after gate metal deposition on reducing the damage induced by dry etching.[97] They showed that annealing at 450 C for 1 min in Ar ambient before gate metal deposition was very effective to reduce the surface damage and recover the Schottky diode characteristics.

Very recently, Chlorine-based dry etching of α-Ga_2O_3 was studied.[100] The effects of the BCl_3/Cl_2/Ar gas ratio, bias, and plasma powers and chamber pressure on the etch rate, surface roughness, and mask selectivity were investigated. In contrast to previous dry etching studies on GaN, and similar to those on β-Ga_2O_3, BCl_3 was found to be more effective than Cl_2 to etch α-Ga_2O_3. A high etch rate of 65 nm/min, and nearly vertical sidewalls and smooth etched surfaces were achieved. It was shown that the Si_3N_4 hard mask has the highest resistance to BCl_3-based etching compared to SiO_2 and the photoresist.

B. Schottky diodes (SDs)

SDs are attractive because of their fast switching speed due to the absence of minority carriers. β-Ga_2O_3 SDs with a breakdown voltage above 1 kV[101–108] have been demonstrated by several groups. Different techniques such as field plates,[108,109] guard rings (N-implanted rings),[101] and trench Schottky barriers[102,104] have been utilized to improve the breakdown voltage.

Although these are very promising results, when designing for practical applications, the voltage variations (e. g. brownout and startup conditions) require the ability for the diodes to operate under high current surge in the circuit. This means if the input voltage is dropped, the current must increase to maintain a constant output power. A conductivity-modulation concept is typically used when designing a SiC Schottky diode to accommodate higher current when needed during the surge. As demonstrated in Fig. 5, *p*-type regions are implanted in the *n*-type drift layer. Therefore, the diode has two turn on voltages: (i) Schottky junction turn-on voltage ($V_{on,SJ}$) and (ii) *p*-*n* junction turn-on voltage ($V_{on,PN}$). The diode is biased to operate at low voltages slightly above the $V_{on,SJ}$. However, in rare occasions that surge occurs in the circuit, therefore, the voltage on the Schottky diode is increased to the second turn-on voltage ($V_{on,PN}$) to accommodate the surge current and maintain a low voltage across the diode because of conductivity modulation.

In β-Ga_2O_3 SDs, however, it is difficult to adopt a conductivity-modulation concept due to the unavailability of conductive *p*-type β-Ga_2O_3 which can provide holes in the device. Therefore, developing technologies in β-Ga_2O_3 that can accommodate surge is necessary.

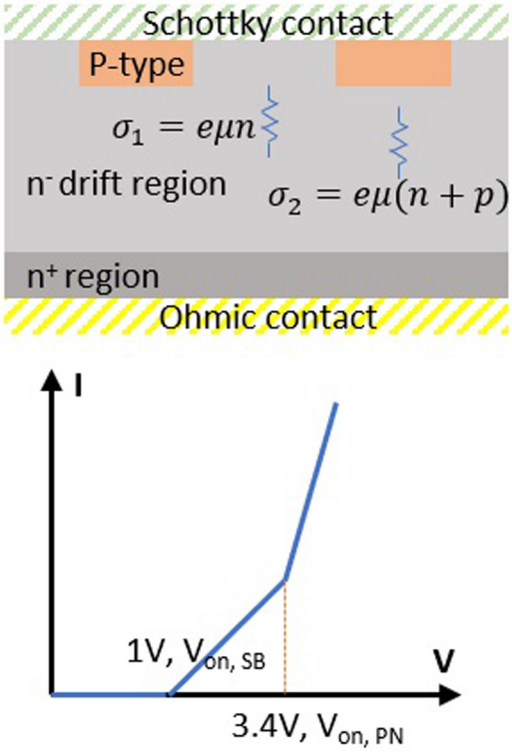

FIG. 5. Schematic of the SD using conductivity-modulation to accommodate for current surge in the circuit.

C. Field effect transistors (FETs)

The first β-Ga_2O_3 FET was reported by Higashiwaki *et al.* and was fabricated on the Sn-doped β-Ga_2O_3 (010) film grown homoepitaxially on a Mg-doped β-Ga_2O_3 substrate by MBE.[110] At this time the device fabrication techniques were immature and therefore a circular FET pattern was used to produce a device without the need for device isolation. Though it possessed poor ohmic contacts and high gate leakage current, a promising breakdown voltage of more than 250 V and an on/off drain current ratio of ~10^4 were obtained. To improve the ohmic contacts, Si-implantation in the source/drain region area was employed followed by an activation annealing at 925 °C in an N_2 environment.[62,111] An atomic layer deposition (ALD) Al_2O_3 dielectric was employed to reduce the high gate current leakage previously observed on their devices. The suppressed gate leakage resulted in a high drain current on/off ratio of over ten orders of magnitude because of an extremely low off-state drain leakage of a few pA/mm, and the breakdown voltage increased to 370 V in the off-state. Moreover, stable transistor operation was sustained at temperatures up to 250 °C, although the drain leakage current increased six orders of magnitude at this high temperature.

This group changed their device fabrication approach going forward, using ion implantation for the active region and the ohmic contacts. First a 1.2 μm UID Ga_2O_3 epilayer was grown on an Fe-doped semi-insulating β-Ga_2O_3 (010) substrate by ozone MBE.[63] Selective area Si-implantation was used to define 300 nm deep channels with a uniform concentration of 3×10^{17} cm^{-3}. Rectangular devices with 2 μm gate length were then fabricated. Room temperature drift mobilities of 90–100 $cm^2 V^{-1} s^{-1}$ were measured in the channel on these devices.[63] To increase the breakdown voltage, the gate-connected field plates were later used and a breakdown voltage up to 750 V in Ga_2O_3 devices was demonstrated.[112] Pulsed measurements showed a power added efficiency of 12%, drain efficiency of 22.4%, output power density of 0.13 W/mm, and maximum gain up to 4.8 dB at 1 GHz.[113] These devices also showed excellent Gamma-ray tolerance after exposure to the highest dose (230 kGy).[114] Radiation-induced degradations in the gate insulation and surface passivation limited the overall radiation resistance of these devices.

The development of chlorine-based dry etching of Ga_2O_3 has enabled device isolation through mesa etch.[115,116] The group at AFRL have fabricated MOSFETs on Sn-doped β-Ga_2O_3 channels grown by MBE[117] and MOCVD[64] on Fe-doped β-Ga_2O_3 (010) and Mg-doped β-Ga_2O_3 (100) substrates, respectively. An average gate-to-drain electric field of 3.8 MV/cm, which is the highest one reported for any transistor and surpassing bulk GaN and SiC theoretical limits, was obtained. Alternate dielectrics and channel dopants have also been explored. Moser *et al.*[117] studied high-k ALD HfO_2 dielectrics for gates in MOSFETs with Sn-doped channels and a pulsed current density of >450 mA/mm was observed upon applying a gate voltage of 4 V. The same group demonstrated the first MOSFET with the Ge-doped channel grown by MBE on (010) Fe-doped semi-insulating substrates.[64] The Ge-doped channel devices performed similarly to previously reported devices with Sn- and Si-doped channels with the drain current ON/OFF ratios $>10^8$ and the saturated drain current >75 mA/mm at VG = 0 V. Hall effect measurements showed a high carrier mobility of 111 $cm^2/(V s)$ with 4×10^{17} cm^{-3} active carriers. They were also first to report the RF performance of β-Ga_2O_3 MOSFETs.[118,119] A gate recess design was used to scale the gate length and a highly doped cap layer was employed under source and drain to reduce the ohmic resistance. Current density, transconductance, f_T, and f_{MAX} of 150 mA/mm, 21.2 mS/mm, 3.3 GHz and 12.9 GHz were measured on these devices, respectively. A maximum output power of 0.23 W/mm was demonstrated with a maximum power added efficiency of 6.3%. An output current of 20 mA mm^{-1} and an on-resistance of 520 mΩ cm^2 were achieved on these devices when a highly-Si-doped Ga_2O_3 cap layer was used under the source and drain.[120] Joishi *et al.*[121] have investigated the impact of Fe-related trap states in the UID buffer due to the diffusion of Fe from the Fe-doped substrate, on MOSFET characteristics. They showed that increasing the buffer layer thickness from 100 nm to 600 nm improves the charge density/electron mobility from 1.4×10^{13} cm^{-2}/65 cm^2/V s to 1.7×10^{13} cm^{-2}/105 cm^2/V s. Additionally, the growth of a thicker UID buffer layer improved the DC-RF dispersion.

In power switching applications, high voltage and high current devices are required. MOSFETs with a breakdown voltage of ~2 kV have been demonstrated using a 400-nm thick composite field plate oxide, with a combination of atomic layer deposited and plasma enhanced chemical vapor deposited SiO_2 layers.[122] E-mode transistors are typically more desirable over D-mode devices due to safety considerations and simplicity of gate-drive circuitry. The E-mode Ga_2O_3 MOSFETs have been realized by depleting the channel via a wrap-gate fin-array field-effect transistor (finFET) structure,[69] an unintentionally doped Ga_2O_3 film with low carrier concentration as the channel,[88] and a gate-recessed structure with ALD SiO_2 as the gate dielectric.[123] Chabak *et al.*[69] were the first to demonstrate E-mode MOSFETs in Sn-doped Ga_2O_3 wrap-gate finFETs on a native semi-insulating Mg-doped (100) β-Ga_2O_3 substrate. These finFETs demonstrated normally off operation with a threshold voltage between 0 and +1 V during high-voltage operation and an I_{ON}/I_{OFF} ratio of greater than 10^5 which were mainly limited by a reduced I_{ON} due to the high on-resistance. The same group recently reported E-mode β-Ga_2O_3 transistors grown homoepitaxially by MBE, utilizing a recessed-gate process, which depleted the channel under the gate followed by the deposition of ALD SiO_2 as the gate dielectric.[124] Wong *et al.*[88] also demonstrated E-mode MOSFETs with low series resistance using Si-ion implantation of the source/drain contacts and access region. In these devices, the channel was formed by an unintentionally doped Ga_2O_3 film with low background carrier concentration. They achieved a positive threshold voltage without additional constraints on the channel dimensions or device architecture. The devices suffered from nonidealities associated with the Al_2O_3 gate dielectric, which caused large hysteresis.

The primary drawback of Ga_2O_3-based MOSFETs is that the low channel mobilities in the channel lead to very low current densities compared with their GaN counterparts. To address this issue, modulation-doped field effect transistors (MODFETs) have been investigated.[26,125–127] Ahmadi *et al.*[26] and Zhang *et al.*[65] have separately reported $(Al_xGa_{1-x})_2O_3$-Ga_2O_3 modulation-doped FETs using Ge and Si as *n*-type dopants in the barrier, respectively. Though Ge is an attractive dopant it has been shown that Ge incorporation in β-Ga_2O_3 films reduces as the substrate temperature increases.[30] Unfortunately, this is in conflict with the higher substrate temperatures required to grow $(Al_xGa_{1-x})_2O_3$ films with a larger Al content.[28] Therefore, the Ge-doped MODFET structures suffer from a low Al content $(Al_xGa_{1-x})_2O_3$ barrier. In contrast, Si incorporation does not depend on the substrate temperature, which allows high growth temperatures for $(Al_xGa_{1-x})_2O_3$ films.[128]

It was expected that the introduction of β-$(Al_xGa_{1-x})_2O_3$ and formation of two-dimensional electron gas (2DEG) will lead to an enhancement of electron mobility in these structures. However, the highest room-temperature electron mobility reported, so far, in β-$(Al_xGa_{1-x})_2O_3$-Ga_2O_3 heterostructures has been only 180 cm^2/V s.[129–131] The electron mobility increased to 2790 cm^2/V s at 50 K. This high electron mobility allowed for the observation of Shubnikov-de-Haas oscillations from which an electron effective mass of 0.33 m_e was extracted, establishing that phonon scattering coupled with the high electron effective mass limited the electron mobility. A maximum drain current of I_{DS} = 257 mA/mm, a peak g_m of 39 mS/mm and a pinch off voltage of −7 V have been measured on MODFETs.[132] Very recently, the same group increased the breakdown voltage of the MODFET from 475 V for a device with a gate-drain spacing (L_{GD}) of 1.55 μm to a high breakdown

voltage of 1.37 kV for a gate-to-drain separation (LGD) of 16 μm having a specific ON-resistance of 120.1 mΩ cm^2 using SiNx as the passivation dielectric.[133]

For high voltage and high-power applications, vertical topologies are preferred to enhance the packing density of devices and suppress the sensitivity of surface effects. Two types of vertical Ga_2O_3-based devices have been reported to date, including current aperture vertical transistors (CAVETs) and FinFETs.

Wong *et al.*[134] fabricated a current aperture vertical transistor (CAVET) with a Mg-implanted current blocking layer (CBL). They recently showed that the N-implanted CBL helps to improve the device characteristics as N atoms are more stable in β-Ga_2O_3, whereas Mg diffuses during the postimplantation-annealing.[89] It must be noted that in this device structure, holes that are generated during the reverse bias will be collected in the CBL. If the CBL is not grounded, the accumulation of holes in this region will lead to a large positive voltage in the CBL and result in a shift in threshold voltage and huge instability in the device performance. Unfortunately, both Mg and N are very deep acceptors (1 eV) in β-Ga_2O_3, and although the N/Mg-implanted layers can be used to block the current, N/Mg-doping of β-Ga_2O_3 does not lead to a conductive *p*-type β-Ga_2O_3 film. Therefore, it is not possible to make the ohmic contact with these current blocking layers. Moving forward, one needs to consider this serious issue while designing β-Ga_2O_3-based CAVETs.

Hu *et al.*,[70] on the other hand, employed a deep-etch process to fabricate ~1 μm thick vertical structures on a low-doped Ga_2O_3 substrate. Very recently, normally-off Ga_2O_3 vertical FinFETs with a threshold voltage of 4 V, breakdown voltage of 1.6 kV, and a drain current density of 600 A/cm ^{2} were demonstrated.[113] The high threshold voltage was achieved by Fin-shaped channels with submicrometer widths. The main issue in these devices is the low electron mobility in the channel (10–30 cm^2/V s) due to the surface roughness and charged surface states caused by dry etching. The low electron mobility in the channel leads to higher R_{on}. Additionally, the surface states due to surface damage caused by dry etching may lead to a hysteresis and a shift in the threshold voltage and device degradation. Therefore, to enhance the performance of β-Ga_2O_3 FinFETs and improve their reliability, various techniques including wet etching, regrowth, and annealing must be investigated to improve the surface quality of the sidewalls, and consequently, the electron mobility of the channel in these structures.

As mentioned earlier, vertical devices are more sensitive to defects and the dislocation densities in the substrate. Therefore, in an immature material system or in a material system in which high-quality substrates are not available, typically increasing the device area (necessary to increase the current for high power applications) leads to reduction in the breakdown voltage and an increase in the reverse-biased leakage current. This is due to the increase in the number of defects or dislocations in the device (which are typically electrically active and form leakage paths) when the device area increases. This phenomenon has also been reported in β-Ga_2O_3 Schottky diodes. However, very recently, Novel Crystal Technology announced that in the epistructures consisting of 5 μm of lightly-doped ($2–9 \times 10^{16}$ cm^{-3}) Ga_2O_3 films grown on n$^+$-doped β-Ga_2O_3 (001) substrates by HVPE, the film quality is such that the breakdown voltage in the reverse direction shall not decrease even if the electrode size of the SBD is enlarged on all over the entire 2-in. epi wafer. This rapid progress in bulk and the epitaxial growth of β-Ga_2O_3 indicate its great potential, particularly, for high-power vertical devices.

V. CONCLUSION AND FUTURE PERSPECTIVE

To summarize, both α- and β-Ga_2O_3 are promising semiconductors for future power electronics applications. For Ga_2O_3 to achieve its full potential, significant sustained funding is necessary for scientific discovery and technology development. This will be catalyzed by "a killer application" in which the advantages of Ga_2O_3 are irrefutable. Such an application is needed to be identified as was done in the case of GaN for next-generation RF transistors.

As discussed earlier, high quality single crystal β-Ga_2O_3 can be grown cost-effectively via conventional melt growth techniques and is already commercially available. The availability of the bulk substrate is the main advantage of β-Ga_2O_3 over α-Ga_2O_3 and other UWB semiconductors and makes the β- phase particularly interesting and provides more advantages for devices with vertical topologies. This is because the performances of vertical devices, such as gate leakage and reliability, are more sensitive to the dislocation density. Additionally, since the electron mobility of Ga_2O_3 is mainly limited by high phonon scattering and high electron effective mass, modulation-doped heterostructures do not lead to any significant improvement in the electron mobility. Therefore, in contrast to GaN power transistors that are dominantly based on AlGaN-GaN high electron mobility transistors (HEMTs), the fabrication of lateral β-Ga_2O_3-based MODFETs or MOSFETs may not provide substantial advantages for high power application. Instead such devices with lateral topologies will increase the device footprint that will lead to an increase in cost. Therefore, design and fabrication of β-Ga_2O_3-based lateral power conversion devices disregards the main advantage of this semiconductor which distinguishes it from all other wide bandgap semiconductors and that is the availability of the cost-effective high-quality bulk substrate. Lateral devices still remain viable for RF applications.

Nonetheless, as mentioned earlier, low thermal conductivity of β-Ga_2O_3 is one of the major obstacles of this material system that must be overcome before it can be considered for practical applications. It has been shown[135] that a β-Ga_2O_3 homoepitaxial device suffers from an unacceptable junction temperature rise of ~1500 °C under a targeted power density of 10 W/mm with a wafer thickness of 500 μm. The effectiveness of various active and passive cooling solutions was tested to achieve a goal of reducing the device operating temperature below 200 °C at a power density of 10 W/mm. This study showed that 100 μm of β-Ga_2O_3, even when integrated with a diamond substrate, is still too thick to achieve the target cooling. In contrast, when the Ga_2O_3 substrate was thinned down to 10 μm, integration with a diamond substrate reduced the junction to package thermal resistance by a factor of six. Flip-chip heterointegration, as shown in Fig. 6, has also been suggested as an effective technique for thermal management. The metal bumps shown in this figure help in removing the heat from the device active region through the contacts, however the dominant thermal resistance is still the contribution from the Ga_2O_3 as the heat flows laterally through the semiconductor to the location of the device-side bond

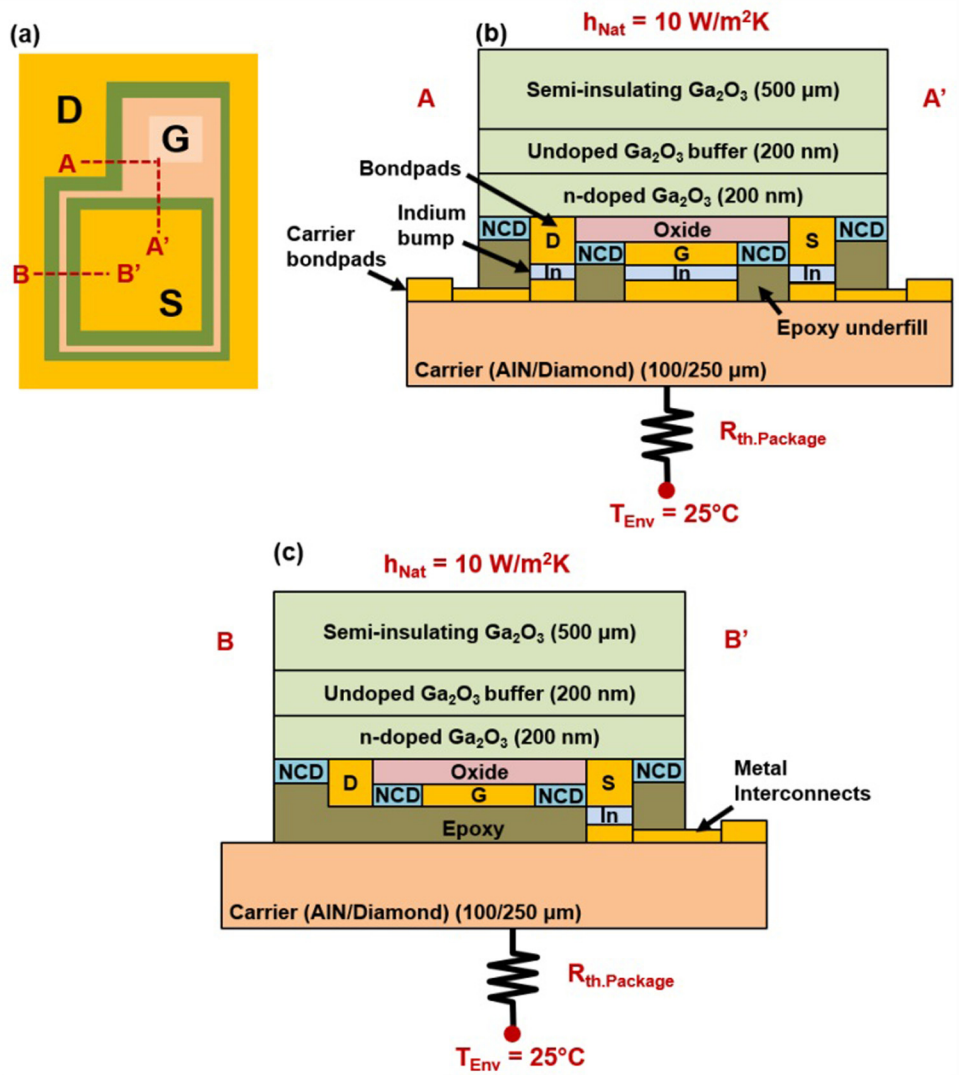

FIG. 6. Schematic of Flip-chip hetero-integration of the β-Ga_2O_3 FET for thermal management. Reproduced with permission from Chatterjee *et al.*, "Device-Level thermal management of gallium oxide field-effect transistors," IEEE Trans. Compon. Packag. Manuf. Technol. (published online), Copyright 2019 IEEE.

pads. Incorporating high thermal conductivity into nano-crystal diamond passivation further helps with heat removal from the device active region. Figure 7(a) shows the comparison of the device junction temperature rise at 10 W/mm upon varying the carrier wafer material (AlN vs diamond), carrier thickness (100 μm vs 250 μm), and electrical bump material (In vs Au). Figure 7(b) shows the effect of the thermal conductivity of the epoxy under-fill material on the device temperature rise. Therefore, although the low thermal conductivity of Ga_2O_3 is the main drawback of this material system, there are feasible pathways to address this issue.

One of the advantages of α-Ga_2O_3 is its corundum crystal structure which allows for an all-oxide p-n junction through the epitaxial growth of heterostructures with corundum-structured *p*-type oxides such as Rh_2O_3 or Ir_2O_3. Moreover, there are several transition metal oxides (α-M_2O_3; M = Fe, Cr, V, Ti, Rh, and Ir) which form in the corundum crystal structure (Fig. 8) with ferroelectric and ferromagnetic properties, enabling integration with multifunctional devices.[136,137] Additionally, α-Ga_2O_3 has a similar crystal structure as that of sapphire (Al_2O_3) and α-In_2O_3. Therefore, the epitaxial growth of α-$(In,Ga,Al)_2O_3$ alloys allows bandgap engineering from 3.8 eV to 8.8 eV. The possibility of epitaxial growth of α-$(Al_xGa_{1-x})_2O_3$ films with a larger Al content on α-Ga_2O_3 enables larger conduction band discontinuity in these heterostructures which will, consequently, allow for higher densities of two-dimensional electron gas in these heterostructures beyond what is achievable in β-$(Al,Ga)_2O_3$-Ga_2O_3 heterostructures. Nonetheless, α-Ga_2O_3 bulk substrates are not currently available and α-Ga_2O_3 films must be grown heteroepitaxially on sapphire substrates, and the threading dislocation density is several orders of magnitude larger than that in β-Ga_2O_3 substrates. As mentioned earlier, devices with vertical topologies are more sensitive to threading dislocation density. Therefore, at least until high quality free-standing α-Ga_2O_3 substrates

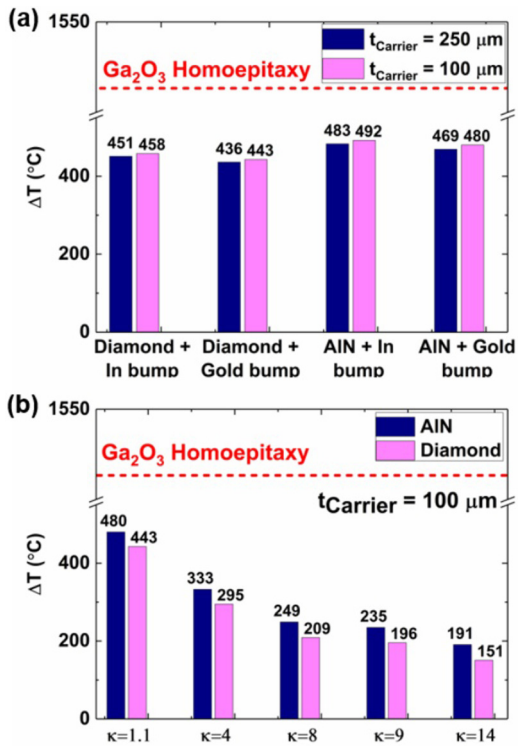

FIG. 7. (a). Device junction temperature rise at 10 W/mm as a function of the carrier wafer material (AlN vs diamond), carrier thickness (100 μm vs 250 μm), and electrical bump material (In vs Au). (b) The effect of thermal conductivity of the epoxy under-fill material on device temperature rise. Chatterjee *et al.*, "Device-Level thermal management of gallium oxide field-effect transistors," IEEE Trans. Compon. Packag. Manuf. Technol. (published online). Copyright 2019 IEEE.

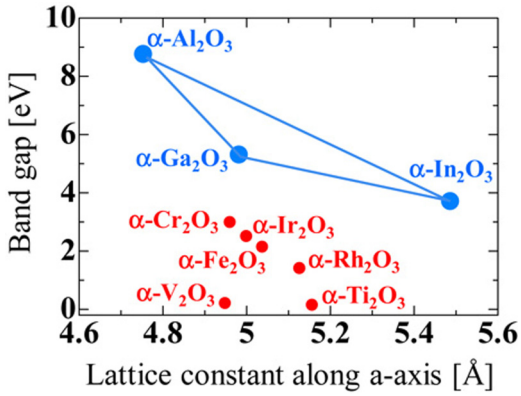

FIG. 8. Relationship between the bandgap and lattice constant along a axis of 9 types of corundum-structured oxides. Reproduced with permission from Kaneko *et al.*, Jpn. J. Appl. Phys. **57** 02CB18 (2018). Copyright 2018 The Japan Society of Applied Physics.

with low threading dislocations are available, horizontal structures are more suitable for α-Ga_2O_3-based electronic devices. Additionally, since α-Ga_2O_3 can be lifted off sapphire relatively easily, the low thermal conductivity of this material can be addressed simply by bonding it to other substrates (SiC, AlN, diamond, etc.) with higher thermal conductivity. Therefore, α-$(In,Ga,Al)_2O_3$ heterostructures are very promising for high power switching and RF applications. Nevertheless, as mentioned earlier, there have been only a few reports on α-Ga_2O_3 devices, which is mainly due to the unavailability of substrates. Therefore, to discover the full potential of the α-$(Al,Ga,In)_2O_3$ material system, it is crucial to realize high-quality α-Ga_2O_3 freestanding substrates or template substrates. HVPE will play a key role in the development of such α-Ga_2O_3 substrates, just like it did in GaN technology. The key technologies, such as rapid growth, conductivity control, defect control, have already been demonstrated as described in Sec. III B 2. Therefore, demonstration of high-quality α-Ga_2O_3 substrates in the near future is expected and will require further development of the key technologies.

ACKNOWLEDGMENTS

Professor Umesh Mishra is acknowledged for many fruitful discussions on device perspectives.

REFERENCES

[1]Green Power Electronics, Council on Competitiveness-Nippon 2009 Report (in Japanese).
[2]M. Rosina, Yole Development Report Presented in SEMICON Europa (2018).
[3]Y. M. Tairov and V. F. Tsvetkov, "Investigation of growth processes of ingots of silicon carbide single crystals," J. Cryst. Growth **43**, 209–212 (1978).
[4]Y. Oshima, T. Eri, M. Shibata, H. Sunakawa, K. Kobayashi, T. Ichihashi, and A. Usui, "Preparation of freestanding GaN wafers by hydride vapor phase epitaxy with void-assisted separation," Jpn. J. Appl. Phys. **42**, L1–3 (2003).
[5]K. Motoki, T. Okahisa, N. Matsumoto, M. Matsushima, H. Kimura, H. Kasai, K. Takemoto, K. Uematsu, T. Hirano, M. Nakayama, S. Nakahata, M. Ueno, D. Hara, Y. Kumagai, A. Koukitu, and H. Seki, "Preparation of large freestanding GaN substrates by hydride vapor phase epitaxy using GaAs as a starting substrate," Jpn. J. Appl. Phys. **40**, L140–3 (2001).
[6]E. G. Víllora, K. Shimamura, Y. Yoshikawa, K. Aoki, and N. Ichinose, "Large-size β-Ga_2O_3 single crystals and wafers," J. Cryst. Growth **270**, 420–426 (2004).
[7]H. Aida, K. Nishiguchi, H. Takeda, N. Aota, K. Sunakawa, and Y. Yaguchi, "Growth of β-Ga_2O_3 single crystals by the edge-defined, film fed growth method," Jpn. J. Appl. Phys. **47**, 8506–8509 (2008).
[8]A. Kuramata, K. Koshi, S. Watanabe, Y. Yamaoka, T. Masui, and S. Yamakoshi, "High-quality β-Ga_2O_3 single crystals grown by edge-defined film-fed growth," Jpn. J. Appl. Phys. **55**, 1202A2 (2016).
[9]M. Kasu, K. Hanada, T. Moribayashi, A. Hashiguchi, T. Oshima, T. Oishi, K. Koshi, K. Sasaki, A. Kuramata, and O. Ueda, "Relationship between crystal defects and leakage current in β-Ga_2O_3 Schottky barrier diodes," Jpn. J. Appl. Phys. **55**, 1202BB (2016).
[10]K. Nakai, T. Nagai, K. Noami, and T. Futagi, "Characterization of defects in β-Ga_2O_3 single crystals," Jpn. J. Appl. Phys. **54**, 051103 (2015).
[11]Y. Tomm, P. Reiche, D. Klimm, and T. Fukuda, "Czochralski grown Ga_2O_3 crystals," J. Cryst. Growth **220**, 510–514 (2000).
[12]Z. Galazka, K. Irmscher, R. Uecker, R. Bertram, M. Pietsch, A. Kwasniewski, M. Naumann, T. Schulz, R. Schewski, D. Klimm, and M. Bickermann, "On the bulk β-Ga_2O_3 single crystals grown by the Czochralski method," J. Cryst. Growth **404**, 184–191 (2014).

[13]J. Blevins, K. Chabak, G. Jessen, D. Thomson, K. Stevens, G. Foundos, J. Leach, J. Rumsey, and A. Green, "13.5 growth of 50 mm beta-gallium oxide (β-Ga2O3) substrates," in CSMantech, 2018.
[14]Z. Galazka, R. Uecker, D. Klimm, K. Irmscher, M. Naumann, M. Pietsch, A. Kwasniewski, R. Bertram, S. Ganschow, and M. Bickermann, "Scaling-Up of bulk β-Ga_2O_3 single crystals by the Czochralski method," ECS J. Solid State Sci. Technol. **6**, Q3007–11 (2017).
[15]E. G. Víllora, K. Shimamura, Y. Yoshikawa, T. Ujiie, and K. Aoki, "Electrical conductivity and carrier concentration control in β-Ga_2O_3 by Si doping," Appl. Phys. Lett. **92**, 202120 (2008).
[16]N. Ueda, H. Hosono, R. Waseda, and H. Kawazoe, "Synthesis and control of conductivity of ultraviolet transmitting β-Ga_2O_3 single crystals," Appl. Phys. Lett. **70**, 3561–3563 (1997).
[17]K. Hoshikawa, E. Ohba, T. Kobayashi, J. Yanagisawa, C. Miyagawa, and Y. Nakamura, "Growth of β-Ga_2O_3 single crystals using vertical Bridgman method in ambient air," J. Cryst. Growth **447**, 36–41 (2016).
[18]T. Kawaharamura, G. T. Dang, and M. Furuta, Jpn. J. Appl. Phys. **51**, 040207 (2012).
[19]Y. Oshima, E.G. Víllora, and K. Shimamura, Appl. Phys. Express **8**, 055501 (2015).
[20]D. Machon, P. F. McMillan, B. Xu, and J. Dong, "High-pressure study of the β -to- α transition in Ga_2O_3," Phys. Rev. B **73**, 094125 (2006).
[21]J. P. Remeika and M. Marezio, "Growth of α-Ga_2O_3 single crystals at 44 kbars," Appl. Phys. Lett. **8**, 87–88 (1966).
[22]R. Schewski, M. Baldini, K. Irmscher, A. Fiedler, T. Markurt, B. Neuschulz, T. Remmele, T. Schulz, G. Wagner, Z. Galazka, and M. Albrecht, "Evolution of planar defects during homoepitaxial growth of β-Ga_2O_3 layers on (100) substrates—A quantitative model," J. Appl. Phys. **120**, 225308 (2016).
[23]K. Sasaki, A. Kuramata, T. Masui, E. G. Víllora, K. Shimamura, and S. Yamakoshi, "Device-quality b-Ga_2O_3 epitaxial films fabricated by ozone molecular beam epitaxy," Appl. Phys. Express **5**, 035502 (2012).
[24]P. Vogt and O. Bierwagen, "Reaction kinetics and growth window for plasma-assisted molecular beam epitaxy of Ga_2O_3: Incorporation of Ga vs. Ga_2O desorption," Appl. Phys. Lett. **108**, 072101 (2016).
[25]Y. Oshima, E. Ahmadi, S. Kaun, and F. Wu, "Growth and etching characteristics of (001) β-Ga_2O_3 by plasma-assisted molecular beam epitaxy," Mater. Chem. Phys. **133**, 1–6 (2012).
[26]E. Ahmadi, O. S. Koksaldi, X. Zheng, T. Mates, Y. Oshima, U. K. Mishra, and J. S. Speck, "Demonstration of β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 modulation doped field-effect transistors with Ge as dopant grown via plasma-assisted molecular beam epitaxy," Appl. Phys. Express **10**, 071101 (2017).
[27]V. G. Hill, R. Roy, and E. F. Osborn, "The system alumina-gallia-water," J. Am. Ceram. Soc. **35**, 135–142 (1952).
[28]S. W. Kaun, F. Wu, and J. S. Speck, "β-$(Al_xGa_{1-x})_2O_3$/Ga_2O_3 (010) heterostructures grown on β-Ga_2O_3 (010) substrates by plasma-assisted molecular beam epitaxy," J. Vac. Sci. Technol. A **33**, 041508 (2015).
[29]E. Ahmadi, Y. Oshima, F. Wu, and J. S. Speck, "Schottky barrier height of Ni to β-$(Al_xGa_{1-x})_2O_3$ with different compositions grown by plasma-assisted molecular beam epitaxy," Semicond. Sci. Technol. **32**, 035004 (2017).
[30]E. Ahmadi, O. S. Koksaldi, S. W. Kaun, Y. Oshima, D. B. Short, U. K. Mishra, and J. S. Speck, "Ge doping of β-Ga_2O_3 films grown by plasma-assisted molecular beam epitaxy," Appl. Phys. Express **10**, 041102 (2017).
[31]T. Oshima, Y. Kato, N. Kawano, A. Kuramata, S. Yamakoshi, S. Fujita, T. Oishi, and M. Kasu, "Carrier confinement observed at modulation-doped β-$(Al_xGa_{1-x})_2O_3$/Ga_2O_3 heterojunction interface," Appl. Phys. Express **10**, 035701 (2017).
[32]Y. Zhang, Z. Xia, J. Mcglone, W. Sun, C. Joishi, A. R. Arehart, S. A. Ringel, and S. Rajan, "Evaluation of Low-temperature saturation velocity in -$(Al_xGa_{1-x})_2O_3$/Ga_2O_3 modulation-doped field-effect transistors," IEEE Trans. Electron Devices **66**, 1574–1578 (2019).
[33]K. Nomura, K. Goto, R. Togashi, H. Murakami, Y. Kumagai, A. Kuramata, S. Yamakoshi, and A. Koukitu, "Thermodynamic study of β-Ga_2O_3 growth by halide vapor phase epitaxy," J. Cryst. Growth **405**, 19–22 (2014).
[34]Y. Oshima, E. G. Víllora, and K. Shimamura, "Quasi-heteroepitaxial growth of β-Ga_2O_3 on off-angled sapphire (0 0 0 1) substrates by halide vapor phase epitaxy," J. Cryst. Growth **410**, 53–58 (2015).
[35]K. Konishi, K. Goto, R. Togashi, H. Murakami, M. Higashiwaki, A. Kuramata, S. Yamakoshi, B. Monemar, and Y. Kumagai, "Comparison of O_2 and H_2O as oxygen source for homoepitaxial growth of β-Ga_2O_3 layers by halide vapor phase epitaxy," J. Cryst. Growth **492**, 39–44 (2018).
[36]H. Murakami, K. Nomura, K. Goto, K. Sasaki, K. Kawara, Q. T. Thieu, R. Togashi, Y. Kumagai, M. Higashiwaki, A. Kuramata, S. Yamakoshi, B. Monemar, and A. Koukitu, "Homoepitaxial growth of β-Ga_2O_3 layers by halide vapor phase epitaxy," Appl. Phys. Express **8**, 015503 (2015).
[37]J. H. Leach, K. Udwary, J. Rumsey, G. Dodson, H. Splawn, and K. R. Evans, "Halide vapor phase epitaxial growth of β-Ga_2O_3 and α-Ga_2O_3 films," APL Mater. **7**, 022504 (2019).
[38]J. B. Varley, J. R. Weber, A. Janotti, and C. G. Van de Walle, "Oxygen vacancies and donor impurities in β-Ga_2O_3," Appl. Phys. Lett. **97**, 142106 (2010).
[39]M. Higashiwaki, K. Sasaki, H. Murakami, Y. Kumagai, A. Koukitu, A. Kuramata, T. Masui, and S. Yamakoshi, "Recent progress in Ga_2O_3 power devices," Semicond. Sci. Technol. **31**, 034001 (2016).
[40]F. Alema, B. Hertog, A. Osinsky, P. Mukhopadhyay, M. Toporkov, and W. V. Schoenfeld, "Fast growth rate of epitaxial β–Ga_2O_3 by close coupled showerhead MOCVD," J. Cryst. Growth **475**, 77–82 (2017).
[41]J. L. Lyons, D. Steiauf, A. Janotti, and C. G. Van de Walle, "Carbon as a shallow donor in transparent conducting oxides," Phys. Rev. Appl. **2**, 064005 (2014).
[42]Z. Feng, A. F. M. Anhar Uddin Bhuiyan, M. R. Karim, and H. Zhao, "MOCVD homoepitaxy of Si-doped (010) β-Ga_2O_3 thin films with superior transport properties," Appl. Phys. Lett. **114**, 250601 (2019).
[43]R. Miller, F. Alema, and A. Osinsky, "Epitaxial β-Ga_2O_3 and β-$(Al_xGa_{1-x})_2O_3$-Ga_2O_3 heterostructures growth for power electronics," IEEE Trans. Semicond. Manuf. **31**, 467–474 (2018).
[44]Y. Zhang, F. Alema, A. Mauze, O. S. Koksaldi, R. Miller, A. Osinsky, and J. S. Speck, "MOCVD grown epitaxial β-Ga_2O_3 thin film with an electron mobility of 176 $cm^2/V\,s$ at room temperature," APL Mater. **7**, 022506 (2019).
[45]F. Alema, B. Hertog, P. Mukhopadhyay, Y. Zhang, A. Mauze, A. Osinsky, W. V. Schoenfeld, J. S. Speck, and T. Vogt, "Solar blind Schottky photodiode based on an MOCVD-grown homoepitaxial β-Ga_2O_3 thin film," APL Mater. **7**, 022527 (2019).
[46]D. Gogova, G. Wagner, M. Baldini, M. Schmidbauer, K. Irmscher, R. Schewski, Z. Galazka, M. Albrecht, and R. Fornari, "Structural properties of Si-doped β-Ga_2O_3 layers grown by MOVPE," J. Cryst. Growth **401**, 665–669 (2014).
[47]D. Shinohara and S. Fujita, "Heteroepitaxy of corundum-structured α-Ga_2O_3 thin films on α-Al_2O_3 substrates by ultrasonic mist chemical vapor deposition," Jpn. J. Appl. Phys. **47**, 7311–7313 (2008).
[48]R. Jinno, T. Uchida, K. Kaneko, and S. Fujita, "Reduction in edge dislocation density in corundum-structured α-Ga_2O_3 layers on sapphire substrates with quasi-graded α-$(Al,Ga)_2O_3$ buffer layers," Appl. Phys. Express **9**, 071101 (2016).
[49]S. Fujita and K. Kaneko, "Epitaxial growth of corundum-structured wide band gap III-oxide semiconductor thin films," J. Cryst. Growth **401**, 588–592 (2014).
[50]K. Kaneko, K. Suzuki, Y. Ito, and S. Fujita, "Growth characteristics of corundum-structured α-$(Al_xGa_{1-x})_2O_3$/Ga_2O_3 heterostructures on sapphire substrates," J. Cryst. Growth **436**, 150–154 (2016).
[51]K. Akaiwa and S. Fujita, "Electrical conductive corundum-structured α-Ga_2O_3 thin films on sapphire with Tin-doping grown by spray-assisted mist chemical vapor deposition," Jpn. J. Appl. Phys. **51**, 070203 (2012).
[52]M. Oda, R. Tokuda, H. Kambara, T. Tanikawa, T. Sasaki, and T. Hitora, "Schottky barrier diodes of corundum-structured gallium oxide showing on-resistance of 0.1 $m\Omega\,cm^2$ grown by MIST EPITAXY®," Appl. Phys. Express **9**, 021101 (2016).
[53]K. Akaiwa, K. Kaneko, K. Ichino, and S. Fujita, "Conductivity control of Sn-doped α-Ga_2O_3 thin films grown on sapphire substrates," Jpn. J. Appl. Phys. **55**, 1202BA (2016).

[54]Y. Oshima, K. Kawara, T. Shinohe, T. Hitora, M. Kasu, and S. Fujita, "Epitaxial lateral overgrowth of α-Ga_2O_3 by halide vapor phase epitaxy," APL Mater. **7**, 022503 (2019).
[55]Y. Oshima, "Heteroepitaxial growth of α and ε-Ga_2O_3," in *Gallium Oxide: Crystal Growth, Materials Properties, and Devices* (Springer, 2019).
[56]H. Sun, K.-H. Li, C. G. T. Castanedo, S. Okur, G. S. Tompa, T. Salagaj, S. Lopatin, A. Genovese, and X. Li, "HCl flow-induced phase change of α-, β-, and ε-Ga_2O_3 films grown by MOCVD," Cryst. Growth Des. **18**, 2370–2376 (2018).
[57]Z. Cheng, M. Hanke, P. Vogt, O. Bierwagen, and A. Trampert, "Phase formation and strain relaxation of Ga_2O_3 on c-plane and a-plane sapphire substrates as studied by synchrotron-based x-ray diffraction," Appl. Phys. Lett. **111**, 162104 (2017).
[58]R. Jinno, Y. Cho, K. Lee, V. Protasenko, H. G. Xing, and D. Jena, "Stabilization of alpha-Ga_2O_3 on m-plane alpha-Al_2O_3 by Plasma-Assisted MBE," in *66th JSAP Spring Meeting, Tokyo, Japan* (2019).
[59]G. T. Dang, T. Kawaharamura, M. Furuta, and M. W. Allen, "Mist-CVD grown Sn-doped alpha-Ga_2O_3 MESFETs," IEEE Trans. Electron Devices **62**, 3640–3644 (2015).
[60]Z. Hu, K. Nomoto, W. Li, R. Jinno, T. Nakamura, D. Jena, and H. Xing, "1.6 kV vertical Ga_2O_3 FinFETs with source-connected field plates and normally-off operation," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, (IEEE, 2019), pp. 483–486.
[61]2018 Ground breaking work on gallium oxide (Ga_2O_3) normally-off transistor *Flosfia*.
[62]M. Higashiwaki, K. Sasaki, T. Kamimura, M. Hoi Wong, D. Krishnamurthy, A. Kuramata, T. Masui, and S. Yamakoshi, "Depletion-mode Ga_2O_3 metal-oxide-semiconductor field-effect transistors on β-Ga_2O_3 (010) substrates and temperature dependence of their device characteristics," Appl. Phys. Lett. **103**, 1–5 (2013).
[63]M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Electron channel mobility in silicon-doped Ga_2O_3 MOSFETs with a resistive buffer layer," Jpn. J. Appl. Phys. **55**, 1202–1211 (2016).
[64]A. J. Green, K. D. Chabak, E. R. Heller, R. C. Fitch, M. Baldini, A. Fiedler, K. Irmscher, G. Wagner, Z. Galazka, S. E. Tetlak, A. Crespo, K. Leedy, and G. H. Jessen, "3.8-MV/cm breakdown strength of MOVPE-grown Sn-doped β-Ga_2O_3 MOSFETs," IEEE Electron Device Lett. **37**, 902–905 (2016).
[65]Y. Zhang, A. Neal, Z. Xia, C. Joishi, J. M. Johnson, Y. Zheng, S. Bajaj, M. Brenner, D. Dorsey, K. Chabak, G. Jessen, J. Hwang, S. Mou, J. P. Heremans, and S. Rajan, "Demonstration of high mobility and quantum transport in modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures," Appl. Phys. Lett. **112**, 173502 (2018).
[66]C. Joishi, Y. Zhang, Z. Xia, W. Sun, A. R. Arehart, S. Ringel, S. Lodha, and S. Rajan, "Breakdown characteristics of β-$(Al_{0.22}Ga_{0.78})_2O_3/Ga_2O_3$ field-plated modulation doped field effect transistors with SiNx passivation," IEEE Electron Device Lett. 40, 1241 (2019).
[67]Y. Zhang, C. Joishi, Z. Xia, M. Brenner, S. Lodha, and S. Rajan, "Demonstration of β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ double heterostructure field effect transistors," Appl. Phys. Lett. **112**, 233503 (2018).
[68]Y. Zhang, M. Sun, D. Piedra, J. Hu, Z. Liu, Y. Lin, X. Gao, K. Shepard, and T. Palacios, "1200 V GaN vertical fin power field-effect transistors," in *2017 IEEE International Electron Devices Meeting (IEDM)*, (IEEE, 2017), pp. 9.2.1–9.2.4.
[69]K. D. Chabak, N. Moser, A. J. Green, D. E. Walker, S. E. Tetlak, E. Heller, A. Crespo, R. Fitch, J. P. McCandless, K. Leedy, M. Baldini, G. Wagner, Z. Galazka, X. Li, and G. Jessen, "Enhancement-mode Ga_2O_3 wrap-gate fin field-effect transistors on native (100) β-Ga_2O_3 substrate with high breakdown voltage," Appl. Phys. Lett. **109**, 213501 (2016).
[70]Z. Hu, K. Nomoto, W. Li, L. Zhang, J.-H. Shin, N. Tanen, T. Nakamura, D. Jena, and H. G. Xing, "Vertical fin Ga_2O_3 power field-effect transistors with on/off ratio >109," in *2017 75th Annual Device Research Conference (DRC)* (IEEE, South Bend, IN, 2017).
[71]Z. Hu, K. Nomoto, W. Li, Z. Zhang, N. Tanen, Q. T. Thieu, K. Sasaki, A. Kuramata, T. Nakamura, D. Jena, and H. G. Xing, "Breakdown mechanism in 1 kA/cm ^{2} and 960 V E-mode β-Ga_2O_3 vertical transistors," Appl. Phys. Lett. **113**, 122103 (2018).
[72]B. Song, A. K. Verma, K. Nomoto, M. Zhu, D. Jena, and H. G. Xing, "Vertical Ga_2O_3 Schottky barrier diodes on single-crystal β-Ga_2O_3 (-201) substrates," in *2016 74th Annual Device Research Conference* (IEEE, 2016), Vol. 3, pp. 1–2.
[73]W. Li, K. Nomoto, Z. Hu, N. Tanen, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, "1.5 kV Vertical Ga_2O_3 Trench-MIS Schottky barrier diodes," in *2018 76th Device Research Conference* (IEEE, 2018), Vol. 110, pp. 1–2.
[74]W. Li, Z. Hu, K. Nomoto, Z. Zhang, J-Y. Hsu, Q. T. Thieu, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, "1230 V β-Ga_2O_3 trench Schottky barrier diodes with an ultra-low leakage current of <1 μA/cm^2," Appl. Phys. Lett., **113** 202101 (2018).
[75]E. Ahmadi, F. Wu, H. Li, S. W. Kaun, M. Tahhan, K. Hestroffer, S. Keller, J. S. Speck, and U. K. Mishra, "N-face GaN/AlN/GaN/InAlN and GaN/AlN/AlGaN/GaN/InAlN high-electron-mobility transistor structures grown by plasma-assisted molecular beam epitaxy on vicinal substrates," Semicond. Sci. Technol. **30**, 055012 (2015).
[76]A. T. Neal, S. Mou, S. Rafique, H. Zhao, E. Ahmadi J. S., D. B. Speck, N. Thomson, K. D. Moser, and G. H. J. Chabak, "Donors and acceptors in β-Ga_2O_3," Appl. Phys. Lett. **113**, 062101 (2018).
[77]N. Moser, J. McCandless, A. Crespo, K. Leedy, A. Green, A. Neal, S. Mou, E. Ahmadi, J. Speck, K. Chabak, N. Peixoto, and G. Jessen, "Ge-Doped β-Ga_2O_3 MOSFETs," IEEE Electron Device Lett. **38**, 775–778 (2017).
[78]M. Higashiwaki, *Current Status of Gallium Oxide-Based Power Device Technology* (IEEE, 2015), pp. 1–4.
[79]M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Field-Plated Ga_2O_3 MOSFETs With a breakdown voltage of over 750 V," IEEE Electron Device Lett. **37**, 212–215 (2016).
[80]Y. Yao, R. F. Davis, and L. M. Porter, "Investigation of different metals as ohmic contacts to β-Ga_2O_3: Comparison and analysis of electrical behavior, morphology, and other physical properties," J. Electron. Mater. **46**, 2053–2060 (2017).
[81]M.-H. Lee and R. L. Peterson, "Interfacial reactions of titanium/gold ohmic contacts with Sn-doped β-Ga_2O_3," APL Mater. **7**, 022524 (2019).
[82]M. Higashiwaki, K. Sasaki, K. Goto, K. Nomura, Q. T. Thieu, R. Togashi, H. Murakami, Y. Kumagai, B. Monemar, A. Koukitu, A. Kuramata, and S. Yamakoshi, "Ga_2O_3 Schottky barrier diodes with n–Ga_2O_3 drift layers grown by HVPE," in *Device Research Conference-Conference Digest* (DRC, 2015), Vol. 2015, pp. 29–30.
[83]K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Ga_2o_3 Schottky barrier diodes fabricated by using single-crystal β-Ga_2O_3 (010) substrates," IEEE Electron Device Lett. **34**, 493–495 (2013).
[84]D. Khan, D. Gajula, S. Okur, G. S. Tompa, and G. Koley, "β-Ga_2O_3 thin film based lateral and vertical Schottky barrier diode," ECS J. Solid State Sci. Technol. **8**, Q106–10 (2019).
[85]Y. Yao, R. Gangireddy, J. Kim, K. K. Das, R. F. Davis, and L. M. Porter, "Electrical behavior of β-Ga_2O_3 Schottky diodes with different Schottky metals," J. Vac. Sci. Technol. B **35**, 03D113 (2017).
[86]D. Splith, S. Müller, F. Schmidt, H. von Wenckstern, J. J. van Rensburg, W. E. Meyer, and M. Grundmann, "Determination of the mean and the homogeneous barrier height of Cu Schottky contacts on heteroepitaxial β-Ga_2O_3 thin films grown by pulsed laser deposition," Phys. Status Solidi **211**, 40–47 (2014).
[87]Z. Hu, K. Nomoto, W. Li, N. Tanen, K. Sasaki, A. Kuramata, T. Nakamura, D. Jena, and H. G. Xing, "Enhancement-Mode Ga_2O_3 vertical transistors With breakdown voltage >1 kV," IEEE Electron Device Lett. **39**, 869–872 (2018).
[88]M. H. Wong, Y. Nakata, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Enhancement-mode Ga_2O_3 MOSFETs with Si-ion-implanted source and drain," Appl. Phys. Express **10**, 3–6 (2017).
[89]M. H. Wong, K. Goto, H. Murakami, Y. Kumagai, and M. Higashiwaki, "Current aperture vertical β-Ga_2O_3 MOSFETs fabricated by N- and Si-Ion implantation doping," IEEE Electron Device Lett. **40**, 431–434 (2019).
[90]K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Si-Ion implantation doping in β-Ga_2O_3 and its application to fabrication of low-resistance ohmic contacts," Appl. Phys. Express **6**, 086502 (2013).
[91]M. H. Wong, C.-H. Lin, A. Kuramata, S. Yamakoshi, H. Murakami, Y. Kumagai, and M. Higashiwaki, "Acceptor doping of β-Ga_2O_3 by Mg and N ion implantations," Appl. Phys. Lett. **113**, 102103 (2018).

[92]M. H. Wong, K. Goto, Y. Morikawa, A. Kuramata, S. Yamakoshi, H. Murakami, Y. Kumagai, and M. Higashiwaki, Appl. Phys. Express **11**, 064102 (2018).
[93]A. Y. Polyakov, I.-H. Lee, N. B. Smirnov, E. B. Yakimov, I. V. Shchemerov, A. V. Chernykh, A. I. Kochkova, A. A. Vasilev, P. H. Carey, F. Ren, D. J. Smith, and S. J. Pearton, "Defects at the surface of β-Ga_2O_3 produced by Ar plasma exposure," APL Mater. **7**, 061102 (2019).
[94]J. Yang, S. Ahn, F. Ren, S. Pearton, R. Khanna, K. Bevlin, D. Geerpuram, and A. Kuramata, "Inductively coupled plasma etching of bulk, single-crystal Ga_2O_3," J. Vac. Sci. Technol. B **35**, 031205 (2017).
[95]S. Jang, S. Jung, K. Beers, J. Yang, F. Ren, A. Kuramata, S. J. Pearton, and K. H. Baik, "A comparative study of wet etching and contacts on ($2^{-}01$) and (010) oriented β-Ga_2O_3," J. Alloys Compd. **731**, 118–125 (2018).
[96]L. Zhang, A. Verma, H. G. Xing, and D. Jena, "Inductively-coupled-plasma reactive ion etching of single-crystal β-Ga_2O_3," Jpn. J. Appl. Phys. **56**, 030304 (2017).
[97]J. Yang, F. Ren, R. Khanna, K. Bevlin, D. Geerpuram, L.-C. Tung, J. Lin, H. Jiang, J. Lee, E. Flitsiyan, L. Chernyak, S. J. Pearton, and A. Kuramata, "Annealing of dry etch damage in metallized and bare (-201) Ga_2O_3," J. Vac. Sci. Technol. B **35**, 051201 (2017).
[98]J. Yang, S. Ahn, F. Ren, R. Khanna, K. Bevlin, D. Geerpuram, S. J. Pearton, and A. Kuramata, "Inductively coupled plasma etch damage in (-201) Ga_2O_3 Schottky diodes," Appl. Phys. Lett. **110**, 142101 (2017).
[99]J. E. Hogan, S. W. Kaun, E. Ahmadi, Y. Oshima, and J. S. Speck, "Chlorine-based dry etching of β-Ga_2O_3," Semicond. Sci. Technol. **31**, 065006 (2016).
[100]Z. A. Jian, Y. Oshima, S. Wright, K. Owen, and E. Ahmadi, "Chlorine-based inductive coupled plasma etching of α-Ga_2O_3," Semicond. Sci. Technol. **34**, 035006 (2019).
[101]C.-H. Lin, Y. Yuda, M. H. Wong, M. Sato, N. Takekawa, K. Konishi, T. Watahiki, M. Yamamuka, H. Murakami, Y. Kumagai, and M. Higashiwaki, "Vertical Ga_2O_3 Schottky barrier diodes with guard ring formed by nitrogen-Ion implantation," IEEE Electron Device Lett. **40**, 18937409 (2019).
[102]W. Li, Z. Hu, K. Nomoto, R. Jinno, Z. Zhang, T. Q. Tu, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, "2.44 kV Ga_2O_3 vertical trench Schottky barrier diodes with very low reverse leakage current," in *2018 IEEE International Electron Devices Meeting (IEDM)*, (IEEE, 2018), pp. 8.5.1–8.5.4.
[103]J. Yang, F. Renl, M. Tadjer, S. J. Pearton, and A. Kuramata, "2.3 kV Field-Plated Vertical Ga_2O_3 Schottky rectifiers and 1 a forward current with 650 V reverse breakdown Ga_2O_3 field-plated Schottky barrier diodes," in *2018 76th Device Research Conference (DRC)*, (IEEE, 2018), pp. 1–2.
[104]W. Li, Z. Hu, K. Nomoto, Z. Zhang, J.-Y. Hsu, Q. T. Thieu, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, "1230 V β-Ga_2O_3 trench Schottky barrier diodes with an ultra-low leakage current of >1 μA/cm^2," Appl. Phys. Lett. **113**, 202101 (2018).
[105]J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, and A. Kuramata, "High breakdown voltage (−201) β-Ga_2O_3 Schottky rectifiers," IEEE Electron Device Lett. **38**, 906–909 (2017).
[106]K. Sasaki, D. Wakimoto, Q. T. Thieu, Y. Koishikawa, A. Kuramata, M. Higashiwaki, and S. Yamakoshi, "First demonstration of Ga_2O_3 trench MOS-type Schottky barrier diodes," IEEE Electron Device Lett. **38**, 783–785 (2017).
[107]J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, J. Kim, and A. Kuramata, "High reverse breakdown voltage Schottky rectifiers without edge termination on Ga_2O_3," Appl. Phys. Lett. **110**, 192101 (2017).
[108]K. Konishi, K. Goto, H. Murakami, Y. Kumagai, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "1-kV vertical Ga_2O_3 field-plated Schottky barrier diodes," Appl. Phys. Lett. **110**, 103506 (2017).
[109]J. Yang, F. Ren, M. Tadjer, S. J. Pearton, and A. Kuramata, "Ga_2o_3 Schottky rectifiers with 1 ampere forward current, 650 V reverse breakdown and 26.5 MW cm^{-2} figure-of-merit," AIP Adv. **8**, 055026 (2018).
[110]M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Gallium oxide (Ga_2O_3) metal-semiconductor field-effect transistors on single-crystal β-Ga_2O_3 (010) substrates," Appl. Phys. Lett. **100**, 1–4 (2012).
[111]M. Higashiwaki, K. Sasaki, M. H. Wong, T. Kamimura, D. Krishnamurthy, A. Kuramata, T. Masui, and S. Yamakoshi, "Depletion-mode Ga_2O_3 MOSFETs on β-Ga_2O_3 (010) substrates with Si-ion-implanted channel and contacts," in *Technical Digest—International Electron Devices Meeting*, (IEDM, 2013), Vol. **3**, pp. 707–710.
[112]M. H. Wong, K. Sasaki, A. Kuramata, and S. Yamakoshi, "Field-Plated Ga_2O_3 MOSFETs With a breakdown voltage of over 750 V," IEEE Electron Device Lett. **37**, 212–215 (2016).
[113]M. Singh, M. A. Casbon, M. J. Uren, J. W. Pomeroy, S. Dalcanale, S. Karboyan, P. J. Tasker, M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, M. Higashiwaki, and M. Kuball, "Pulsed large signal RF performance of field-plated Ga_2O_3 MOSFETs," IEEE Electron Device Lett. **39**, 1572–1575 (2018).
[114]M. H. Wong, A. Takeyama, T. Makino, T. Ohshima, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Radiation hardness of β-Ga_2O_3 metal-oxide-semiconductor field-effect transistors against gamma-ray irradiation," Appl. Phys. Lett. **112**, 023503 (2018).
[115]L. Zhang, A. Verma, H. G. Xing, and D. Jena, "Inductively-coupled-plasma reactive ion etching of single-crystal β-Ga_2O_3," Jpn. J. Appl. Phys. **56**, 030304 (2017).
[116]Z. Jian, Y. Oshima, S. Wright, K. Owen, and E. Ahmadi, "Chlorine-based inductive coupled plasma etching of α-Ga_2O_3," Semicond. Sci. Technol. **34**, 035006 (2019).
[117]N. A. Moser, J. P. McCandless, A. Crespo, K. D. Leedy, A. J. Green, E. R. Heller, K. D. Chabak, N. Peixoto, and G. H. Jessen, "High pulsed current density β-Ga_2O_3 MOSFETs verified by an analytical model corrected for interface charge," Appl. Phys. Lett. **110**, 143505 (2017).
[118]K. D. Chabak, D. E. W. Jr, A. J. Green, A. Crespo, M. Lindquist, K. Leedy, S. Tetlak, N. A. Moser, and G. Jessen, "Sub-micron gallium oxide radio frequency field-effect transistors," in *2018 IEEE MTT-S International Microwave Workshop Series Advanced Materials and Processes RF THz Applications* (IEEE, 2018), pp. 1–3.
[119]A. J. Green, K. D. Chabak, M. Baldini, N. Moser, R. Gilbert, R. C. Fitch, G. Wagner, Z. Galazka, J. McCandless, A. Crespo, K. Leedy, and G. H. Jessen, "β-Ga_2O_3 MOSFETs for radio frequency operation," IEEE Electron Device Lett. **38**, 790–793 (2017).
[120]K. Zeng, A. Vaidya, and U. Singisetti, "A field-plated Ga_2O_3 MOSFET with near 2-kV breakdown voltage and 520 mΩ cm^2 on-resistance," Appl. Phys. Express **12**, 081003 (2019).
[121]Y. Zhang, A. R. Arehart, and S. Ringel, Appl. Phys. Lett. **113**, 123501 (2018).
[122]K. Zeng, A. Vaidya, and U. Singisetti, "1.85 kV breakdown voltage in lateral field-plated Ga_2O_3 MOSFETs," IEEE Electron Device Lett. **39**, 1385–1388 (2018).
[123]K. Chabak, A. Green, N. Moser, S. Tetlak, J. McCandless, K. Leedy, R. Fitch, A. Crespo, and G. Jessen, "Gate-recessed, laterally-scaled β-Ga_2O_3 MOSFETs with high-voltage enhancement-mode operation," in *2017 75th Annual Device Research Conference (DRC)*, (IEEE, 2017), Vol. **38**, pp. 1–2.
[124]K. D. Chabak, J. P. McCandless, N. A. Moser, A. J. Green, K. Mahalingam, A. Crespo, N. Hendricks, B. M. Howe, S. E. Tetlak, K. Leedy, R. C. Fitch, D. Wakimoto, K. Sasaki, A. Kuramata, and G. H. Jessen, "Recessed-Gate enhancement-mode β-Ga_2O_3 MOSFETs," IEEE Electron Device Lett. **39**, 67–70 (2018).
[125]S. Krishnamoorthy, Z. Xia, C. Joishi, Y. Zhang, J. McGlone, J. Johnson, M. Brenner, A. R. Arehart, J. Hwang, S. Lodha, S. Rajan, "Modulation-doped β-$(Al_{0.2}Ga_{0.8})_2O_3$/Ga_2O_3 field-effect transistor," Appl. Phys. Lett. **111**, 023502 (2017).
[126]Y. Zhang, Z. Xia, J. McGlone, W. Sun, C. Joishi, A. R. Arehart, S. A. Ringel, and S. Rajan, IEEE Trans. Electron Devices **66**, 1574 (2019).
[127]H. Okumura, Y. Kato, T. Oshima, and T. Palacios, "Demonstration of lateral field-effect transistors using Sn-doped β-$(AlGa)_2O_3$ (010)," Jpn. J. Appl. Phys. **58**, SBBD12 (2019).
[128]S. Krishnamoorthy, Z. Xia, S. Bajaj, M. Brenner, and S. Rajan, "Delta-doped β-gallium oxide field-effect transistor," Appl. Phys. Express **10**, 051102 (2017).
[129]K. Ghosh and U. Singisetti, "Ab initio velocity-field curves in monoclinic β-Ga_2O_3," J. Appl. Phys. **122**, 035702 (2017).

[130]K. A. Mengle, G. Shi, D. Bayerl, and E. Kioupakis, "First-principles calculations of the near-edge optical properties of β-Ga_2O_3," Appl. Phys. Lett. **109**, 212104 (2016).
[131]N. Ma, N. Tanen, A. Verma, Z. Guo, T. Luo, H. G. Xing, and D. Jena, "Intrinsic electron mobility limits in β-Ga_2O_3," Appl. Phys. Lett. **109**, 212101 (2016).
[132]Y. Zhang, Z. Xia, C. Joishi, and S. Rajan, "Design and Demonstration of $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ Double Heterostructure Field Effect Transistor (DHFET)," in *Device Research Conference—Conference Digest, DRC*, (IEEE, 2018), Vol. 2018, pp. 1–2.
[133]H. Zhou, K. Maize, G. Qiu, A. Shakouri, and P. D. Ye, "β-Ga_2O_3 on insulator field-effect transistors with drain currents exceeding 1.5 A/mm and their self-heating effect," Appl. Phys. Lett. **111**, 092102 (2017).
[134]M. H. Wong, K. Goto, A. Kuramata, S. Yamakoshi, H. Murakami, Y. Kumagai, and M. Higashiwaki, "First demonstration of vertical Ga_2O_3 MOSFET: Planar structure with a current aperture," in *2017 75th Annual Device Research Conference (DRC), 25–28 June 2017* (IEEE, South Bend, IN, 2017).
[135]B. Chatterjee, K. Zeng, C. D. Nordquist, U. Singisetti, and S. Choi, "Device-Level thermal management of gallium oxide field-effect transistors," IEEE Trans. Compon. Packag. Manuf. Technol. (published online).
[136]K. Kaneko, S. Fujita, and T. Hitora, "A power device material of corundum-structured α-Ga_2O_3 fabricated by MIST EPITAXY® technique," Jpn. J. Appl. Phys. **57**, 02CB18 (2018).
[137]K. Akaiwa, K. Kaneko, S. Fujita, E. Chikoidze, and Y. Dumont, "Room temperature ferromagnetism in conducting α-$(In_{1-x}Fe_x)_2O_3$ alloy films," Appl. Phys. Lett. **106**, 062405 (2015).
[138]K. Harafuji, T. Tsuchiya, and K. Kawamura, "Molecular dynamics simulation for evaluating melting point of wurtzite-type GaN crystal," J. Appl. Phys. **96**, 2501–2512 (2004).