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A Gate Programmable van der Waals Metal-Ferroelectric-Semiconductor Vertical Heterojunction Memory

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Ferroelectricity, one of the keys to realize non-volatile memories owing to the remanent electric polarization, is an emerging phenomenon in the 2D limit. Yet the demonstrations of van der Waals (vdW) memories using 2D ferroelectric materials as an ingredient are very limited. Especially, gate-tunable ferroelectric vdW memristive device, which holds promises in future multi-bit data storage applications, remains challenging. Here, a gate-programmable multi-state memory is shown by vertically assembling graphite, $CuInP_2S_6$, and MoS_2 layers into a metal(M)-ferroelectric(FE)-semiconductor(S) architecture. The resulted devices seamlessly integrate the functionality of both FE-memristor (with ON–OFF ratios exceeding 10^5 and long-term retention) and metal-oxide-semiconductor field effect transistor (MOS-FET). Thus, it yields a prototype of gate tunable giant electroresistance with multi-levelled ON-states in the FE-memristor in the vertical vdW assembly. First-principles calculations further reveal that such behaviors originate from the specific band alignment between the FE-S interface. Our findings pave the way for the engineering of ferroelectricity-mediated memories in future implementations of 2D nanoelectronics.

1. Introduction

The phenomenon of switchable electro-resistance between ON and OFF states in a metal-insulator-metal (MIM) junction, often facilitated by the formation/deformation of conduction paths through filaments upon application of voltages,[1] has been an endeavor toward industrial manufacturation of resistive random access memories (ReRAM, deemed also as memristors). Conventionally, such resistive switching behaviors are preferably realized in a two-terminal device in the tunneling regime, with the insulator in the MIM junction being a high-k dielectric material.[2] Notably, by substituting the dielectric layer with ferroelectric or multi-ferroic ones, a family of memristors can be established, with their tunneling electro-resistance

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(TER) inheriting the ferroic-characteristics and exhibiting enhanced tunability of the tunneling barriers.[3–9]

Recently, routes have been developed either to boost the performance or to exploit distinct mechanisms of the memristive devices.[10–12] Among them, vdW devices are of particular promises, as they can be interfaced free of lattice-matching and compatible with a diversity of functionalities.[13,14] For example, it is demonstrated that memristive behaviors can be observed in vdW devices in both the tunneling[15] and the diffusive regimes.[16,17] The latter scenarios can be realized with certain mediations (such as ion-migration,[16] grain boundaries,[17] and ionic-gate induced phase transition[18]), while the channels are often laterally arranged with lengths exceeding a few micron meters. The atomically thin lateral semiconducting conduction channel thus enables further gate tunablility,[19] which leads to multiterminal memtransistors that mimic synaptic responses upon training voltage pulses, holding promises in future neuromorphic computing.[20–23] Besides, compared to lateral memtransistors, vertically assembled memtransistors are more compatible for industrial production thanks to its relatively small footprint.[24] To date, studies of vdW memtransistors, however, remain limited, and especially, vertically assembled gate-tunable memristive device with a specific architecture of M-FE-S has been missing.

In this work, we utilize the vdW vertical assembly as a platform to devise a prototype gate-programmable memory by stacking few-layers of graphene, $CuInP_2S_6$, and MoS_2 into a metal-ferroelectric-semiconductor (M-FE-S) architecture, with the top semiconducting layer simultaneously equipped into a MOS-FET, with the gate dielectric being few-layered hexagonal boron nitride (h-BN). Consequently, when the top gate is not at play, the resulted devices exhibit two-terminal switchable electro-resistance with ON-OFF ratios exceeding 10^5 and long-term retention, akin to a conventional memristor but strongly coupled to the ferroelectric characteristics of the $CuInP_2S_6$ layer, while its memristor can be killed by heating the system above the ferroelectric transition Curie temperature of $CuInP_2S_6$. Interestingly, the obtained memristive characteristics can be quenched (enabled), by setting the Fermi level of MoS_2 inside (outside) of its band gap using the top gate at room temperature, yielding a three-terminal gate programmable non-volatile vdW memory. By first-principles calculations, we attribute this phenomenon to a ferroelectric field effect, which significantly modifies the band alignment at the FE-S interface. The proposed three-terminal non-volatile vdW M-FE-S memory exhibit gate programmable multi-levelled ON-states, and thus can, in principle, be trained into artificial synapses, shedding light on the design of ferroelectric-mediated memories in future nanoelectronics.

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2. Results

2.1. Fabrication and Characterizations of M-FE-S Memristors.

The schematic illustration of M-FE-S memristor is shown in **Figure 1**a, with a typical sample shown in Figure S1 (Supporting Information). In this work, multilayer graphene (or graphite) flakes used as bottom electrodes here are insensitive to gate electrical field (Figure S2, Supporting Information). The scheme of monolayer graphene coupled with the ferroelectric 2D materials has already been investigated by previous studies.[12] Here, we take a different route in our system: other than taking advantage of the gate-tunable carrier density of monolayer graphene, we utilize the 2D semiconductor with a band gap (MoS_2 in our case) to construct the M-FE-S vertical junction, in which graphite is a metallic electrode as the "M" part. And the key role of MoS_2 is that its Fermi level can be gate tuned outside/inside the bandgap, allowing the realization of a unique gate-programmable M-FE-S memory by the specific band alignment between MoS_2 and $CuInP_2S_6$, as supported by the DFT simulations. Using the dry-transfer method,[25] multi-layered vdW heterostructure was fabricated by stacking few-layers of graphene, $CuInP_2S_6$, MoS_2, and hexagonal boron nitride (h-BN), with a graphite layer (5–10 nm in thickness) serving as the bottom electrode (see Figure S3, Supporting Information). Electrodes and top gates were patterned via standard lithography and electron-beam evaporation. Raman spectroscopy of $CuInP_2S_6$ and MoS_2 layers were measured to confirm the phonon modes of each crystal, as shown in Figure S4 (Supporting Information). It is seen that both of the two materials exhibit consistent Raman peaks as compared to the previous reported results.[26,27] It is noteworthy that the anion and cation peaks can be found in the Raman spectrum of $CuInP_2S_6$, indicating the existence of ferroelectric dipole polarization at room temperature in the flake. Indeed, Curie temperature T_C of few-layered $CuInP_2S_6$ is ≈315 K.[28] It is noticed that in order to effectively tune the carrier density of the semiconducting layer (few-layered MoS_2, for example), the underneath ferroelectric layer has to be thick enough to avoid leakage and to allow a well defined chemical potential in the MoS_2 layer. It is known that ferroelectric tunnelling memory was reported recently,[15] where a 4-nm-thick $CuInP_2S_6$ layer was used to form a simple M-FE-M tunnel junction. However, as mentioned above, such structure cannot be compatible with gate-tunability. Therefore, $CuInP_2S_6$ flakes with thicknesses of 30–50 nm were used to fabricate the M-FE-S junctions in the current study to retain their dielectric properties. On the other hand, thick $CuInP_2S_6$ (above 80 nm in thickness) used as a ferroic dielectric together with

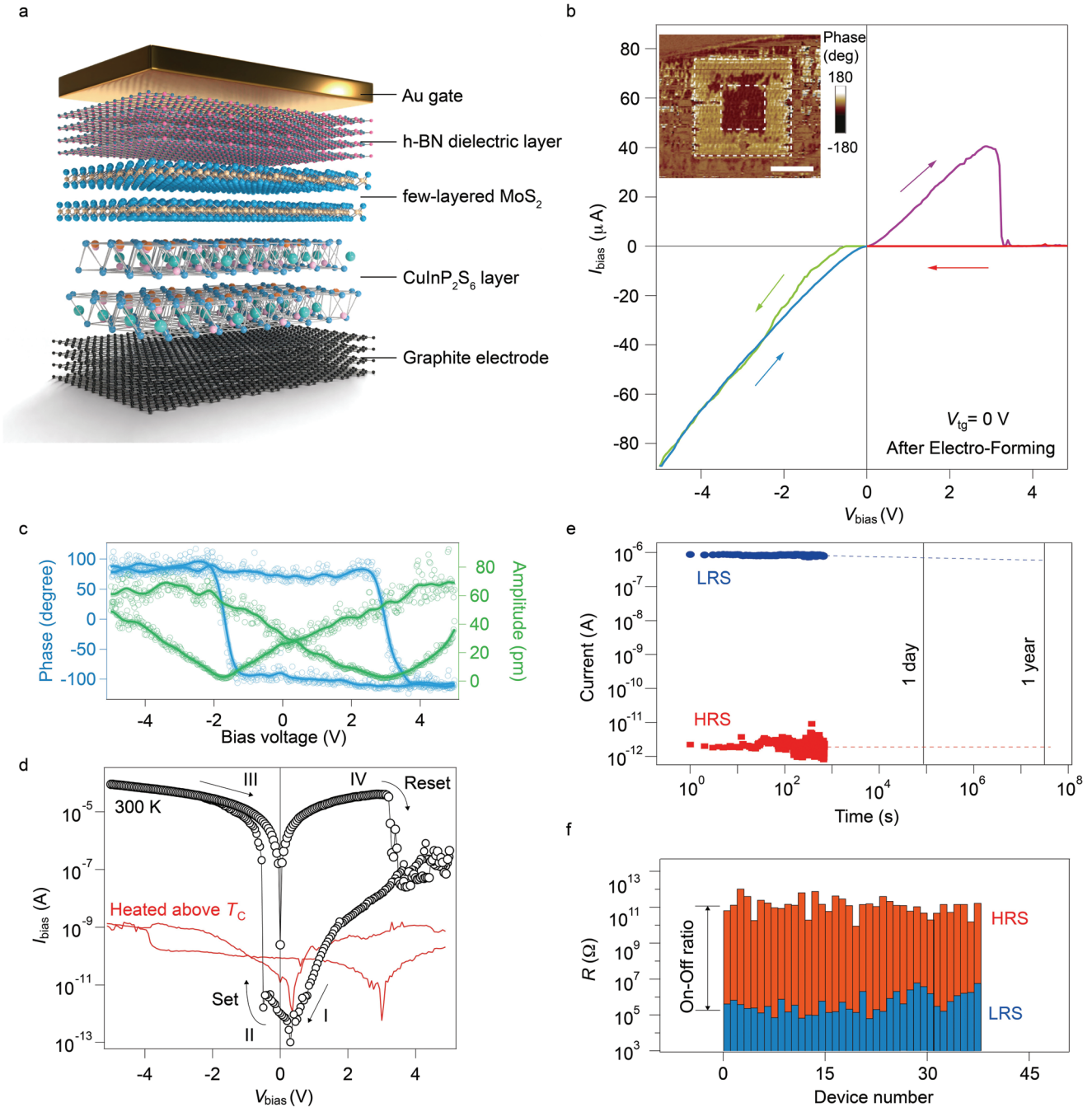

Figure 1. Characterizations of vdW M-FE-S heterojunctions. a) Schematic illustration of M-FE-S memristor. b) A typical pinched *I–V* curve obtained in a vdW M-FE-S heterojunction, showing characteristic memristive behavior. Inset in (b) shows the PFM phase image for a typical $CuInP_2S_6$ flake (thickness $t \approx 50$ nm) with written box-in-box pattern with reverse DC bias. Scale bar is 2 μm. c) Out-of-plane amplitude and phase curves as a function of bias voltage obtained by PFM on a typical $CuInP_2S_6$ flake with $t \approx 40$ nm. d) Looped *I –V* characteristics in a log-scale showing typical resistive switching behaviour, as presented by the curve of open circles. Directions of the sweep are indicated by arrows, with four distinct stages. The device is reset to HRS during stage IV at certain positive V_{bias}, and set to LRS during stage II at certain negative V_{bias}. The device shows absence of memristive performance when heated above T_C, as shown in the red curve. e) Retention time of a typical device measured at $V_{read} = 0.5$ V after applying a 100 μs voltage pulse of $V_{bias} = 4.0$ V (- 4.0 V) to set the OFF (ON) state. f) Statistics of HRS and LRS states measured in more than 30 different samples. Voltage pulses of 100 μs were used to set the OFF (ON) states. Average ON/OFF ratio is estimated to be $\approx 10^5$.

an internal graphene gate has been adopted in fabricating long retention FE memristor, which is very different from our architecture.[29]

We now characterize the two-terminal electro-resistance in the as-prepared M-FE-S junctions (i.e., the FE-memristors). During the electrical measurements, the top gate and the MoS_2

layers were kept grounded, while bias voltages were applied on the graphite (or few-layered graphene, FLG) layer. As shown in Figure 1b, looped $I-V$ characteristics of a representative device is plotted, with the sweep-directions indicated by arrows. This pinched I–V loop is a typical resistive switch curve, with four distinct stages indicated by different colors. Specifically, the device is switching between a high resistance state (HRS) and a low resistance state (LRS) with a hysteresis that is depending on the sweeping direction and maximum polarization voltage. Multiple devices exhibit consistent behavior, as shown in Figure S5 (Supporting Information). We attribute this resistive behavior to the formation of conduction paths in the $CuInP_2S_6$ layer, as the devices all undergo an electro-forming process before they can serve as memristors, shown in Figure S6 (Supporting Information).

2.2. Ferroelectric Characteristics of the M-FE-S Memristor.

In the following, we demonstrate that the fabricated M-FE-S memristors are strongly coupled to the ferroelectric properties of the few-layered $CuInP_2S_6$. First, it is worth mentioning that the electrical resistance of the M-FE-S junctions might be dominated by the Schottky barrier at the FE-S interface, which is carefully discussed in the Figure S7 (Supporting Information). Piezoresponse force microscopy (PFM) is used to characterize the ferroelectricity of the $CuInP_2S_6$ flakes. The ferroelectric domains of a box-in-box pattern of a typical $CuInP_2S_6$ flake can be seen in the phase image in the inset in Figure 1b, with more details in Figure S8 (Supporting Information). Furthermore, out-of-plane amplitude (green) and phase (blue) obtained on a typical $CuInP_2S_6$ flake with $t \approx 40$ nm, exhibiting hysteresis loops with asymmetric coercivity fields biased toward positive voltages, as shown in Figure 1c. Such biased polarization-switching fields are also seen in previous reports.[28,30,31] We notice that for Cr/$CuInP_2S_6$/FLG devices, there is no distinct resistive switching behavior in the diffusive regime, as shown in Figure S9 (Supporting Information). Besides, negligible resistive switching behavior is present in other similar M-FE-M structures, e.g. Au/$CuInP_2S_6$/Au and Cr/$CuInP_2S_6$/Au, indicating that the resistive switching behavior is related to the FE-S interface, shown in Figures S10 and S11 (Supporting Information).

Interestingly, the switching voltages (≈–1.0 and +2.5 V for each polarization directions) in $CuInP_2S_6$ in Figure 1c are inherited by the resistive switching I–V curve in the M-FE-S memristor with similar thickness of $CuInP_2S_6$, as plotted in a log-scaled looped I–V in Figure 1d (as typical linear I–V data is shown in Figure 1b). Four distinct stages along with the sweeping-up and down directions are indicated by arrows in Figure 1d. At the vicinity of positive switching voltage (V_{bias}) of the peizoelectric loop in Figure 1c, the M-FE-S memristor device is "reset" to HRS during stage IV. On the contrary, the device is "set" to LRS during stage II at the vicinity of negative switching voltage. It is worth noted that the voltage differences between "set" and "reset" coincidence well with the differences between polarization-switching voltages of $CuInP_2S_6$,[30] as shown in the Figure S12 (Supporting Information). Mechanism of the observed ferroelectricity-assisted FE-S memristive behavior can be attributed to the formation of conduction paths in the $CuInP_2S_6$ layer, and a modulation of band alignment at the FE-S interface, leading to a tunable interfacial barrier induced by the ferroelectric polarization similar to the scenario of tunneling FE-memristors,[8] but in our case, the FE layer is in the bulk limit. Detailed analysis of the band alignment will be discussed in the coming text.

Moreover, since the T_C of the few-layered $CuInP_2S_6$ studied in this work is ≈315 K, it is crucial to test the M-FE-S memristors above T_C. As expected, the resistive switching of the same device is quenched when heated at 400 K, as shown in the red looped I–V curve in Figure 1d. Even when cooled to room temperature, no memristive behavior was observed, suggesting that the memristive behavior of the M-FE-S device is strongly coupled to the ferroelectric nature of $CuInP_2S_6$, since ferroelectric domains become randomly distributed when the system is naturally cooled down from above T_C. The resistive switching thus may require a ferroelectric domain training process in the system, similar to the initial magnetization process in some hard ferromagnets.[32] Indeed, by re-doing the electro-forming process, the absence of memristive performance can be recovered in those annealed samples, as illustrated in Figure S13 (Supporting Information).

2.3. Performances of Two-Terminal Electro-Resistances in vdW M-FE-S Memristors.

As shown in Figure S14 (Supporting Information), two-terminal I–V curves between –0.4 and 0.4 V in the ON and OFF states. Both are nonlinear, and consecutively tuned from negative to positive V_{bias} for each states, which differ from the grain-boundary mediated resistive switching devices,[17] but resembles the behavior of other TER memristors.[33] It is noticed that the devices may be permanently damaged due to dielectric breakdown at V_{bias} higher than 6.0 V (more details can be found in Figure S15, Supporting Information).

Figure 1e shows resistance versus time of a two-terminal M-FE-S device measured at $V_{read} = 0.5$ V after applying a 100 µs voltage pulse of $V_{bias} = 4.0$ V (–4.0 V) to set the OFF (ON) states. The devices show retention time which can be extrapolated to the time scale of years, with the attenuation of ON/OFF ratio less than one order of magnitude. By measuring HRS and LRS states in more than 30 different samples (data collected with setting-resetting voltage pulses of 100 µs with amplitudes of ±4.0 V) are shown in the statistics in Figure 1f. It is seen that good reproducibility can be obtained in all tested samples, with an average ON/OFF ratio of $\approx 10^5$, and the ON-state current is orders of magnitudes higher than the M-FE-M junctions using thin or thick $CuInP_2S_6$ layers.[28,34] It is noticed that among the measured M-FE-S samples, thicknesses of the ferroelectric and semiconducting layers are in the range of 30–50 nm and 5–15 nm, respectively. The variation of thicknesses among samples may be a cause of the fluctuation of ON/OFF ratios observed.

Based on the above mentioned high performance of standalone M-FE-S devices, we further demonstrated the feasibility of M-FE-S memory arrays, which is a key structure for realizing random access memory (RAM), as illustrated in **Figure 2**a. At each cross point between the bit and word lines, the vdW

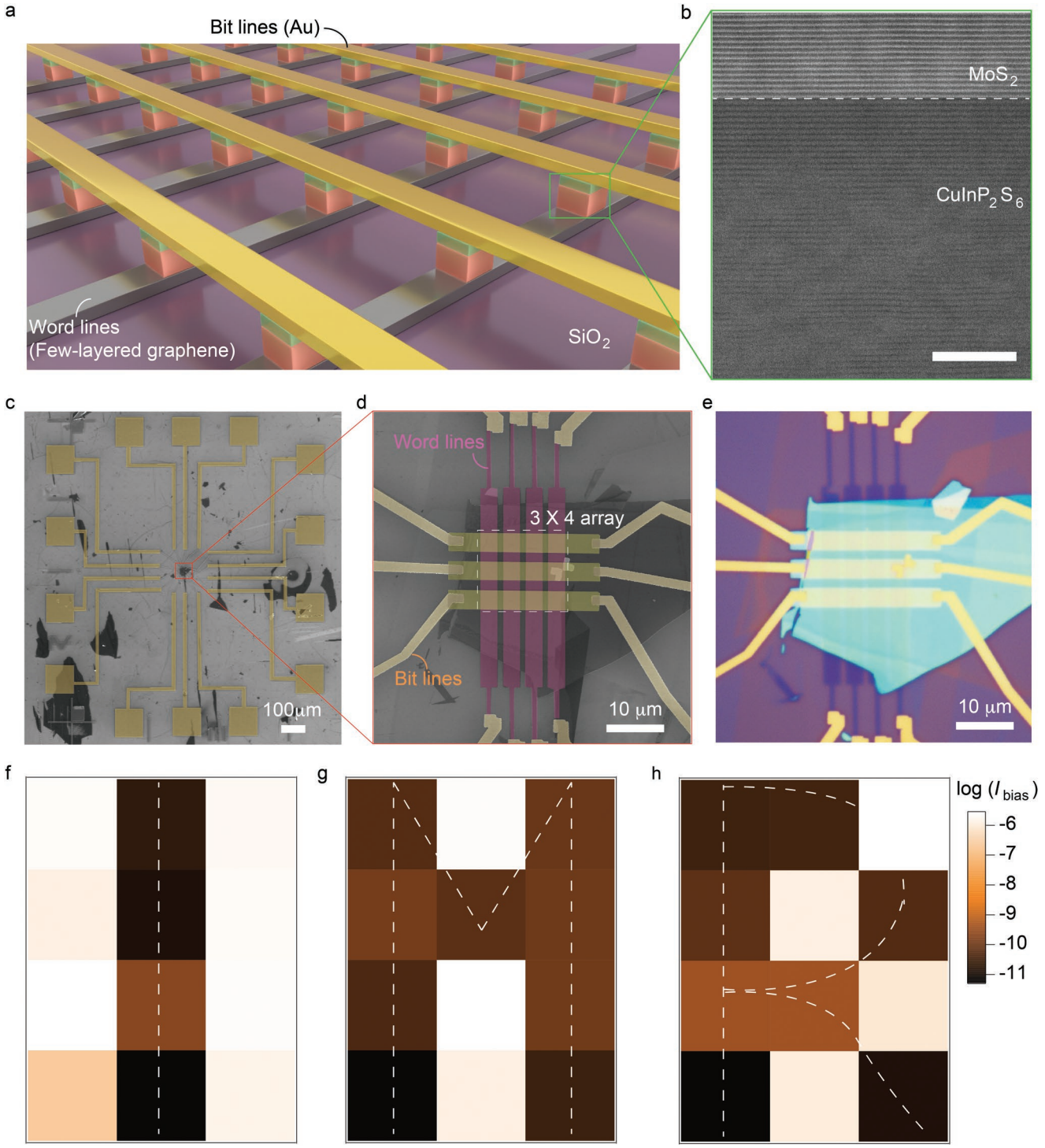

Figure 2. Ferroeletricity-assisted resistive switching behavior in vdW M-FE-S heterojunction arrays. a) Cartoon illustration of M-FE-S memory arrays, which is a key structure for realizing random access memory. b) HAADF-STEM image of the cross section of a typical cross-section of the FE-S interface consisted of vdW layers of MoS_2 and $CuInP_2S_6$. Scale bar is 10 nm. c,d) False colored SEM images of a typical M-FE-S array device. e) Optical image of the same region of the device as shown in (d). f–h) Simplified letters of "I", "M", and "R" encoded by reading the LRS and HRS of each pixel in the 3 × 4 array.

M-FE-S junction is formed. As shown in Figure 2b, the atomic resolution of such a typical cross section can be seen in the high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image. It is seen that the layered structures of $CuInP_2S_6$ and MoS_2 are well defined, and the FE-S interface is atomically sharp. Typical 3 × 4 cross-bar M-FE-S array device is shown in the false-colored scanning electron microscope images in Figure 2c,d, with

the corresponding zoomed-in area shown also in the optical micrograph image in Figure 2e. Using the set and reset voltage for stand-alone devices discussed previously, the switching ratios for the crossbar are in the order of 10^5. By programing the corresponding M-FE-S devices in the array into potentiation (LRS) or depression (HRS) state with polarization voltage $V_{pole} \approx \pm 4$ V pulses of 100 ms width, the pattern writing process is realized. The memorized letters can then be read with a 1 V bias voltage, with example letters "I", "M", and "R" encoded into 3×4-pixel images and stored, shown in Figure 2f–h. This speaks the high reproducibility of the performances in the M-FE-S memristors.

3. Discussion

To this stage, we have demonstrated the subpart of the as-prepared vertical vdW heterojunction, i.e., the M-FE-S junction that serves as a two-terminal FE-memristor. Now, we come to the discussion of the MOS-FET equipped on the top part of the heterojunction illustrated in **Figure 3**a. One of the key roles of the architecture adopted here is that the vdW semiconductor in the M-FE-S junction can be gated to tune the carrier density (or, the Fermi level) in the semiconductor itself, further affecting the memristive performance as a consequence. As shown in Figure 3b, field effect in the few-layered MoS_2 in a typical sample is confirmed and the leakage current is shown in Figure S16 (Supporting Information). The threshold voltage of the ON-state of the FET is ≈ −4 V, below which the MoS_2 is tuned into gapped region where no density of states (DOS) is available. The general FET behavior of few-layered MoS_2 crystals in this work is in agreement with previously reported results.[35] More details on the threshold voltages of the ON-state of MoS_2 flakes with thickness ≈10 nm can be found in Figure S17 (Supporting Information). Two representative gate voltages were chosen to pin the Fermi level of MoS_2 at the position of inside the conduction band (C.B.), at the bottom of C.B., and in the bandgap (between C. B. and the valence band, V. B.), as indicated by green and red cartoons along with corresponding dots in the inset of Figure 3b.

To address the mechanism of the observed gate-programmable features in the memristors, we performed systematic first priciples calculations, as discussed in Figures S18–S21 (Supporting Information). To briefly sketch it, we show illustrations of the band-alignments in Figure 3c,d. When the Fermi level of the semiconducting MoS_2 layer is set into the conduction band, the electrons can be transported between source and drain, leading to the enabling of the memristive performance. In this scenario, the direction of ferroelectric polarizations in the M-FE-S structure will effectively form a band bending and lead to a extra barrier for electrons to migrate when the ferroelectric polarization is pointing against the semiconducting layer, setting the system to the HRS, and vice-versa. Notice that the bulk nature of the FE layer in our system is essential, as such physical progress will not persist in the thin tunneling case. When the Fermi level of the semiconducting MoS_2 layer is set into the gapped region, the DOS are diminished between the chemical potential window of source and drain, thus the device exhibits negligible conductance in general and the memristive behavior is quenched, regardless of the direction of ferroelectric polarizations in the M-FE-S structure, shown in Figure 3d.

One of the key findings in this work is that the unique vertical architecture of M-FE-S vdW heterostructure allows us to seamlessly integrate the functionalities of MOSFET and FE-memristor in a single device. In this manner, one can readily set the Fermi level of MoS_2 with a finite yet programmable density of states, and thanks to the specific band alignment between MoS_2 and CIPS (as discussed in our DFT calculations), a multi-leveled memory can be realized, providing a promising platform for future implementations such as neuromorphic nanoelectronics. Moreover, the existing of a band gap in MoS_2 can further facilitate the unprecedented quenchable memristive behavior as will be discussed in **Figures** 3e,f and **4**. To systematically investigate the memristive behaviors at different gate voltages, we have tested the gate tuned memory windows in multiple devices and all devices show similar behaviors. As shown in Figure S22 (Supporting Information), the switching window shrinks notably when the carrier density in the MoS_2 layer decreases, suggesting gate programmable resistive switching behavior in the devices. The switching window extracted from seven typical samples as a function of gate voltage is shown in Figure S23 (Supporting Information). Besides, to further verify gate programmable ferroelectric resistive switching behavior, the resistances (read at 1.0 V) versus voltage pulse (V_{Pole}) were tested by pulse-voltage tests that is a standard protocol for characterizing ferroelectric resistive switching memories,[36,37] where successive values of V_{Pole} are applied from 0 V to −4.5 V, −4.5 V to 4 V, and 4 V to 0 V, and the pulse duration is 50 ms and interval is 10 ms, see Figure S24 (Supporting Information). A clear hysteretic variation of the resistance state with V_{Pole} is observed, indicating the non-volatile resistance switching in our device, see Figure S25 (Supporting Information). Indeed, it is seen that by tuning the V_g, the memristive characteristics of the device can be programmed into disabled- and enabled-states, as shown in Figure 3e,f, respectively. Detailed analysis of the leakage current of the M-FE-S devices can be found in Figures S26 and S27 (Supporting Information).

We show in Figure 4a–d the demonstration of the gate-programmable multi-leveled ON-states of another typical M-FE-S memory sample. It is seen that the memory windows can be largely tuned from disabled to a number of intermediate states from V_g = −6 to 6 V, and the ON-state current gradually saturates at higher V_g. Figure 4e exhibits the pulses of I_{bias} read at $V_{bias} = +0.8V$ in the sequence of pulse numbers at different gate voltages. Each memory window is controlled with different writing voltages (i.e., V_g = −5, −4, ..., 0 V) and a fixed erasing voltage (i.e., V_g = −6 V). More memory operation datas are shown in Figures S28 and S29 (Supporting Information). Finally, the performance of the gate endurance (ON-states switched between V_g = −5 and 0 V) is shown in Figure 4f, within 10^3 cycles, the general gate programmed behavior does not change. The gate-programmable feature of the as-prepared M-FE-S memories is key for future engineering of such as artificial synapses and may trigger the exploit of exotic functionalities based on ferroelectric 2D materials. Furthermore, the picture of principle-of-work in our devices can be further expanded into vertical vdW heterojunctions with a broader family of 2D materials.

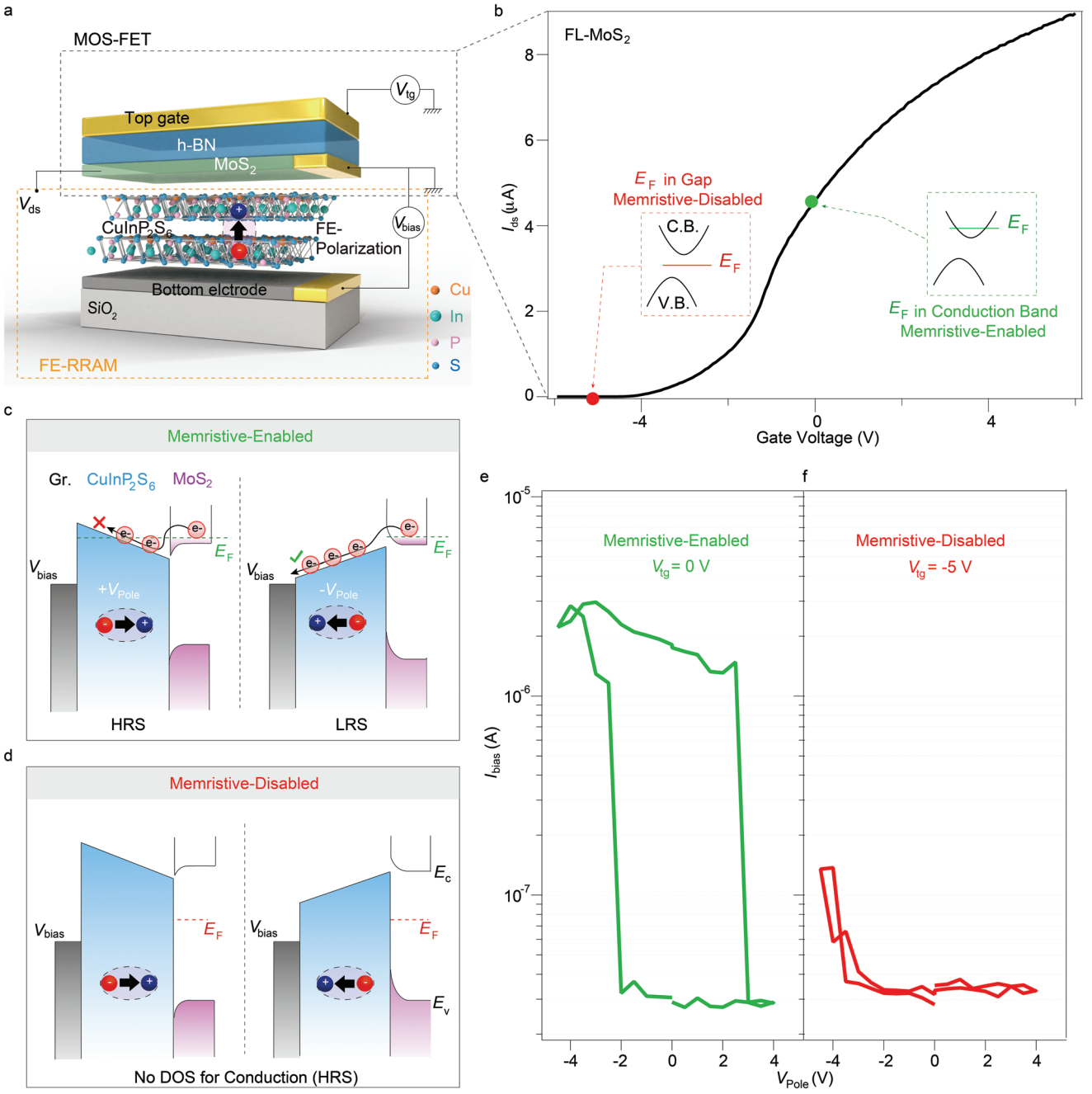

Figure 3. Principle of quenching and enabling the FE-memristive characteristics via gating. a) Art view of the vdW vertical assembly that integrates the functionality of FE-memristor and MOS-FET. b) Field effect curve of few-layered MoS_2, measured on a typical MoS_2 flake with similar thickness in the tested M-FE-S memristor. Illustration of conduction and valence bands with the Fermi energy were given in the insets, for two typical memristive-enabled (green) and disabled (red) states, respectively. E_F denotes the Fermi level. c,d) Band alignments of the metal-ferroelectric-semiconductor heterojunction. The memristive-disabled and memristive-enabled regimes are realized by adjusting the Fermi energy MoS_2 inside the gap, and in the electron side, respectively. e,f) The memory windows (i.e., Resistance versus pulse-voltage loop) measured at different Fermi energies of the MoS_2 layer, set by the top gate V_g. I_{ds}, and I_{bias} are distinguished for the source-drain voltage in the MOS-FET and the FE-memristor, respectively.

To conclude, we devised a conceptual nano architecture that fuses ferroelectric memristor and MOS-FET, using van der Waals vertical assembly as a platform. Experimentally, the devices were constructed by sequentially stacking few-layers of graphene, $CuInP_2S_6$, MoS_2, and h-BN from bottom to top. In this manner, the conjugated nanostructure can pack memristor and MOSFET into one single device, as the fine-tuning of Fermi level in the semiconducting layer can simultaneously affect the resistive switching behavior of the M-FE-S junction. When performed as conventional two-terminal memristors, the M-FE-S devices show resistive switches with ON-OFF ratios reaching 10^5 and state-of-the-art retention time for information

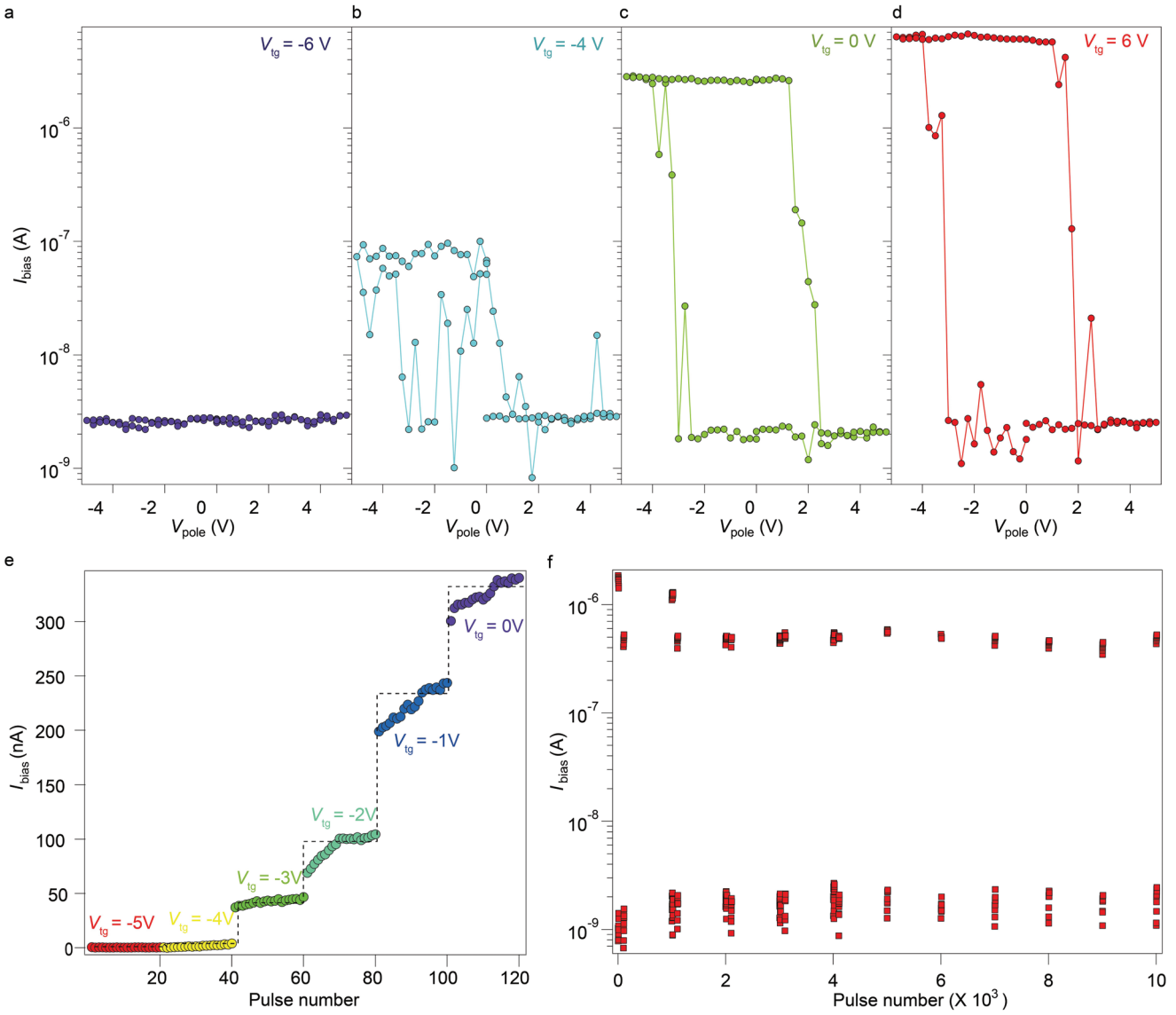

Figure 4. Multi-bit data storage of vdW M-FE-S gate-programmable memory at room temperature. a–d) The demonstration of the gate-programmable multi-levelled ON-states in the memory windows of a typical M-FE-S sample. e) When tuning the gate voltages, I_{bias} at reading voltage of 0.8 V is plotted against the sequence of pulse numbers. f) Shows the gate endurance performance of a typical sample, with the ON-states switched between V_g = −5 and 0 V.

storage. The obtained memristive characteristics are strongly coupled to the ferroelectric nature of $CuInP_2S_6$, and can be further programmed, using the top gate at room temperature, into quenched- or multi-leveled enabled-states. The resulted three-terminal gate programmable non-volatile vdW M-FE-S memory is a potent platform for the design of future ferroelectric-mediated vdW memories, which may find applications in such as neuromorphic computing.

4. Experimental Section

Sample Fabrication: vdW few-layers of the M-FE-S junctions were obtained by mechanically exfoliating high quality bulk crystals. The vertical assembly of vdW-layered compounds were fabricated using the dry-transfer method in a nitrogen-filled glove box. Electron beam lithography was done using a Zeiss Sigma 300 SEM with an Raith Elphy Quantum graphic writer. Top gates as well as contacting electrodes were fabricated with an e-beam evaporator, with typical thicknesses of Cr/Au ≈ 5/50 nm.

TEM Characterizations: TEM characterizations were carried out on a double aberration corrected FEI Themis G2 60-300 electron microscope equipped with a SuperX-EDS detector and operated at 300 kV. Cross sections of as-prepared devices were made using a focused ion beam tool of FEI Helios PFIB CXe cut at 30 kV and polished at 30 and 12 kV.

Morphology Tests: A Bruker Dimension Icon AFM was used for thicknesses and morphology tests, as well as PFM characterizations. Optical images were collected by a Nikon LV-ND100 microscope.

Electrical Measurements: The high precision of current measurements of the devices were measured using a Cascade M150 probe station at room temperature, with an Angilent B1500A Semiconductor

Device Parameter Analyzer. Gate voltages on the as-prepared multi-terminal memristors were fed by a Keithley 2400 source meter. During measurements, the TMD layer was kept grounded, while the V_{bias} was applied on the graphite bottom electrode. It was noticed that if the configuration of source-drain was reversed, the *I–V* characteristics would be reversed accordingly (Figure S30, Supporting Information). For the memory window measurement in Figure 4 in the main text, a pulse train constraints varying program pulse and constant read pulse (1.0 V) was adopted by using the waveform generator fast measurement unit (WGFMU).The program voltage ranged from −4.5 V to 4.0 V at a step of 0.5 V.The pulse duration was 50 ms and interval was 10 ms.

First-Principles Calculations: The first-principles calculations were carried out by the plane-wave package PWmat that implemented in graphics processing units (GPUs).[38] The SG15 seudopotential was adopted,[39] and the cutoff energy was set to 55 Ry. A supercell of $CuInP_2S_6$-MoS_2 interface was constructed by minimizing the mean lattice strain to as low as 2.45%. It contained 3 layers of $CuInP_2S_6$ and 3 layers of MoS_2, and a vacuum layer of 14.5 Å. The cross section of the orthogonal supercell was 12.64 Å× 10.95 Å. For this large supercell, only the Gamma point was sampled for structural relaxation (forces converge to 0.01 eV $Å^{-1}$) and electronic structure calculation. The HSE hybrid functional was used to correct the bandgap of $CuInP_2S_6$ and MoS_2 to 2.90 and 1.35 eV, respectively.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

W.L. and Y.G. contributed equally to this work. Z.H., H.W., and C.Z. conceived the experiment and supervised the overall project. W.L., Y.G., and H.W. fabricated the devices and carried out electrical transport measurements; Y.L., L.W., and Z.W. performed first-principles calculations. K.W. and T.T. provided high quality h-BN bulk crystals. W.H. and L.Y grew the bulk $CuInP_2S_6$ crystal. H.W. and Z.H. analyzed the data, with W.L., Y.G., T.A., and C.Z. participated in. Z.L., X.L., B.H., and P.G. performed TEM characterizations. X.Z., S.W., and J.C. carried out resistance versus pulse-voltage loop measurements. The manuscript was written by Z.H., H.W., and W.L. with discussion and inputs from all authors.

Data Availability Statement

The data that support the findings of this study are available at Zenodo, https://doi.org/10.5281/zenodo.7316549.

Keywords

2D ferroelectrics, array, memristive device, multi-bit storage, van der waals heterostructures

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