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Reconfigurable Ternary Logic-In-Memory With Organic Antiambipolar Transistor

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ABSTRACT

We developed a reconfigurable ternary logic-in-memory (LIM) device based on an organic antiambipolar transistor and incorporating a gold floating gate into a hafnium oxide (HfO_2) gate insulator. First, a standard ternary inverter was obtained with extremely low input and drain voltages (2 V) owing to the high dielectric constant of the HfO_2 gate insulator. Three distinct output logic states ("2," "1," and "0") were clearly obtained for the corresponding input logic states ("0," "1," and "2"). Then, the voltage transfer curve was laterally shifted up to 1.8 V by controlling the hole- and electron-injection processes into the floating gate, obtaining a ternary nonvolatile memory. This memory function realized versatile reconfigurable ternary inverter operations. Three ternary inverters, namely, standard, negative, and positive ternary inverters, were demonstrated in a single LIM device. Remarkably, these inverter operations were performed using the same input voltages and then electrically reconfigured by adjusting the charge condition (i.e., holes or electrons) of the floating gate. Our development seems promising for performing multivalued in-memory computing toward surpassing the capabilities of existing von Neumann systems.

1 | Introduction

The development of high-performance organic integrated circuits (ICs) is gaining increasing attention owing to the emergence of edge artificial intelligence and Internet-of-Things systems given the benefits of organic materials, including mechanical flexibility, light weight, low-cost production, and biocompatibility [1–5]. Many efforts have been devoted to interactive mobile and wearable applications, with representative examples including radiofrequency identification tags, wearable displays, security devices, and healthcare sensors [6–10]. In such applications, organic ICs are often used as flexible amplifiers and analog-to-digital converters for real-time processing of signals from versatile sensors and actuators. However, organic ICs remain constrained by their low integration density and poor processing owing to incompatibility with conventional lithography techniques [1–4]. The typical integration density of organic transistors remains as low as ~100 transistors per cm^2 [1, 4, 5]. Although relatively high integration densities of up to ~1500 transistors per cm^2 have been demonstrated using specific photolithography techniques, such examples remain limited [11–13]. Therefore, exploring new strategies beyond the miniaturization of electronic components is required for the advancement of organic ICs.

Multivalued logic circuits (MVLs) constitute promising alternatives to existing binary logic circuits owing to their high integration density, low power consumption, and high-speed operation. Recently, various types of MVLs have been demonstrated with diverse semiconductor materials including organic semiconductors [14–20]. Moreover, the circuit complexity of

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existing binary logic circuits can be drastically reduced by introducing MVLs. For example, the reduction area in ICs is expected to reach 35% for ternary logic circuits and above 50% for quaternary logic circuits [14, 19, 21]. Such reductions in the circuit area and number of interconnectors can contribute to improving the processing speed and power consumption. Overall, the potential advantages can foster the development of organic MVLs for next-generation computing architectures.

A remarkable alternative is the adaptation of the logic-in-memory (LIM) architecture [22–26]. In current von Neumann systems, logic and memory components are physically isolated, increasing both power consumption and data latency. These obstacles, known as von Neumann bottlenecks, become increasingly prominent due to the intensive data transfer between logic and memory components in modern devices [27, 28]. In the LIM architecture, the logic and memory components are merged in the same circuit, enabling high-throughput and energy-efficient data processing. Moreover, the incorporation of nonvolatile memory enables reconfigurable logic operations. Like field-programmable gate arrays, individual logic circuits can be electrically reconfigured at the hardware level [29–31].

In this study, we developed a ternary LIM device based on an organic antiambipolar transistor (OAAT), where the ternary inverter and ternary nonvolatile memory functions are combined in the same device. An AAT is a heterojunction transistor with at least a p–n junction in the transistor channel [32–39]. This p–n junction induces negative differential transconductance. The drain current increases and then decreases despite the monotonic increase in gate voltage. Therefore, AATs exhibit Λ- or N-shaped current transfer curves, which have been leveraged in MVLs. We have demonstrated ternary and quaternary logic circuits via the series connection of an OAAT and n-type transistors [40–43]. In this study, we further introduced a gold (Au) floating gate to integrate a nonvolatile memory function into a ternary inverter.

First, the prepared ternary LIM device behaves as a standard ternary inverter (STI) with extremely low input (V_{in}) and drain (V_D) voltages of 2 V owing to its hafnium oxide (HfO_2) high-k gate insulator. Three output voltages (V_{out}) corresponding to logic states "2," "1," and "0" are observed while sweeping V_{in}. Subsequently, the voltage transfer curve is markedly shifted up to 1.8 V by adjusting the type of carrier (i.e., holes or electrons) trapped in the floating gate. This feature allows the inverter to work as a ternary nonvolatile memory. Three V_{out} values representing logic states "2," "1," and "0" are clearly observed at the reading input voltage ($V_{in,\ read}$) of 0.5 V, even after turning off the supplied voltages. This memory function enables reconfigurable ternary inverter operations in a single LIM device. Three typical ternary inverters, namely, STI, negative ternary inverter (NTI), and positive ternary inverter (PTI) can be electrically reconfigured by controlling hole- and electron-trapping processes into the floating gate. These functions are required to construct the combined systems of ternary and binary logic circuits, where ternary signals are converted to binary signals and vice versa, leading to the realization of more advanced MVLs, e.g., ternary decoders, adders, and two-input logic circuits, with smaller footprints [14, 26]. Our approach thus paves the way to high-performance flexible and wearable organic ICs in future.

2 | Results and Discussion

2.1 | STI Operation

Figure 1a,b shows the device structure and optical microscope image of the developed ternary LIM device. The corresponding equivalent circuit is depicted in Figure 1c. The ternary inverter part is constructed by a series circuit comprising an OAAT and an n-type transistor via an output electrode. In addition, 7-decyl-2-phenyl[1]benzothieno[3,2-*b*][1]benzothiophene (Ph-BTBT-C_{10}) and PhC_2H_4-benzo[de]isoquinolino[1,8-gh]quinolone diimide (PhC_2-BQQDI) films are used as the p- and n-type organic semiconductors, respectively. The source electrode is formed on the PhC_2-BQQDI channel layer, while the drain electrode is formed on the Ph-BTBT-C_{10} channel layer. Additionally, an Au bottom gate electrode is used as the common input electrode of the inverter. Another Au film sandwiched between two HfO_2 layers constitutes the floating gate to integrate the nonvolatile memory function into the ternary inverter. The top and bottom HfO_2 layers serve as the tunneling and gate insulating layers, respectively. The detailed preparation of the ternary LIM and optimization of the device structure are provided in the experimental section and supporting information (Figures S1–S3).

Figure 1d exhibits the current transfer of drain current (I_D)–gate voltage (V_G) for the OAAT and PhC_2-BQQDI transistor in a ternary LIM device. V_D values of 2 and −2 V were applied to the PhC_2-BQQDI transistor and OAAT, respectively. As the floating gate was grounded before measuring the current transfer curves, no charges appeared in the floating gate. The V_G values for the corresponding transistors are allocated from the common V_{in} values. Given the equivalent circuit in Figure 1c, V_{in} is directly applied to the PhC_2-BQQDI transistor as the gate voltage ($V_{G,\ PhC2\text{-}BQQDI}$). Conversely, voltage difference ($V_{in} - V_D$) is supplied as the OAAT gate voltage ($V_{G,\ AAT}$). The PhC_2-BQQDI transistor exhibits a typical n-type operation. I_D in the transistor monotonically increases with V_{in} (blue line in Figure 1d). Meanwhile, the OAAT indicates a horizontally flipped N-shaped current transfer curve according to V_{in} because ($V_{in} - V_D$) is applied to the OAAT as $V_{G,\ AAT}$ (red line in Figure 1d). First, I_D in the OAAT decreases with V_{in} and then starts increasing at V_{in} of 0.8 V. Afterward, I_D reduces again at V_{in} of 1.3 V and is completely suppressed at V_{in} of 1.8 V.

The corresponding voltage transfer curve (V_{out}–V_{in}) of the ternary LIM device for V_D of 2 V is shown in Figure 1e. Three different V_{out} values are observed at 2.0, 0.9, and 0 V with increasing V_{in}, corresponding to logic V_{out} states "2," "1," and "0," respectively. This response corresponds to the typical STI operation. The change in V_{out} in the ternary LIM device can be explained by considering I_D variations of both constituent transistors according to the common V_{in} (Figure 1d).

The I_D–V_G curves shown in Figure 1d can be divided into three V_{in} ranges (green dashed lines). In range (i) ($V_{in} < 0.8$ V), a higher I_D flows in the OAAT compared with that of the PhC_2-BQQDI transistor. Accordingly, V_D of 2.0 V is the highest V_{out} (logic state "2") in range (i) in Figure 1e because the output and drain electrodes are electrically connected. Then, comparable

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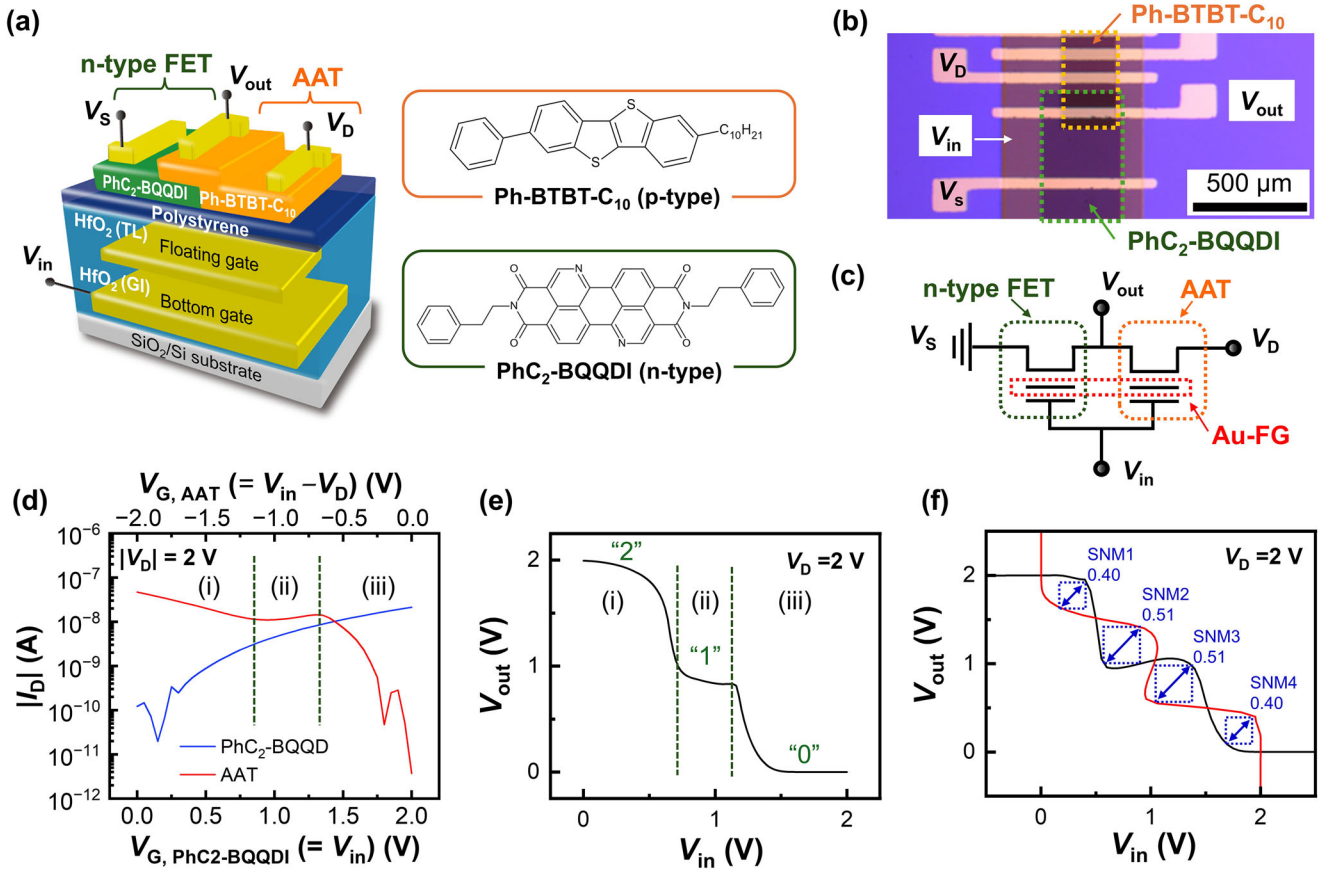


FIGURE 1 | (a) Device structure and (b) optical microscope image of ternary LIM with Au floating gate. PhC_2-BQQDI and Ph-BTBT-C_{10} films are used as transistor channels. (c) Equivalent circuit of ternary LIM device constructed by a series circuit comprising OAAT and n-type transistor. (d) I_D–V_G curves of OAAT and n-type transistor in ternary LIM device. The V_G values for respective transistors are converted from V_{in} of the ternary LIM device. (e) V_{out}–V_{in} curve of ternary LIM device, where V_{in} intervals (i), (ii), and (iii) agree with V_{out} ranges of logic states "2," "1," and "0," respectively. (f) Butterfly curve of ternary LIM device.

I_D values flow in both transistors in range (ii) (0.8< V_{in} < 1.2 V) (Figure 1d). Hence, V_{out} of 0.9 V is obtained as logic state "1" (Figure 1e). Further increasing V_{in} reduces I_D in the OAAT in range (iii) (V_{in} > 1.2 V) (Figure 1d), whereas I_D in the PhC_2-BQQDI transistor increases with increasing V_{in} (Figure 1d). Hence, a conducting path is formed between the output and source electrodes, resulting in the lowest V_{out} (0 V) as logic state "0" (Figure 1e). Therefore, the full V_{out} swing from V_D (2 V) to the ground voltage (0 V) is obtained in the voltage transfer curve (Figure 1e). Moreover, STI operation is achieved at extremely low driven voltages (V_{in} and V_D of 2 V) owing to the HfO_2 high-k gate insulator. Usually, operation voltages above 5 V are required for ternary inverter operation [34–37, 40–42]. Additionally, higher static noise margins (SNMs) are obtained in our LIM device, compared with those of the reported ternary inverters [35, 41]. The maximum and averaged SNMs obtained from 10 different devices were estimated at 0.4 and 0.3 ± 0.1 V, respectively (Figure 1f; Figure S2). These values correspond to 80% and 60% of the ideal value of the ternary inverter (V_D/4 = 0.5 V), respectively. Therefore, the obtained low-voltage STI operation with high SNM is a remarkable achievement in this study.

Figure 2a,b shows the actual STI operation, where V_{in} and V_{out} are measured over time. When 0, 1.0, and 2.0 V are assigned as the lowest (i.e., logic state "0"), middle (i.e., logic state "1"), and highest (i.e., logic state "2") V_{in} states, the corresponding V_{out} values of 2.0, 0.8, and 0 V are obtained as the highest (i.e., logic state "2"), middle (i.e., logic state "1"), and lowest (i.e., logic state "0") V_{out} states, respectively (Figure 2a). Stable STI operation is confirmed for the repeated application of V_{in} signals, as shown in Figure 2b.

2.2 | Ternary Nonvolatile Memory Operation

We present the nonvolatile memory operation in the ternary LIM device by controlling the charge condition of the Au floating gate. The initial, electron- and hole-trapped processes are illustrated in Figure 3a. The carrier injection processes into the floating gate are affected by the film thickness of the HfO_2 tunneling layer and pre-voltage application conditions. Therefore, we optimize these parameters before evaluating the memory properties, as shown in Figures S3 and S4. The detailed carrier-injection mechanism into the Au floating gate is provided in Supporting Information. The electron injection into the Au floating gate occurs from the source electrode via the PhC_2-BQQDI layer when a positive V_{in} is applied. In contrast, holes are injected into the floating gate when a negative V_{in} is applied. Both carrier-injection currents follow Fowler-Nordheim tunneling, which is the same analogy as those in conventional floating-gate memories.

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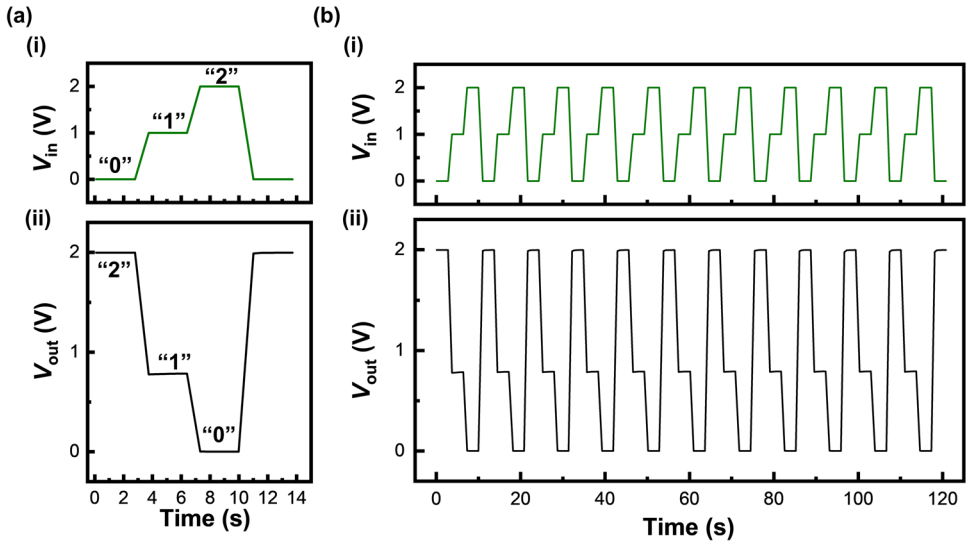


FIGURE 2 | STI operations in ternary LIM device with (a) single and (b) repeated V_{in} signals. Labels (i) and (ii) indicate changes in V_{in} and V_{out} over time, respectively. Three different V_{out} states (i.e., logic states "2," "1," and "0") are observed for the corresponding V_{in} states (i.e., logic states "0," "1," and "2").

In the initial process, the Au floating gate is grounded, and no charges are accumulated in that gate (stage (i) in Figure 3a). Therefore, a similar voltage transfer curve to that shown in Figure 1e appears at the initial state (black line in Figure 3b). Then, V_{in} of −5.5 V is applied for 30 s as the pre-voltage pulse to the input electrode to trap holes in the floating gate, establishing a hole-trapping process (stage (ii) in Figure 3a). In this stage, the voltage transfer curve laterally shifts toward low V_{in} values (red line in Figure 3b). This is because the threshold voltages (V_{th}) of both constituent transistors are shifted to low V_{in} values by the trapped holes in the floating gate (Figure S6a). Hence, the center position of the middle V_{in} state (i.e., logic state "1") varies from 0.5 V (black dotted line) to −0.4 V (red dotted line), as shown in Figure 3b. Meanwhile, the opposite shift in the voltage transfer curve is induced by a pre-voltage V_{in} of 5.5 V applied for 20 s (blue line in Figure 3b) owing to the electron-trapping process into the floating gate (stage (iii) in Figure 3a). The center position of the middle V_{in} state (i.e., logic state "1") changes from 0.5 V (black dotted line) to 1.4 V (blue dotted line) (Figure 3b). This variation in the voltage transfer curve with the electron-trapping process coincides with threshold voltage shifts in both constituent transistors (Figure S6b). Remarkably, the entire shift in the middle V_{in} state (i.e., logic state "1"), namely, the memory window, reaches 1.8 V by adjusting the electron- and hole-trapping processes in the floating gate.

This marked shift in the voltage transfer curve induced by the floating gate allows the device to operate as a ternary nonvolatile memory. Three distinct V_{out} states that correspond to logic states "0, " "1, " and "2" are observed by monitoring at $V_{in,\,read}$ of 0.5 V. The individual V_{out} states are continuously output for at least 3500 s, as shown in Figure 3c. The switching property between the three V_{out} states in the ternary memory is depicted in Figure 3d. The three V_{out} states are clearly distinguishable. The deviations in V_{out} values at corresponding logic states "0, " "1," and "2" are small and estimated to be within 0.2 V.

2.3 | Reconfigurable Ternary LIM Operation

Based on the abovementioned developments, namely, ternary inverter and ternary memory operations in the same device, we demonstrate representative reconfigurable ternary LIM operations (Figure 4). Three distinct inverter operations, namely, STI, NTI, and PTI, are obtained by controlling the charge condition of the floating gate. These inverters are necessary to construct ternary logic circuits, e.g., ternary decoders, adders, and two-input logic circuits, where ternary signals are converted to binary signals and vice versa [26, 44, 45].

The truth table of the individual ternary inverters is depicted in Figure 4a. Figure 4b shows the STI, NTI, and PTI operations at the initial, hole-trapped, and electron-trapped states, respectively. Importantly, the three inverter operations are achieved for the same V_{in} sequence. At the initial state, the device exhibits normal STI operation. For V_{in} logic states "0," "1," and "2," the opposite V_{out} logic states, namely, "2," "1," and "0," are obtained, respectively (stage (i) in Figure 4b). At the hole-trapped state, V_{out} logic states "2," "0," and "0" are output for the same V_{in} sequence as that of the initial state (V_{in} logic states of "0," "1," and "2," respectively) (stage (ii) in Figure 4b). Hence, the circuit varies from STI to NTI by the transition from the initial to the hole-trapped state. Finally, the device operates as PTI at the electron-trapped state. V_{out} logic states "2," "2," and "0" are visible without any variation in the V_{in} sequence (stage (iii) in Figure 4b). Stable inverter operations in STI, NTI, and PTI are confirmed for over 10 repeated V_{in} sequences, as shown in Figure 4c.

Similarly, different ternary inverter operations corresponding to the derivatives of NTI and PTI can be demonstrated with the same V_{in} sequence, as shown in Figure 5, where V_{out} logic states "2," "1," and "0" (STI, initial state), V_{out} logic states "1," "0," and "0" (NTI 2, hole-trapped state), and V_{out} logic states "2," "2," and "1" (PTI 2, electron-trapped state) are obtained at V_{in} of −0.4, 0.5, and 1.5 V representing logic states "0," "1," and "2," respectively.

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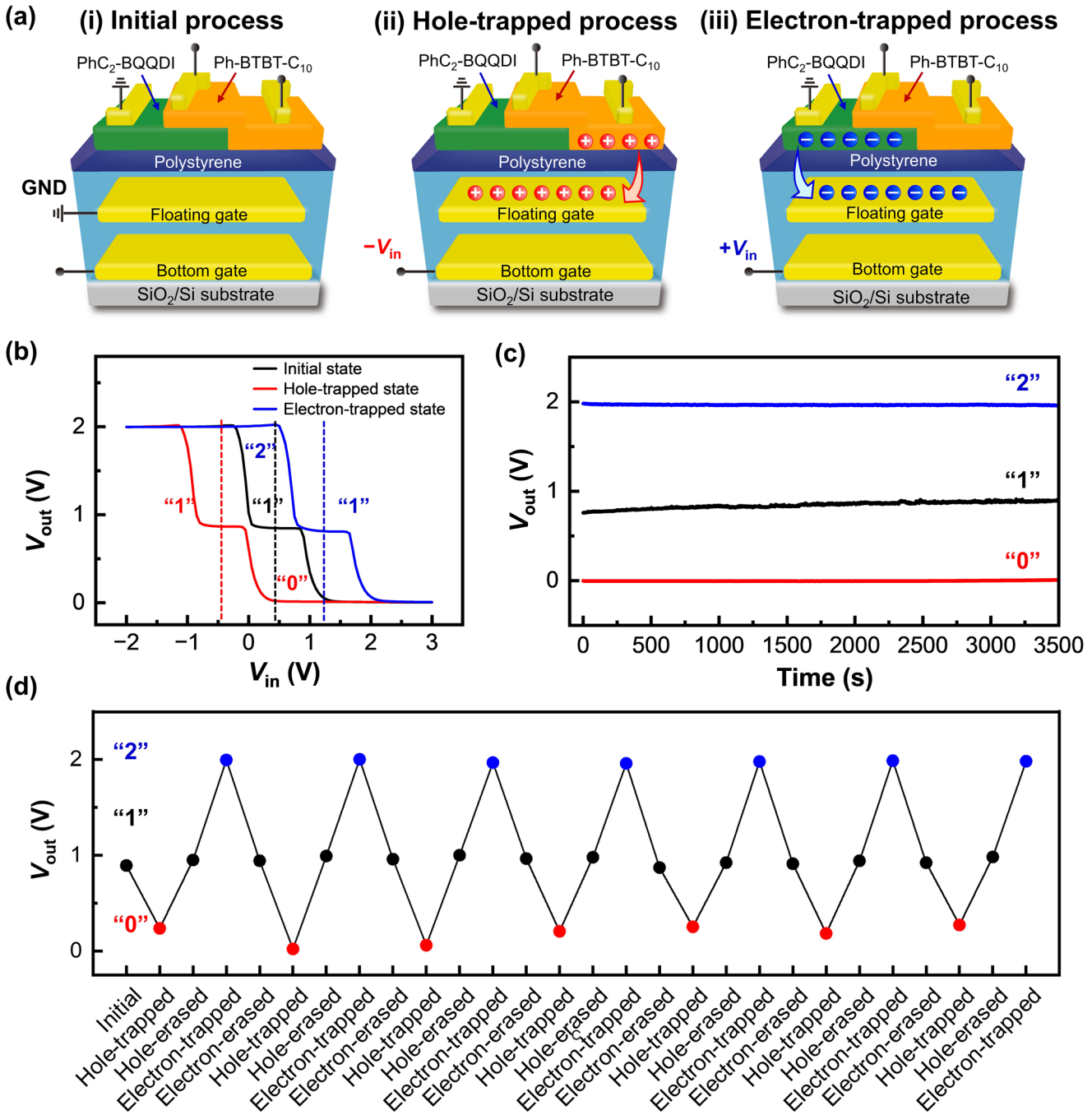


FIGURE 3 | (a) (i) Initial, (ii) hole-trapping, and (iii) electron-trapping processes of ternary LIM device. (b) V_{out}–V_{in} curves obtained at initial (black line), hole-trapped (red line), and electron-trapped (blue line) states. The dotted black, red, and blue lines are drawn at the center positions of the middle V_{in} state (i.e., logic state "1") measured at the initial, hole-trapped, and electron-trapped states, respectively. (c) Retention property of ternary LIM device measured at $V_{in,\,read}$ of 0.5 V. (d) Switching property of ternary LIM device. The switching behavior is measured at $V_{in,\,read}$ of 0.55 V through the following pre-voltage pulse sequence: initial state (V_{in} = 0 V, grounded) → hole-trapped state (V_{in} = −5.5 V for 30 s) → hole-erased state (V_{in} = 5.0 V for 10 s) → electron-trapped state (V_{in} = 5.5 V for 20 s) → electron-erased state (V_{in} = −5.0 V for 10 s).

As shown above, our LIM device enables electrical reconfiguration between STI, NTI, and PTI with only two transistors (OAAT and an n-type transistor). Besides, the operation voltages are as low as 2 V for all ternary inverter operations. Similar ternary LIM operations have been demonstrated with versatile material combinations with not only organic materials, but also inorganic materials (Table 1) [26, 42, 44–47]. However, in most cases, the three ternary inverters are formed by different circuit designs and thus cannot be reconfigured in general [44, 45]. Besides, 3–6 transistors are required to realize the STI operation using conventional transistors [19, 48–50]. Although there is only an example of the complete transition of STI, NTI, and PTI using an organic AAT, the driving voltage of as high as 6 V and the programing voltage of up to 18 V are necessary [26]. Therefore, our proposed LIM device has superior potential to realize further energy-efficient computing systems in future.

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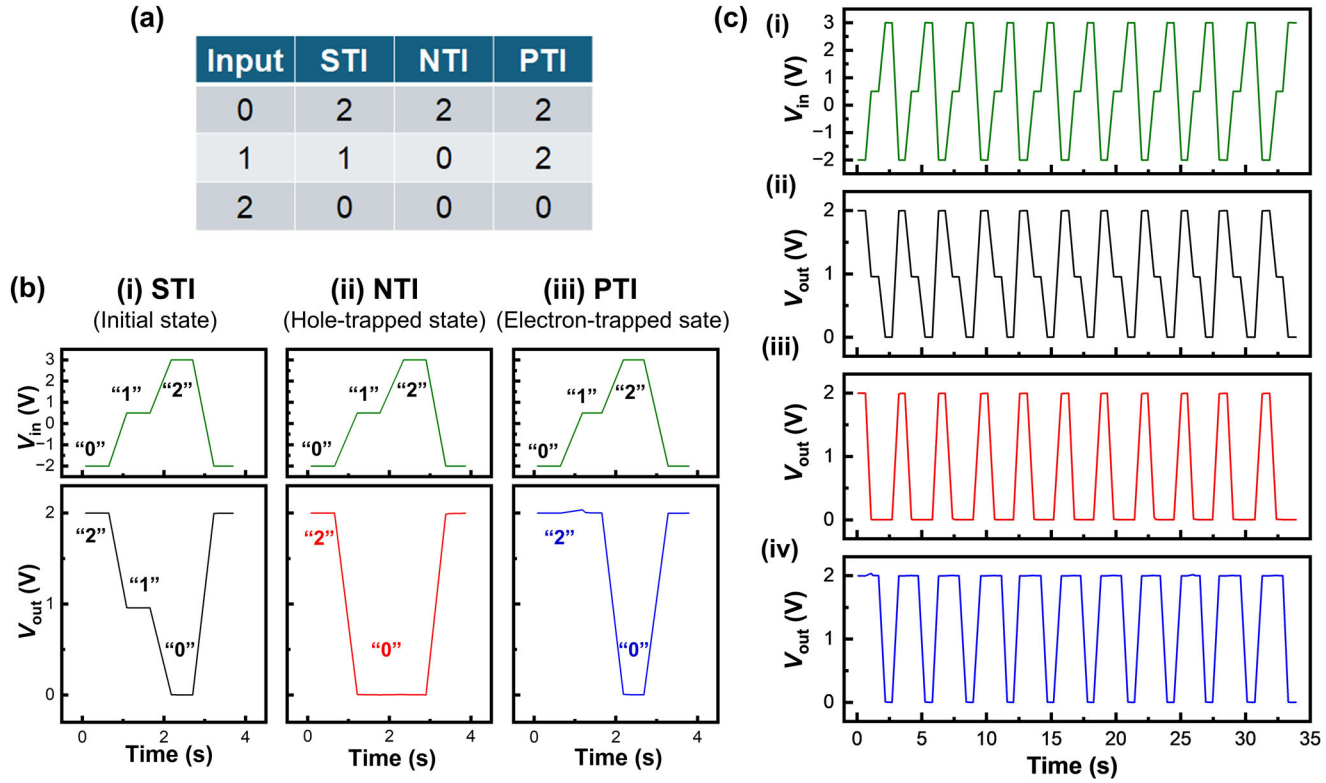


FIGURE 4 | (a) Truth table of ternary inverters: STI, NTI, and PTI. (b) Reconfigurable ternary inverter operations of (i) STI, (ii) NTI, and (iii) PTI achieved at initial, hole-trapped, and electron-trapped states, respectively, for the same V_{in} sequence. (c) Repeated ternary inverter operations of (ii) STI, (iii) NTI, and (iv) PTI for the same (i) V_{in} sequence.

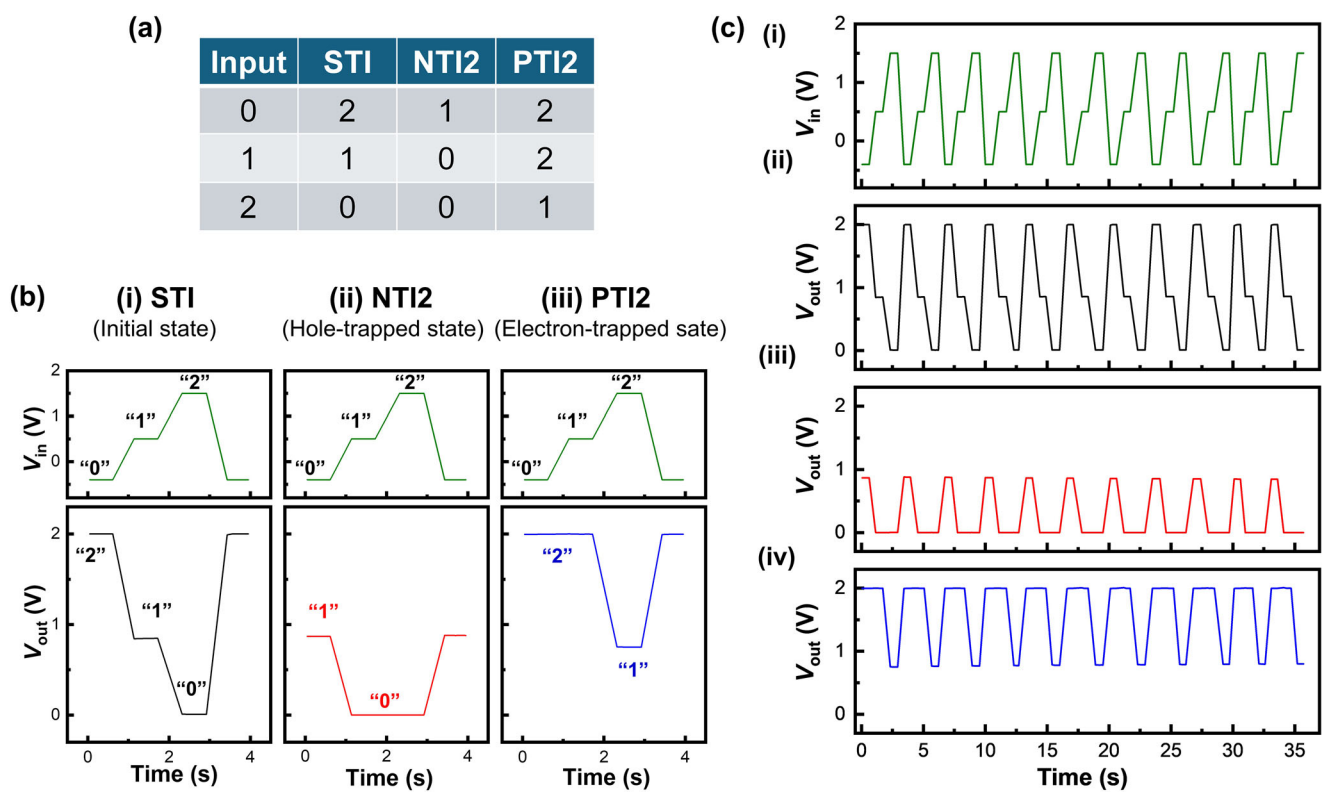


FIGURE 5 | (a) Truth table of ternary inverters STI, NTI 2, and PTI 2. NTI 2 and PTI 2 are the derivatives of NTI and PTI shown in Figure 4, respectively. (b) Reconfigurable ternary inverter operations: (i) STI (initial state), (ii) NTI 2 (hole-trapped state), and (iii) PTI 2 (electron-tapped state). (c) Repeated ternary inverter operations of (ii) STI, (iii) NTI, and (iv) PTI for the same (i) V_{in} sequence.

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TABLE 1 | Comparison in ternary inverters with STI, NTI, and PTI operations.

Type	Material	Number of transistors in STI/NTI/PTI	STI operation voltage (V)	Reconfigurable operation	Memory type	Memory window (V)	Refs.
Si-FinFET/RRAM	Si-FinFET	6/2/2	~1	No	HfO_2-based RRAM	~1	[44]
Si-FinFET/MRAM	Si-FinFET	6/2/2	~1	No	STT-MRAM	NA	[45]
2D-AAT	ReS_2/BP	2/NA/NA	6	No	2D-floating fate	~1	[46]
Organic AAT	PTCDI-C_{13}/DNTT	2/NA/NA	5	No	Metal floating gate (Al)	~3	[47]
Organic AAT	PTCDI-C_{13}/DNTT	2/2/2	6	Yes	Metal floating gate (Al)	~2	[26]
Organic AAT (our previous work)	PhC_2-BQQDI/C_8-BTBT	2/NA/NA	10	No	Polymer floating gate (ZnPc-PS_4)	~2	[42]
Organic Aat (in this work)	PhC_2-BQQDI/Ph-BTBT-C_{10}	2/2/2	2	Yes	Metal floating gate (Au)	~2	

3 | Conclusion

We demonstrated a reconfigurable ternary LIM device consisting of an OAAT and n-type transistor. An Au floating gate played an important role in reconfigurable ternary logic operations. First, a normal STI was obtained at low driven voltages of 2 V at the initial state. Furthermore, NTI and PTI were obtained for the same V_{in} signal as that of STI by adjusting the charge condition of the floating gate. Importantly, these reconfigurable ternary inverters were prepared with an extremely low operating voltage of 2 V and with only two transistors (OAAT and n-type transistor). Additionally, ternary inverter operations cannot be reconfigured in general. In contrast, our proposed ternary LIM device achieved versatile ternary inverter operations, including STI, NTI, and PTI, with only two transistors. Furthermore, these inverters were electrically reconfigured by controlling the charge condition of the floating gate without variations in the V_{in} signals. Such functions can support the development of reconfigurable and energy-efficient artificial intelligence systems, aiming at surpassing existing von Neumann systems.

4 | Experimental Section/Methods

4.1 | Formation of Ternary LIM

A ternary LIM with an Au floating gate was prepared on a highly doped p-type Si (100) substrate (<0.01 Ω·cm) with a 200 nm-thick SiO_2 film. First, an Au (30 nm)/Cr (5 nm) electrode was deposited as a common input electrode of the circuit on an SiO_2/Si substrate via thermal vacuum deposition. Next, an HfO_2 film (35 nm) was formed as the gate insulating layer of the OAAT and n-type transistor using atomic layer deposition (SUGA, SAL 1000) at a substrate temperature of 175°C. Tetrakis(dimethylamino)hafnium and water were used as the hafnium and oxygen sources, respectively. Then, an Au (10 nm)/Cr (5 nm) electrode was thermally grown on the HfO_2 gate insulating layer as the floating gate at a deposition rate of 5 Å/s to ensure a smooth surface morphology of the Au thin film. Subsequently, an 8 nm-thick HfO_2 tunneling layer was formed via atomic layer deposition following the same process as that for the gate insulating layer. To passivate carrier trap sites on the HfO_2 surface, a 10 nm-thick polystyrene (Sigma–Aldrich, 182427; average molecular weight, 280,000) layer was spin-coated on the HfO_2 tunneling layer. Next, Ph-BTBT-C_{10} (17 ± 2 nm) and PhC_2-BQQDI (23 ± 2 nm) films were grown as p- and n-type organic transistor channels, respectively, via thermal vacuum deposition at a background pressure of 10^{-7} Pa. Finally, 30 nm-thick Au films were deposited for the source, drain, and output electrodes via thermal vacuum deposition. The typical channel lengths and widths of the OAAT were 107 ± 11 and 228 ± 11 μm, respectively, and those of the n-type transistor were 304 ± 6 and 334 ± 14 μm, respectively.

4.2 | Electrical Measurement of Ternary LIM

The electrical measurements of the ternary LIM were performed using source measurement units (Keysight Technologies, B2912B) at room temperature. All measurements were conducted using a four-probe system at room temperature under atmospheric conditions.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that supports the findings of this study are available in the supplementary material of this article.

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