Suppression of High Threshold Voltage for Boron-doped Diamond MOSFETs

Jiangwei Liu, Tokuyuki Teraji, Bo Da, and Yasuo Koide

***Abstract*—Suppression of high threshold voltage (V_{TH}) for the boron-doped diamond (B-diamond) metal-oxide-semiconductor field-effect transistors (MOSFETs) plays a key role to design the diamond complementary MOS circuits with low gate drive sources. The V_{TH} can be further suppressed by adjusting B-diamond epitaxial layer thickness, boron doping concentration, and gate oxide thickness. Three MOSFETs with different device structures are fabricated on the same oxygen-terminated B-diamond channel. Thickness and acceptor concentration for the B-diamond epitaxial layer are approximately 800 nm and 1.36×10^{16} cm^{-3}, respectively. A 45 nm-thick Al_2O_3 is deposited as the gate oxide by an atomic layer deposition technique. Maximum drain currents and on/off ratios for the B-diamond MOSFETs are in the range of $-2.4 \sim -4.3$ μA/mm and greater than 10^6, respectively. Their V_{TH} values are lower than 3.4 V with the lowest one of 0.8 V.**

***Index Terms*—Diamond, Boron-doped, MOSFET, Threshold voltage**

I. Introduction

Over the past two decades, diamond-based metal–oxide–semiconductor field-effect transistors (MOSFETs) have undergone significant development to meet requirements of high-power, high-frequency, and high-temperature applications [1-4]. This is attributed to the excellent intrinsic properties of diamond, such as its wide bandgap energy, high breakdown field, high thermal conductivity, and large carrier mobility [5, 6].

Two types of *p*-type diamond channels were employed for the fabrication of MOSFETs. Owing to the transfer of electrons from hydrogen-terminated diamond (H-diamond) to the negatively charged acceptors on the surface, two-dimensional hole gas accumulates on the H-diamond with a sheet hole density as large as ~10^{14} cm^{-2} [7]. To date, most diamond MOSFETs and MOSFET logic circuits have been fabricated on the H-diamond channels with outstanding electrical properties [1-4, 8]. Unfortunately, their poor thermal stability hinders their use in high-temperature field [9].

Recently, significant efforts have been made toward the development of diamond MOSFETs on *p*-type boron-doped diamond (B-diamond) channels with oxygen-terminated surface [9-13]. However, because the activation energy of the boron dopant (370 meV) far exceeds the thermal energy at room temperature (26 meV) [14], B-diamond MOSFETs operate at low output currents. A relatively flat (surface roughness of 0.15 nm) and highly doped B-diamond ($10^{17} \sim 10^{18}$ cm^{-3}) was used to fabricate the MOSFETs [13], which increased their output currents to 490 μA/mm; this value is higher than that of MOSFETs previously studied (120 μA/mm) [10-12].

Another significant issue with B-diamond MOSFETs is their high threshold voltage (V_{TH}) values. When the B-diamond epitaxial layer thickness and acceptor concentration (N_A) were 700 nm and 2.92×10^{16} cm^{-3}, respectively, V_{TH} for the as-fabricated B-diamond MOSFET was 63.2 V [13]. In addition, when these parameters were 2000 nm and 6.02×10^{15} cm^{-3}, respectively, V_{TH} was as high as 58.8 V [15]. It was reported that the V_{TH} decreased to 7.0 V by reducing the thickness to 230 nm for the B-diamond with N_A of 2×10^{17} cm^{-3} [11, 16]. Therefore, the choice of B-diamond active layer thickness and boron concentration are important for reduction of V_{TH} for the B-diamond MOSFETs. On the other hand, it was proved that there were negative flat band voltage (V_{FB}) shift for capacitance-voltage (*C*-*V*) curves of the Al_2O_3/B-diamond MOS capacitors [13, 15]. Therefore, positive fixed charges exist in the Al_2O_3 gate oxides. When the gate–source voltage (V_{GS}) is positive, electric field across the Al_2O_3 would be enhanced due to the existence of positive charges. Increase of the thickness for the Al_2O_3 would increase positive charges and the absolute V_{FB} ($|V_{FB}|$) value, leading to the decrease of the V_{TH} for the MOSFETs.

Since the low V_{TH} for the B-diamond MOSFETs plays a key role to reduce system complexity during designing complementary MOS circuits, in this study, we would make effects to further decrease the V_{TH} of B-diamond MOSFETs by adjusting the thickness of the B-diamond epitaxial layer, boron doping concentration, and thickness of the Al_2O_3 gate oxide.

II. Experimental

A microwave plasma-assisted chemical vapor deposition technique was employed to grow a B-diamond epitaxial layer on a well-polished (roughness: 0.1 nm) and acid-cleaned (H_2SO_4 + HNO_3 at 300 °C for 3 h) Ib-type (100) diamond substrate [17]. Thickness and boron concentration of the B-diamond channel were confirmed using a secondary-ion mass spectroscopy (SIMS) technique to be approximately 800 nm and $10^{16} \sim 10^{17}$ cm^{-3}, respectively [Fig. 1(a)]. The N_A for the B-diamond is deduced by the *C*-*V* measurement in the following section to be 1.36×10^{16} cm^{-3}. Surface root mean square roughness is lower than 0.2 nm [13, 15]. Comparing to the B-diamond in *Ref.* 13 (V_{TH} = 56.1 V), the channel thickness is similar, but the boron concentration decreases. While the doping level is higher than that of the *Ref. 15* (V_{TH} = 58.8 V), the B-diamond thickness is reduced from 2000 nm to 800 nm.

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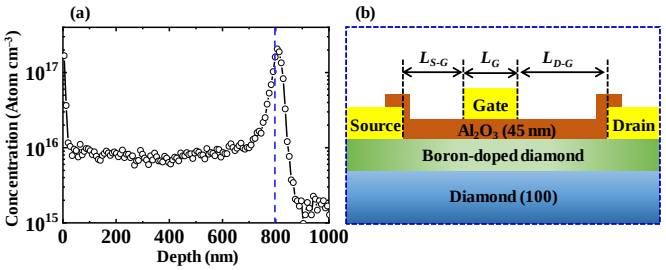

Fig. 1. (a) Depth profile of the SIMS measurement for concentration of boron atoms in the B-diamond epitaxial layer, and (b) schematic diagram of the Al_2O_3/B-diamond MOSFET.

After modifying the hydrogen- to oxygen-terminated surface for the B-diamond channel in the mixture acid solution (H_2SO_4 + HNO_3), the fabrication of MOSFETs was performed. The B-diamond was coated using a spin-coater with photoresists of LOR 5A and AZ 5214E sequentially. The rotation rate and time for both photoresists are 7000 rpm and 1 second, respectively. The baking temperature and time for the LOR 5A are 180 °C and 5 minute, respectively. Those for the AZ 5214E are 110 °C and 2 minute, respectively. The sample was exposed and developed via a scanning maskless lithography system and a Tetramethyl Ammonium Hydroxide (concentration: 2.38%) solution, respectively. The developing time is 2.0 min.

After evaporating the source/drain Ti/Au electrodes in a high-vacuum evaporation chamber with thicknesses of 10/150 nm, the sample was lifted-off in an N-Methyl-2-Pyrrolidone solution at 80 °C for 40 min and annealed at 550 °C for 20 min to form Ohmic contact using a rapid thermal annealing system. The 45 nm-thick Al_2O_3 film was deposited using an atomic layer deposition technique at 200 °C with $Al(CH_3)_3$ and water vapor precursors to cover all the surface of the sample. The thickness of the Al_2O_3 film is larger than that of the previous reports [13, 15]. Then, the Ti/Au gate electrodes with thicknesses of 10/150 nm was formed. Lastly, the Al_2O_3 film covering on the source/drain electrodes was etched by a capacitively coupled plasma reactive-ion etching system in the CHF_3+Ar atmosphere to open the contact windows. The plasma power, CHF_3 flow rate, and Ar flow rate were 100 W, 10 sccm, and 40 sccm, respectively.

A schematic of the Al_2O_3/B-diamond MOSFET is shown in Fig. 1(b). Three types of B-diamond MOSFETs were fabricated by varying the gate length (L_G) and interspace length between the source/drain and gate electrodes (L_{S-G} and L_{D-G}). The electrical properties for the B-diamond MOSFETs were measured at room temperature using an MX-200/B prober and a B1500A parameter analyzer.

III. Results and Discussion

Figures 2(a), (c), and (e) show optical microscope images of B-diamond MOSFET-I, -II, and -III, respectively. The diameter of the drain electrodes of the three MOSFETs was maintained as 398.2 μm with a gate width of 1.25 mm. Figures 2(b), (d), and (f) show scanning electron microscopy (SEM) images of the B-diamond MOSFET-I, -II, and -III marked with blue boxes in Figs. 2(a), (c), and (e), respectively. The L_G, L_{S-G}, and L_{D-G} values for MOSFET-I are 3.7, 7.3, and 8.9 μm, respectively,

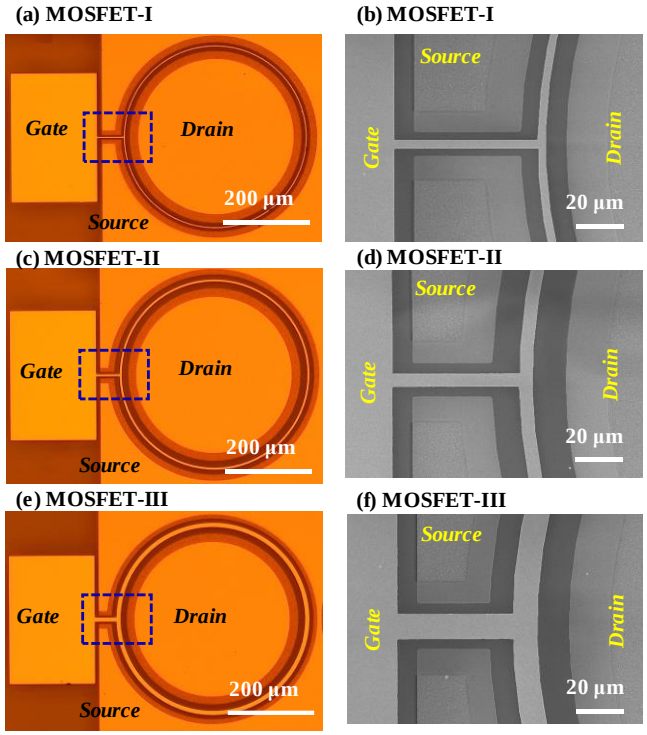

Fig. 2. (a), (c), and (e) Microscope images of B-diamond MOSFET-I, -II, and III, respectively. (b), (d), and (f) SEM images of B-diamond MOSFET-I, -II, and -III marked with blue boxes in Figs. 2(a), (c), and (e), respectively.

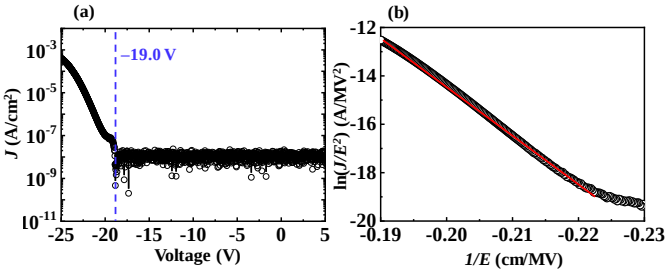

Fig. 3. (a) and (b) *J-V* and $ln(J/E^2)$-*1/E* characteristics of B-diamond MOSFET.

and 5.4/11.8/13.9 and 10.3/9.9/13.6 μm for MOSFET-II and -III, respectively.

Figure 3(a) shows the leakage current density (J) as a function of the voltage for the B-diamond MOS capacitor. The J is in the region of 10^{-8} A/cm^2 at −19.0 ~ 5.0 V. The low J value indicates a good quality Al_2O_3 gate insulator and high band offsets for the Al_2O_3/B-diamond heterojunction. As the voltage changes from −19.0 to −25.0 V, the J increases to 4.1×10^{-4} A/cm^2. Based on the *J–V* curve, the possible conduction mechanism at high voltage for the Al_2O_3/B-diamond MOS capacitor was analyzed.

Figure 3(b) shows the $\ln(J/E^2)$-$1/E$ characteristic. The E is the electrical field of Al_2O_3, which was obtained by dividing the voltage by the thickness (45 nm) of the Al_2O_3 film. There is a linear dependence of the $\ln(J/E^2)$-$1/E$ characteristic on the $1/E$ that ranges from −0.19 V to −0.22 cm/MV. Therefore, the conduction mechanism at high voltage of the Al_2O_3/B-diamond MOSFET is consistent with the Fowler–Nordheim tunneling model, according to the following equation [18]:

$$J = AE^2 \exp\left(\frac{-4\sqrt{2m^*\Phi^3}}{3\hbar q}\frac{1}{E}\right), \quad (1)$$

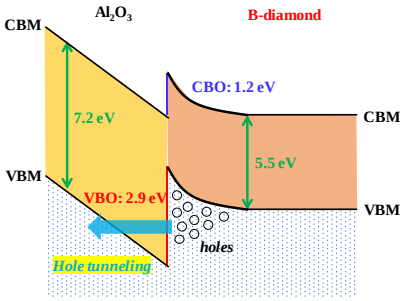

Fig. 4. Band configuration of Al_2O_3/B-diamond heterojunction. The CBM and VBM are conductance band minimum and valence band maximum, respectively.

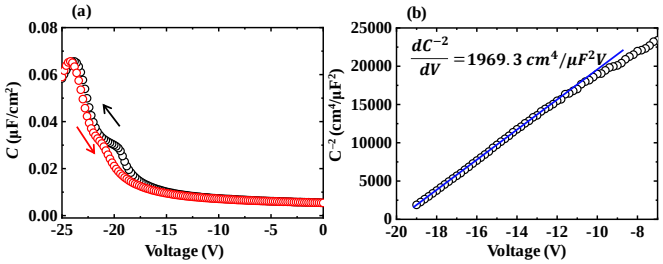

Fig. 5. (a) *C-V* and (b) C^{-2}-*V* properties for the Al_2O_3/B-diamond MOS capacitor, respectively.

where m^*, Φ, h, and q are the tunneling effective mass of a hole in Al_2O_3 ($0.36m_0$, where m_0 is the free electron mass) [19], valence band offset of the Al_2O_3/H-diamond heterojunction, Planck's constant, and elementary charge, respectively. A is a parameter that depends on m^*, Φ, and temperature.

By fitting the linear portions of $\ln(J/E^2)$-$1/E$ characteristics using Eq. (1), the valence band offset of the Al_2O_3/B-diamond heterojunction was calculated to be 2.9 eV. According to the bandgap energies of diamond (5.5 eV) and Al_2O_3 (7.2 eV) [20], the conduction band offset for the Al_2O_3/B-diamond heterojunction was deduced to be 1.2 eV. Both the valence and conduction band offsets are larger than 1.0 eV, which explains the low J of the B-diamond MOSFET [21]. Further, the band configuration of the Al_2O_3/B-diamond heterojunction exhibited a type II staggered structure, as shown in Fig. 4.

Figure 5(a) shows *C-V* properties for the Al_2O_3/B-diamond MOS capacitor. The black and red circle lines represent the measurement voltage swept from 0 V to –25.0 V and from –25.0 V to 0 V, respectively. Maximum capacitance is 0.065 μF/cm^2, which is much lower than the theoretical value of 0.157 μF/cm^2 based on the dielectric constant (8.0) of 45-nm-thick Al_2O_3 deposited at 200 °C [22]. This is possibly attributed to that the measurement capacitance is the series value between Al_2O_3 insulator and B-diamond channel layer. The capacitance decreases with the voltage shifting to the left hand side relative to –24.2 V. This is possibly attributed to the increase of the J. Hysteresis voltage shift is 0.3 V at the capacitance of 0.06 μF/cm^2 due to the trapped charges in the Al_2O_3 film. There are residual capacitances for the *C-V* curve around –20.0 V. This phenomenon can be suppressed by changing the water to ozone precursor for the Al_2O_3 deposited by the atomic layer deposition technique [15].

The *C-V* curves shift to the left hand side relative to the 0 V. Positive fixed charges exist in the Al_2O_3 film, leading to the V_{FB} shift for the B-diamond MOS capacitor. The C^{-2}–V property is shown in Fig. 5(b). Based on the value of 1969.3 cm^4/μF^{2}V for the dC^{-2}/dV, the N_A in the B-diamond channel layer can be calculated to be 1.36×10^{16} cm^{-3}. Debye length for the B-diamond is deduced to 244.3 nm by considering the hole density for the uncompensated p-type B-diamond is approximately 1% of the N_A [23], Experimental flat band capacitance and V_{FB} shift can be determined to be 0.018 μF/cm^2 and –19.5 V, respectively. The $|V_{FB}|$ is larger than those of our previous reports (13.3 and 4.1 V) [13, 15].

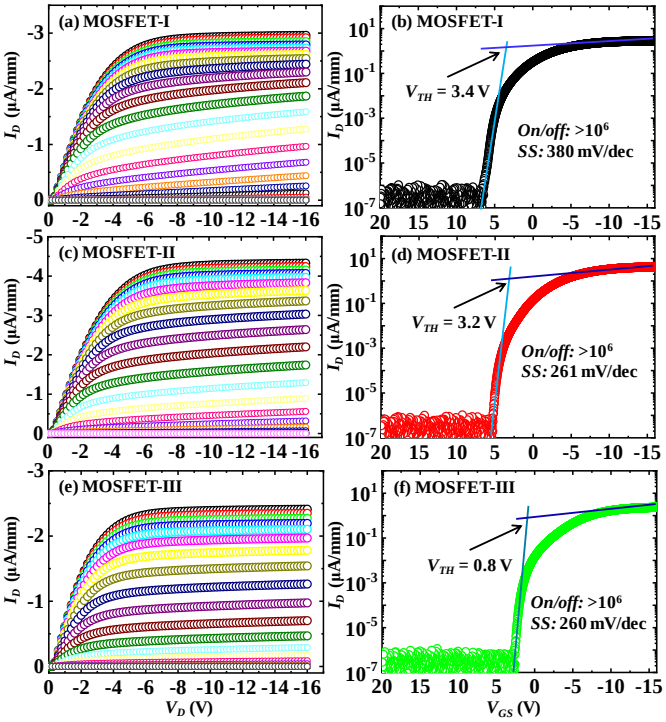

Fig. 6. (a), (c), and (e) I_D–V_D characteristics of B-diamond MOSFET-I, -II, and -III, respectively. (b), (d), (f) I_D–V_{GS} characteristics of B-diamond MOSFET-I, -II, and -III, respectively.

Figures 6(a), (c), and (e) show the drain current–drain voltage (I_D–V_D) characteristics of MOSFET-I, -II, and -III, respectively. The V_{GS} for all three MOSFETs varies from –16.0 V to 40.0 V in steps of +1.0 V. Distinct saturation and pinch-off characteristics are observed. The maximum I_D ($I_{D,max}$) values for MOSFET-I, -II, and -III are −3.0, −4.3, and −2.4 μA/mm, respectively. Although the MOSFET-I has smaller L_G, $L_{S\text{-}D}$, and $L_{D\text{-}G}$, its $I_{D,max}$ is lower than that of the MOSFET-II. This is possibly attributed to the nonuniformity of the B-diamond channel layer or the unintentional damage for the MOSFETs during the fabrication process.

Figures 6(b), (d), and (f) show the I_D–V_{GS} characteristics for B-diamond MOSFET-I, -II, and -III, respectively. Through linear extrapolation, their respective V_{TH} were determined to be 3.4, 3.2, and as low as 0.8 V, respectively. The on/off ratios for the three MOSFETs were greater than 10^6, which is reasonable for B-diamond MOSFETs with water vapor as the precursor for Al_2O_3 deposition [13]. Subthreshold voltage (*SS*) values were determined as 380, 261, and 260 mV/dec for MOSFET-I, -II, and -III, respectively. The interfacial trapped charge density (D_{it}) of the Al_2O_3/B-diamond heterojunction can be calculated using Eq. (2) [24].

TBALE1 SUMMARY OF ELECTRICAL PROPERTIES FOR THE AS-FABRICATED B-DIAMOND MOSFETS [10, 11, 13, 15]

	B-diamond thickness (nm)	Acceptor concentration (cm^{-3})	Al_2O_3 thickness (nm)	Dielectric constant of Al_2O_3	$L_G/L_{S\text{-}G}/L_{D\text{-}G}$ (μm)	$\|V_{FB}\|$ (V)	$I_{D,max}$ (μA/mm)	V_{TH} (V)
MOSFET [10]	230	1.75×10^{17}	40	9.0	3.0/4.0/4.0	-	–1.9	7.0
MOSFET [11]	500	2×10^{17}	20	-	4.0/3.0/4.0	-	–120	>20.0
MOSFET [13]	700	2.92×10^{16}	23.3	8.0	7.0/9.9/17.4	13.3	–490	56.1
MOSFET [15]	2000	6.02×10^{15}	24	7.8	5.6/9.8/15.3	4.1	–109.7	32.0
MOSFET [this work]	800	1.36×10^{16}	45	8.0	3.7/7.3/8.9 5.4/11.8/13.9 10.3/9.9/13.6	19.5	–3.0 –4.3 –2.4	3.4 3.2 0.8

$$SS = \frac{kT}{q}\ln(10)\left(1+\frac{qD_{it}}{C_{OX}}\right), \quad (2)$$

where k and T are Boltzmann's constant (8.62×10^{-5} eV/K) and room temperature (298.15 K), respectively. C_{OX} is the oxide capacitance of 45-nm-thick Al_2O_3 film (0.157 μF/cm^2) [22]. The D_{it} values for the three Al_2O_3/B-diamond interfaces were calculated as 5.32×10^{12}, 3.35×10^{12}, and 3.33×10^{12} eV^{-1} cm^{-2}, respectively. These values are greater than those for Al_2O_3/H-diamond (6.2×10^{11} eV^{-1} cm^{-2}) [25]. This is possibly attributed to the existence of more defects at the Al_2O_3/B-diamond interface. The g_m-V_{GS} characteristics for the B-diamond MOSFET-I, -II, and -III are shown in Fig. 7. They are determined based on the slopes of the linear portions for the I_D-V_{GS} characteristics in Figs. 6(b), (d), and (f). The $g_{m,max}$ values for them are –0.30, –0.44, and –0.30 μS/mm, respectively.

Table 1 summarizes electrical properties of the as-fabricated B-diamond MOSFETs reported previously [10, 11, 13, 15] and this work. The absolute $I_{D,max}$ ($|I_{D,max}|$) values in this study are higher than that (1.9 μA/mm) of the MOSFET on the B-diamond channel with a thickness and the N_A of 230 nm and 1.75×10^{17} cm^{-3}, respectively [10]. However, because of the thinner B-diamond layer and lower N_A (800 nm and 1.36×10^{16} cm^{-3}) in this work, the $|I_{D,max}|$ values are much lower than those of MOSFETs with B-diamond thicknesses and N_A values of 700 nm/2.92×10^{16} cm^{-3} [13] and 2000 nm/6.02×10^{15} cm^{-3} [15], respectively. For the B-diamond MOSFETs reported in references [10] and [11], the N_A values of the B-diamond channel layers are similar. However, the thinner B-diamond and Al_2O_3 leads to the decrease of V_{TH} greatly. Although the V_{TH} values for the B-diamond MOSFETs in this work are unstable with different device structures, they are much lower than those reported in previous studies [10, 11, 13, 15]. The B-diamond thickness for the reference [13] and this work is similar. The lower N_A for the B-diamond channel layer and the larger $|V_{FB}|$ value lead to the decrease of V_{TH}. On the other hand, even the N_A for the B-diamond channel layer in reference [15] is lower than that in this work, its thicker B-diamond layer and lower $|V_{FB}|$ value generate a high V_{TH}. Therefore, larger $|V_{FB}|$ value, thinner channel layer, and lower dopant concentration can decrease V_{TH} for B-diamond MOSFETs greatly. In contrast, this type of B-diamond MOSFETs demonstrate low output currents. Therefore, the balance between low V_{TH} and high output current is important to advance the development of B-diamond MOSFETs for future applications.

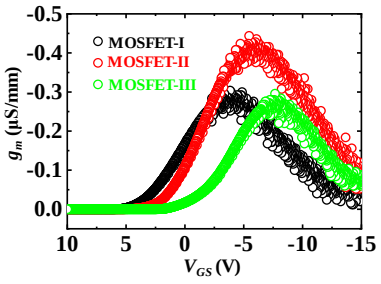

Fig. 7. The g_m-V_{GS} characteristics for the B-diamond MOSFET-I, -II, and -III, respectively.

IV. Conclusions

In this study, we suppressed the high V_{TH} of the B-diamond MOSFETs by adjusting the thickness of the B-diamond epitaxial layer, N_A, and thickness of the Al_2O_3 gate oxide to 800 nm, 1.36×10^{16} cm^{-3}, and 45 nm. The J value for the B-diamond MOS capacitor was approximately 10^{-8} A/cm^2 at voltage in the range of −19.0 ~ 5.0 V. The $|V_{FB}|$ for the Al_2O_3/B-diamond capacitor was deduced to be 19.5 V. The $|I_{D,max}|$ and on/off ratios for the B-diamond MOSFETs were in the range of 2.4 ~ 4.3 μA/mm and greater than 10^6, respectively. The V_{TH} values for three types of MOSFETs were determined to be lower than 3.4 ± 0.1 V with the lowest one being 0.8 ± 0.1 V. It was concluded that the larger $|V_{FB}|$ value, thinner channel layer, and lower dopant concentration can decrease V_{TH} for B-diamond MOSFETs greatly. A low V_{TH} is desirable to reduce the system complexity and gate drive source during the design of B-diamond MOSFET circuits. Further studies will be located at making the balance between the low V_{TH} and high output current for the B-diamond MOSFETs.

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