

Room Temperature Negative Differential Resistance with High Peak Current in MoS₂/WSe₂ Heterostructures

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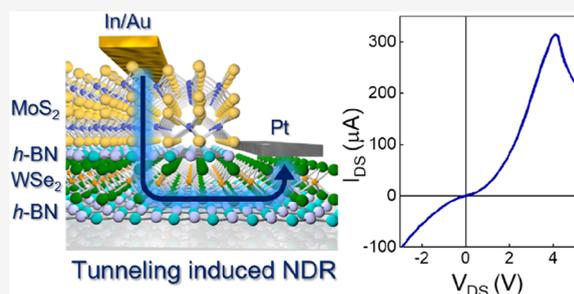
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ABSTRACT: Two-dimensional transition metal dichalcogenide (2D TMD) semiconductors allow facile integration of p- and n-type materials without a lattice mismatch. Here, we demonstrate gate-tunable n- and p-type junctions based on vertical heterostructures of MoS₂ and WSe₂ using van der Waals (vdW) contacts. The p–n junction shows negative differential resistance (NDR) due to Fowler–Nordheim (F–N) tunneling through the triangular barrier formed by applying a global back-gate bias (V_{GS}). We also show that the integration of hexagonal boron nitride (*h*-BN) as an insulating tunnel barrier between MoS₂ and WSe₂ leads to the formation of sharp band edges and unintentional inelastic tunnelling current. The devices based on vdW contacts, global V_{GS} , and *h*-BN tunnel barriers exhibit NDR with a peak current (I_{peak}) of 315 μ A, suggesting that the approach may be useful for applications.

KEYWORDS: 2D materials, negative differential resistance, tunnel transistor, MoS₂/WSe₂ heterostructure, *h*-BN tunnel barrier



Devices with negative differential resistance (NDR) exhibit multiple threshold voltages, making them attractive for multivalued logic systems^{1,2} and radio frequency oscillators.³ NDR devices are based on the transition of carrier transport from quantum mechanical tunnelling to thermionic emission by sweeping the applied voltage.⁴ To use NDR for functional devices, the output characteristics of the transistor in the NDR regime should have a high peak current (I_{peak}) and a high peak-to-valley current ratio (PVCR). The importance of high I_{peak} and high PVCR lies in their role in enabling efficient signal amplification, reliable switching behavior, and optimization of device performance for various high-frequency applications.^{5,6}

Two-dimensional transition metal dichalcogenide (2D TMD) semiconductors are ideally suited for realizing NDR because they can be easily assembled, and sharp interfaces can be formed without lattice mismatch.⁷ A variety of NDR devices based on heterostructures of 2D semiconductors have been reported. In particular, heterostructures using SnSe₂^{8–10} or black phosphorus (BP)^{11,12} have been studied because both are highly doped degenerate 2D semiconductors—SnSe₂ being n-type and BP being p-type. Despite the ease of forming type III band alignment due to the degeneracy, the low ambient stability and consequential surface oxidation make it difficult to achieve clean interfaces.⁸ Conversely, widely used 2D TMDs such as MoS₂ and WSe₂ can provide improved ambient stability. Thus, several reports have explored tunnel devices using MoS₂ and WSe₂ heterostructures. Roy et al. have reported a dual-gate MoS₂/WSe₂ heterojunction, which shows NDR behavior at low temperatures.¹³ Here, the dual-gate structure plays a key role in electrostatically doping the two

materials to split the band alignment. Additionally, Nourbakhsh et al. have shown room-temperature (RT) NDR with MoS₂/WSe₂ heterostructure with back-gate bias (V_{GS}) modulation.¹ Through calculated band diagrams, the authors determined the optimal thicknesses of the two materials that would allow tunneling in the transverse direction. However, the low I_{peak} of a few hundred pA should be improved for practical application.

In this work, we demonstrate RT gate-tunable MoS₂ and WSe₂ heterostructures. We use In/Au van der Waals (vdW) contacts for n-type transport in MoS₂¹⁴ and Pt vdW contacts for p-type transport in WSe₂,¹⁵ which help in boosting electron and hole injection, respectively. We compare the performance of the MoS₂/WSe₂ junctions when they are directly in contact with each other and when a thin hexagonal boron nitride (*h*-BN) tunnel barrier is inserted between them. We observe that the devices with a *h*-BN tunnel barrier and vdW contacts exhibit an I_{peak} of 315 μ A, which is among the highest values reported at RT.

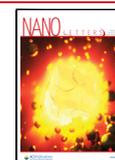
For the NDR, forming an effective p–n junction is necessary. We applied three strategies to form an effective p–n junction. First, for all devices, we have used WSe₂

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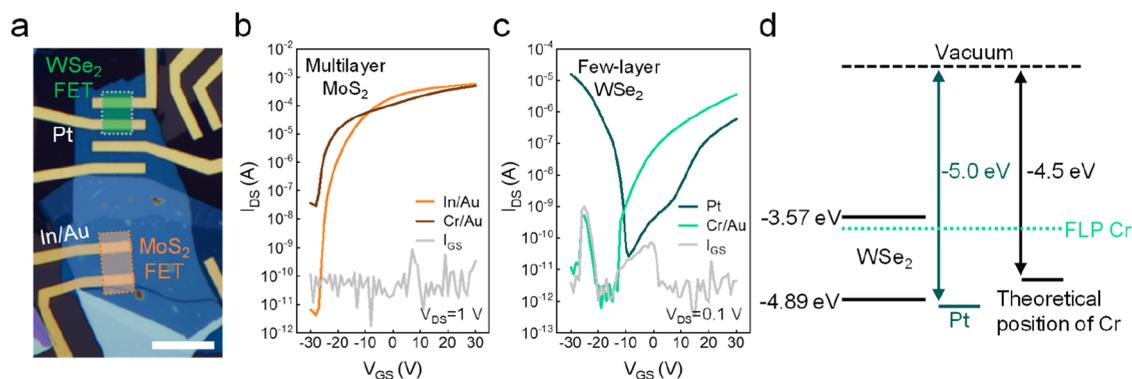


Figure 1. FET comparison of vdW and Cr/Au contacts. (a) OM image of MoS₂ and WSe₂ FETs. The scale bar is 10 μ m. (b,c) V_{GS} -dependent transfer curves of (b) multilayer MoS₂ and (c) few-layer WSe₂. Gray-colored curves represent gate-leakage current (I_{GS}). (d) Energy band alignment of WSe₂ and the metal contacts. FLP of Cr contacts induce n-type transport of WSe₂.

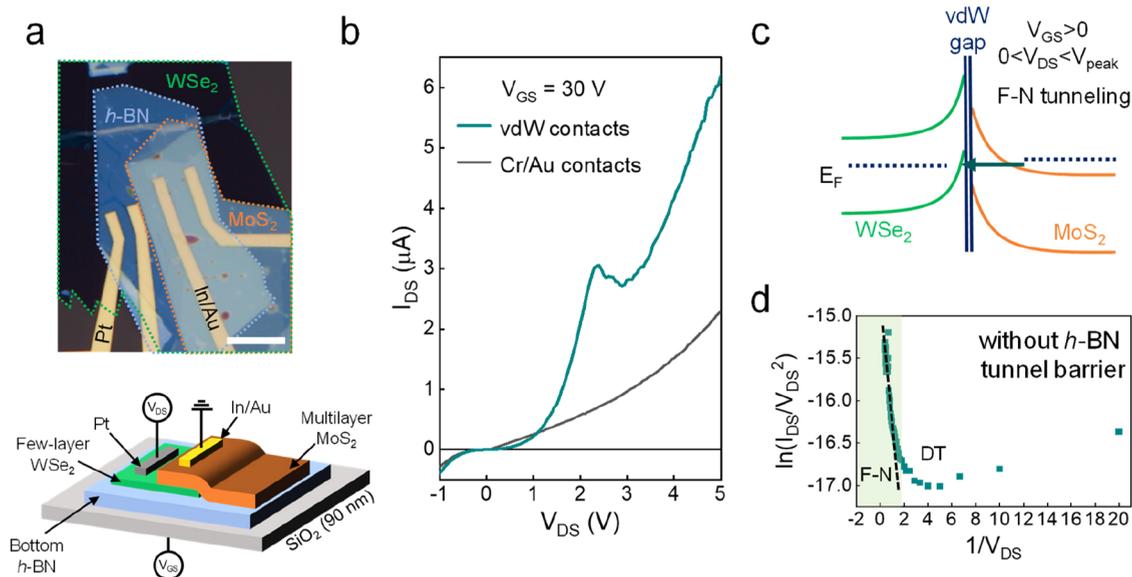


Figure 2. A comparison of NDR from FETs with vdW and Cr/Au contacts. (a, top) OM image of MoS₂/WSe₂ heterostructure devices. In/Au and Pt electrodes were used as electrical contacts on MoS₂ and WSe₂, respectively. The scale bar is 10 μ m. (bottom) A device schematic drawing of the device. (b) I - V curves of the vdW (green) and Cr/Au contacts (black). (c) Energy band diagram of the MoS₂/WSe₂ heterojunction with a vdW gap and F-N tunneling. The drawing is based on $V_{GS} > 0$, $0 < V_{DS} < V_{peak}$ conditions. (d) $\ln(I_{DS}/V_{DS}^2)$ versus $1/V_{DS}$ plot. Linear region (black dotted line) refers to the F-N tunneling.

consisting of two or three layers and MoS₂ of >10 layers, fabricated on h-BN on SiO₂ (90 nm)/Si substrates (device fabrication is described in detail in the Supporting Information, Experimental Methods). We selected the layer thicknesses based on an earlier study, which calculated the optimal thicknesses for NDR.¹ The use of h-BN as a substrate helps reduce hysteresis due to substrate traps,¹⁶ interface phonon scattering,¹⁷ and most importantly electron doping from SiO₂,¹⁵ essential for achieving p-type (WSe₂) and improving device performance (Figure S1). Finally, we used In (8 nm)/Au (80 nm) and Pt (20 nm capped with 60 nm of Au) vdW contacts for the MoS₂ and WSe₂ FETs, respectively. The optical microscope (OM) image of MoS₂ and WSe₂ FETs with vdW contacts is shown in Figure 1a. Our prior investigation revealed that vdW contacts, specifically In/Au on MoS₂ and Pt on WSe₂, exhibit distinct n- and p-type transport behavior, originating from clean metal/semiconductor interfaces that prevent Fermi-level pinning (FLP).^{14,15}

We compared the characteristics of FETs with vdW contacts with non-vdW contacts based on Cr (5 nm)/Au (80 nm), commonly used for 2D TMD FETs (Figure 1b and c). Both In/Au and Cr/Au contacts show n-type behavior,¹⁸ while In/Au contacts show an improved on/off ratio. In contrast, Cr/Au contacts on few-layer WSe₂ exhibit n-type transport while the vdW Pt contacts show p-type-dominant behavior.¹⁹ This result is consistent with previous studies showing that vdW contacts are effective in achieving p-type transport in WSe₂.^{15,20} In addition, temperature-dependent transport measurements showing stable transport behavior over a large temperature range are shown in Figure S2.

The p-type behavior with Pt vdW contacts can be understood by using the energy band diagram in Figure 1d. According to the band alignment, Cr/Au contact is expected to show ambipolar transport closer to p-type.^{21,22} However, for non-vdW contacts, defects are formed at the metal/semiconductor interface leading to FLP close to the conduction band (CB) of WSe₂,²³ which leads to n-type behavior of Cr/

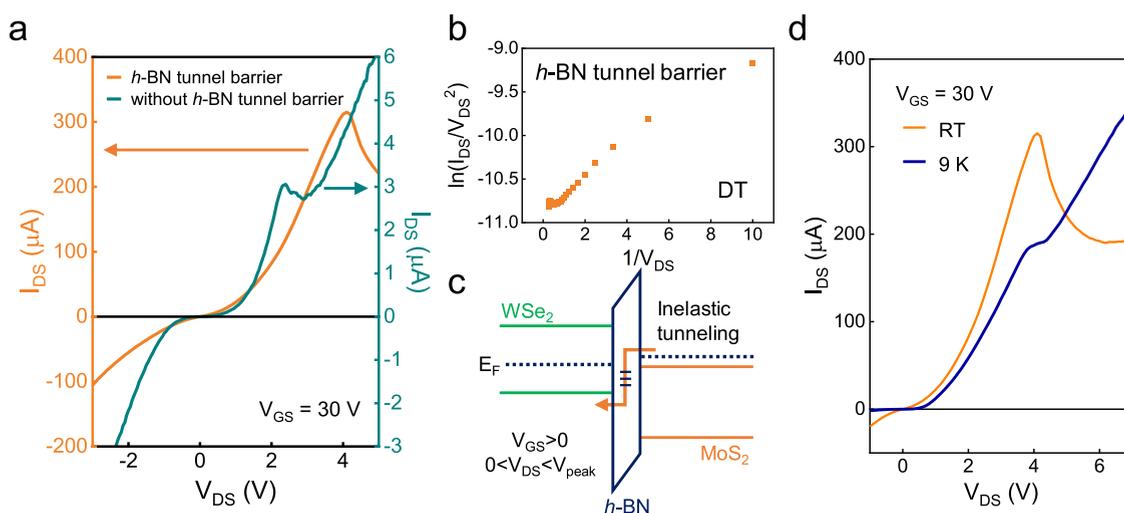


Figure 3. The role of the *h*-BN tunnel barrier. (a) I – V curves with *h*-BN tunnel barrier (orange) and without tunnel barrier (green). (b) $\ln(I_{\text{DS}}/V_{\text{DS}}^2)$ versus $1/V_{\text{DS}}$ plot depicting DT for the device with an *h*-BN tunnel barrier. (c) Energy band diagram of $\text{MoS}_2/\text{WSe}_2$ heterojunction with *h*-BN tunnel barrier. The drawing is based on $V_{\text{GS}} > 0$ and $0 < V_{\text{DS}} < V_{\text{peak}}$ conditions. (d) NDR behavior of the device with *h*-BN tunnel barrier at 9 K and RT.

Au- WSe_2 FETs.²⁴ In contrast, Pt deposition forms a vdW gap between the metal and WSe_2 , which follows the Pt work function. This leads to an effective hole injection for p-type WSe_2 .

Figure 2 describes the role of vdW contacts in heterostructure performance. We prepared two different sets of devices with identical configurations: a stack of multilayer MoS_2 flakes on top of few-layer WSe_2 on the *h*-BN bottom layer. In the first set of devices, we deposited In and Au on MoS_2 and Pt on WSe_2 . Figure 2a displays an OM image of a device along with a device schematic at the bottom. For comparison, we fabricated another set of devices with Cr/Au contacts (see Figure S3 for an OM image of such a device). We applied voltage (drain-source voltage, V_{DS}) to WSe_2 (drain) while MoS_2 (source) was grounded. The current–voltage (I – V) curves of these two types of devices, measured at RT, are plotted in Figure 2b (the V_{GS} -dependent I – V curves are presented in Figure S4). The devices with vdW contacts exhibit a clear NDR, whereas it is absent in devices with Cr/Au contacts. The observation of NDR in the devices with vdW contacts is evidence of tunneling (the I_{DS} – V_{GS} curve is depicted in Figure S5).

To observe NDR in the forward bias region ($V_{\text{DS}} > 0$) of a p–n junction, a type III junction, with a broken band alignment at $V_{\text{DS}} = 0$ V is needed. Type III junctions can form when both p- and n-type semiconductors are highly doped and are in a degenerate state. However, the materials that we used (MoS_2 and WSe_2) are not in a degenerate state. Moreover, unlike a dual gate structure,¹³ global V_{GS} makes it difficult to control the carrier density of each material separately. Notably, in our heterostructures, NDR shows a more distinct trend at $V_{\text{GS}} > 0$, which is also observed in previous works.^{12,25} We attribute this to steep band bending of a few layers of WSe_2 with better V_{GS} coupling due to its proximity to the gate and slight bending of multilayer MoS_2 due to screening from WSe_2 (Figure 2c). At $0 < V_{\text{DS}} < 2.35$ V (peak voltage, V_{peak}), the electrons from the MoS_2 tunnel through the thin triangular barrier and reach WSe_2 . With increasing forward bias, the overlap between the MoS_2 CB and the WSe_2 VB closes the thin triangular tunnel path, and therefore the tunneling current

begins to decrease, thereby showing NDR. Conversely, the case differs when Cr/Au contacts are employed. Because the Fermi-level is pinned, WSe_2 band bending cannot occur effectively under V_{GS} variation. Hence, the MoS_2 electrons will face the midband gap state of WSe_2 due to the forming of a small triangular barrier. The tunnel transport mechanism is depicted in Figure 2d to validate the tunnel transport mechanism. The I – V curve in the region of $0 < V_{\text{DS}} < V_{\text{peak}}$ can be modeled using the Simmons approximation.²⁶ The Fowler–Nordheim (F–N) tunnelling can be expressed as

$$I_{\text{FNT}} \propto V^2 \exp\left(-\frac{8\pi d\sqrt{2m^*\varphi^3}}{3heV}\right)$$

Here, d represents the thickness of the tunnel barrier, m^* denotes the effective electron mass, φ corresponds to the tunnelling barrier height, and h is the Planck constant. Plotting $\ln(I/V^2)$ versus $1/V$ should reveal a linear regime with a negative slope (black dotted line) for F–N tunnelling.^{27,28} From the slope of the curve, we can derive the F–N tunneling barrier height (φ) of 0.11 eV.

We further validate the occurrence of F–N tunneling in our devices through temperature-dependent transport measurements. In Figure S6, we present the temperature-dependent I – V curves from a device showing NDR with In/Au and Pt contacts. Here, we can observe that the steep increase of tunnelling current in the reverse bias region ($V_{\text{DS}} < 0$ V) is insensitive to changes in temperature. Furthermore, the F–N tunnelling current, which is the increase in current in the forward bias region preceding the NDR effect ($0 < V_{\text{DS}} < V_{\text{peak}}$), also shows a negligible temperature dependence. However, beyond the NDR effect, the current flow is governed by thermionic emission and is highly sensitive to changes in temperature (Figure S6, inset). The results in Figures 2b,d and S6 suggest that the vdW gap between $\text{MoS}_2/\text{WSe}_2$ alongside the contribution of F–N tunneling is critical.

Next, we integrated 10 layers (3.4 nm) of *h*-BN between MoS_2 and WSe_2 . The insertion of *h*-BN as a tunnel barrier serves as an insulating spacer that enables precise band alignment.^{17,29,30} The insulating nature of *h*-BN results in

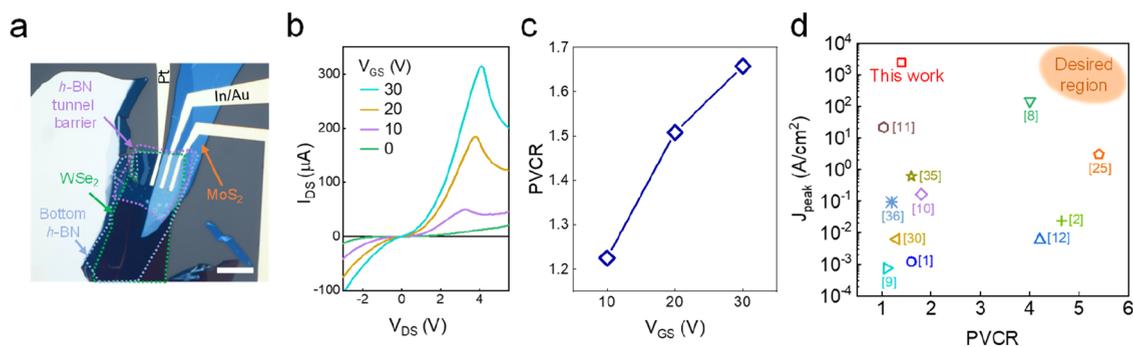


Figure 4. V_{GS} -dependent NDR with h -BN tunnel barrier. (a) OM image of the heterostructure. The scale bar is 10 μm . (b) V_{GS} -dependent NDR. (c) V_{GS} -dependent PVCR and the (d) benchmark of J_{peak} versus PVCR for various reported 2D NDR devices based on tunnelling that operate at RT. The transverse tunnelling transistor³¹ is not included in this plot due to a different operation mechanism and lack of device size information.

sharper band edges for both MoS_2 and WSe_2 . Consequently, the energy levels of the VB and CB experience a sharp transition at the MoS_2/h -BN and WSe_2/h -BN interfaces, resulting in a well-defined tunnel barrier. However, at the same time, it requires extra energy for the electrons to tunnel through the barrier. Also, due to additional stacking steps during fabrication and natural defects in the h -BN crystal, unintentional trap sites may be involved.³¹ The difference in the transport behavior between two devices with and without the h -BN tunnel barrier at RT is shown in Figure 3a. Both devices show clear NDR behavior. However, the device with the h -BN tunnel barrier (left y axis, orange) displays a substantial increase (2 orders of magnitude) in I_{peak} compared to the device without the tunnel barrier (right y axis, green). Additionally, we observe an increase in the V_{DS} , from 2.35 to 4.1 V, required to reach the I_{peak} . We attribute this to the presence of an additional tunnel barrier (h -BN), which necessitates a higher voltage for carriers to reach the opposite side (WSe_2) of the energy band.

To explore the mechanism for higher I_{peak} , the I - V curve in the forward bias region ($0 < V_{\text{DS}} < V_{\text{peak}}$) is studied. Unlike the F-N tunnelling observed in Figure 2d, Figure 3b follows a logarithmic slope, meaning the device incorporating the h -BN tunnel barrier operates via direct tunnelling (DT).³² The DT current can be expressed as

$$I_{\text{DT}} \propto V \exp\left(-\frac{4\pi d \sqrt{2m^* \phi}}{h}\right)$$

The possible energy band alignment due to DT transport through the h -BN tunnel barrier is shown in Figure 3c. Although precise band alignment is difficult to extract and varies from study to study,^{1,13,27} we can imagine the presence of inelastic tunnelling such as phonon-assisted, trap-assisted, or Shockley-Read-Hall tunnelling.^{13,33,34} To obtain more insight, we plotted the NDR behavior of the h -BN tunnel barrier device at 9 K and RT for comparison (Figure 3d). It shows a distinct increase in the current at RT, and such a temperature-dependent enhancement is absent in devices without an h -BN tunnel barrier (Figure S6). This leads to a higher I_{peak} and a larger peak-to-valley current ratio (PVCR) at higher temperatures due to thermally enhanced inelastic tunnelling. Thus, we believe that combined effects including the sharp band edges as well as inelastic tunnelling through the h -BN barrier are important for the enhanced I_{peak} .

The properties of devices with the h -BN tunnel barrier were further examined by varying V_{GS} . Figure 4a shows an OM image of a typical device. The three-layer thickness of WSe_2 enables effective gate tunability of the Fermi level, while the effect of the V_{GS} on the relatively thick (10 layers) MoS_2 is small. The thicknesses of the layers measured by atomic force microscopy (AFM) topography are presented in Figure S7. Electrical bias was applied to the Pt contact connected to WSe_2 , while the current was collected from the In/Au contact on MoS_2 . The gate bias was applied by global V_{GS} (SiO_2/Si). The V_{GS} dependence of the NDR at RT is plotted in Figure 4b. With increasing V_{GS} , the NDR becomes more pronounced, resulting in higher current levels.^{12,25} This behavior can be attributed to the accumulation of electrons in MoS_2 as $V_{GS} > 0$, providing a large number of carriers available for tunnelling when a forward bias is applied.

The energy band alignment of the WSe_2/h -BN/ MoS_2 device under varying applied V_{DS} is illustrated in Figure S8. When reverse bias ($V_{\text{DS}} < 0$) is applied, it allows the tunnelling of electrons from filled states in WSe_2 through the h -BN barrier to reach the unoccupied states in the MoS_2 CB. This tunnelling phenomenon results in a sharp increase in current as a larger negative V_{DS} is applied. Conversely, when positive voltage ($V_{\text{DS}} > 0$) is applied, the direction of carrier injection reverses. Electrons in the MoS_2 CB tunnel through the barrier to reach the WSe_2 , leading to an inelastic tunnelling current. This current continues to increase until it reaches the maximum value, I_{peak} . Beyond V_{peak} , electrons from MoS_2 face the midband gap state of the WSe_2 , where no density of states exists. Thus, the current decreases. Notably, some hot electrons may still overcome this barrier and contribute to the valley current (I_{valley}). Subsequently, when thermionic emission provides sufficient energy for MoS_2 electrons to transit to the WSe_2 CB, as in a normal diode, the current once again begins to rise.

We extracted the PVCR, which exhibits an increasing trend as V_{GS} increases (Figure 4c). The overall PVCR value is not exceptionally high due to the presence of a substantial I_{valley} . This can be attributed to a high probability of inelastic tunnelling and thermally excited electrons across the tunnel barrier. Consequently, this results in a relatively small overall PVCR value. Nonetheless, the increase in I_{peak} surpasses the rise in I_{valley} , leading to an elevation in PVCR as V_{GS} increases.

To benchmark our results, in Figure 4d we have plotted the J_{peak} (peak current density, $I_{\text{peak}}/\text{device working area}$) and PVCR from other devices based on the heterostructure of 2D semiconductors.^{1,2,8-12,25,30,35,36} Among various types of

devices employing different 2D materials, principles, and environments, we have selected devices based on tunneling that operate at RT. Our devices exhibit a large I_{peak} of 2420 A/cm². A further increase in PVCR could be accomplished by exploring materials with different band gaps and higher doping levels, as well as carefully controlling the inelastic tunneling to minimize the I_{valley} . It is noteworthy that the transverse tunnelling transistor demonstrated by Xiong et al.³¹ using black phosphorus exhibits a large I_{peak} and PVCR simultaneously. Employing transverse tunneling may be an alternative route to improve the PVCR.

In summary, our findings demonstrate a high I_{peak} NDR device by using vdW heterostructures. The utilization of In/Au and Pt vdW contacts facilitates the effective formation of the p–n junction. The devices show NDR, facilitated by F–N tunneling through a triangular barrier induced by applied V_{GS} . Furthermore, integration of the *h*-BN tunnel barrier leads to improved NDR because of sharp band edges as well as inelastic tunnelling. This result yields high I_{peak} values. These results pave the way for potential applications in logic devices and oscillators.

■ ASSOCIATED CONTENT

SI Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acs.nanolett.3c04607>.

Role of *h*-BN as a substrate, temperature-dependent transport of MoS₂ and WSe₂ with vdW contacts, OM image of the Cr/Au device, V_{GS} -dependent I – V curves of the MoS₂/WSe₂ heterostructure with vdW contacts and Cr/Au contacts, V_{DS} -dependent transfer curves of the MoS₂/WSe₂ heterostructure, temperature-dependence of the NDR device, thickness of each layer of the heterostructure, energy band diagram of the heterostructure, OM and I – V characteristics of additional NDR devices, experimental methods (PDF)

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Author Contributions

M.C. designed and supervised the project. J.H.K. fabricated samples, performed experiments, and analyzed the data. S.S. and Y.W. supported the data analysis. T.T. and K.W. provided the bulk *h*-BN crystals. J.H.K. and M.C. wrote the manuscript with support from S.S. and Y.W. All authors discussed the results and commented on the manuscript.

Notes

The authors declare no competing financial interest.

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■ REFERENCES

- (1) Nourbakhsh, A.; Zubair, A.; Dresselhaus, M. S.; Palacios, T. Transport Properties of a MoS₂/WSe₂ Heterojunction Transistor and Its Potential for Application. *Nano Lett.* **2016**, *16*, 1359–1366.
- (2) Seo, S.; et al. A Van Der Waals Reconfigurable Multi-Valued Logic Device and Circuit Based on Tunable Negative-Differential-Resistance Phenomenon. *Adv. Mater.* **2022**, *34*, 2202799.
- (3) Lin, J. C.; et al. Porous Silicon NDR-Based High Power RF Oscillator Diode. *IEEE Electron Device Lett.* **2017**, *38*, 701–704.
- (4) Woo, G.; Kim, T.; Yoo, H. Band-to-Band Tunneling Control by External Forces: A Key Principle and Applications. *Adv. Electron Mater.* **2023**, *9*, 2201015.
- (5) Mehdi, I.; Haddad, G. I.; Mains, R. K. Performance Criteria for Resonant Tunneling Diodes as Millimeter-Wave Power Sources. *Microw Opt Techn Lett* **1989**, *2*, 172–175.
- (6) Zhang, Z. H.; et al. Toward High-Peak-to-Valley-Ratio Graphene Resonant Tunneling Diodes. *Nano Lett.* **2023**, *23*, 8132–8139.
- (7) Geim, A. K.; Grigorieva, I. V. Van der Waals heterostructures. *Nature* **2013**, *499*, 419–425.
- (8) Fan, S. D.; et al. Tunable Negative Differential Resistance in van der Waals Heterostructures at Room Temperature by Tailoring the Interface. *ACS Nano* **2019**, *13*, 8193–8201.
- (9) Cong, X. N.; et al. Efficiently band-tailored type-III van der Waals heterostructure for tunnel diodes and optoelectronic devices. *Nano Res.* **2022**, *15*, 8442–8450.
- (10) Yan, R. S.; et al. Esaki Diodes in van der Waals Heterojunctions with Broken-Gap Energy Band Alignment. *Nano Lett.* **2015**, *15*, 5791–5798.
- (11) Na, J.; Kim, Y.; Smet, J. H.; Burghard, M.; Kern, K. Gate-Tunable Tunneling Transistor Based on a Thin Black Phosphorus-SnSe₂ Heterostructure. *ACS Appl. Mater. Inter* **2019**, *11*, 20973–20978.
- (12) Shim, J.; et al. Phosphorene/rhenium disulfide heterojunction-based negative differential resistance device for multi-valued logic. *Nat. Commun.* **2016**, *7*, 13413.
- (13) Roy, T.; et al. Dual-Gated MoS₂/WSe₂ van der Waals Tunnel Diodes and Transistors. *ACS Nano* **2015**, *9*, 2071–2079.

- (14) Wang, Y.; et al. Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature* **2019**, *568*, 70–74.
- (15) Wang, Y.; et al. P-type electrical contacts for 2D transition-metal dichalcogenides. *Nature* **2022**, *610*, 61–66.
- (16) Illarionov, Y. Y.; et al. The role of charge trapping in MoS₂/SiO₂ and MoS₂/hBN field-effect transistors. *2D Mater.* **2016**, *3*, 035004.
- (17) Knobloch, T.; et al. The performance limits of hexagonal boron nitride as an insulator for scaled CMOS devices based on two-dimensional materials. *Nat. Electron* **2021**, *4*, 98–108.
- (18) Schranghamer, T. F.; et al. Ultrascaled Contacts to Monolayer MoS₂ Field Effect Transistors. *Nano Lett.* **2023**, *23*, 3426–3434.
- (19) Oberoi, A.; et al. Toward High-Performance p-Type Two-Dimensional Field Effect Transistors: Contact Engineering, Scaling, and Doping. *ACS Nano* **2023**, *17*, 19709–19723.
- (20) Kong, L. G.; et al. Doping-free complementary WSe₂ circuit via van der Waals metal integration. *Nat. Commun.* **2020**, *11*, 1866.
- (21) Zatko, V.; et al. Band-Gap Landscape Engineering in Large-Scale 2D Semiconductor van der Waals Heterostructures. *ACS Nano* **2021**, *15*, 7279–7289.
- (22) Liu, C. S.; et al. Various and Tunable Transport Properties of WSe₂ Transistor Formed by Metal Contacts. *Small* **2017**, *13*, 1604319.
- (23) Kim, C.; et al. Fermi Level Pinning at Electrical Metal Contacts of Monolayer Molybdenum Dichalcogenides. *ACS Nano* **2017**, *11*, 1588–1596.
- (24) Pudasaini, P. R.; et al. High-performance multilayer WSe₂ field-effect transistors with carrier type control. *Nano Res.* **2018**, *11*, 722–730.
- (25) Afzal, A. M.; et al. High performance and gate-controlled GeSe/HfS₂ negative differential resistance device. *RSC Adv.* **2022**, *12*, 1278–1286.
- (26) Simmons, J. G. Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film. *J. Appl. Phys.* **1963**, *34*, 1793–1803.
- (27) Doan, M. H.; et al. Charge Transport in MoS₂/WSe₂ van der Waals Heterostructure with Tunable Inversion Layer. *ACS Nano* **2017**, *11*, 3832–3840.
- (28) Srivastava, P. K.; et al. Van der Waals Broken-Gap p-n Heterojunction Tunnel Diode Based on Black Phosphorus and Rhenium Disulfide. *ACS Appl. Mater. Inter* **2019**, *11*, 8266–8275.
- (29) Britnell, L.; et al. Field-Effect Tunneling Transistor Based on Vertical Graphene Heterostructures. *Science* **2012**, *335*, 947–950.
- (30) Movva, H. C. P.; et al. Room Temperature Gate-tunable Negative Differential Resistance in MoS₂/hBN/WSe₂ Heterostructures. *74th Annual Device Research Conference*, June 19–22, 2016; Institute of Electrical and Electronics Engineers (IEEE), 2016; pp 1–2. DOI: 10.1109/DRC.2016.7548486.
- (31) Xiong, X.; et al. A transverse tunnelling field-effect transistor made from a van der Waals heterostructure. *Nat. Electron* **2020**, *3*, 106–112.
- (32) Ahmed, F.; Choi, M. S.; Liu, X.; Yoo, W. J. Carrier transport at the metal-MoS₂ interface. *Nanoscale* **2015**, *7*, 9222–9228.
- (33) Lee, C. H.; et al. Atomically thin p–n junctions with van der Waals heterointerfaces. *Nat. Nanotechnol* **2014**, *9*, 676–681.
- (34) Hansma, P. K. Inelastic Electron-Tunneling. *Phys. Rep.* **1977**, *30*, 145–206.
- (35) Fan, S.; Yun, S. J.; Yu, W. J.; Lee, Y. H. Tailoring Quantum Tunneling in a Vanadium-Doped WSe₂/SnSe₂ Heterostructure. *Adv. Sci.* **2020**, *7*, 1902751.
- (36) Wang, J. X.; et al. Vertical WS₂/SnS₂ van der Waals Heterostructure for Tunneling Transistors. *Sci. Rep* **2018**, *8*, 17755.