MNE 23 (2024) 100246

Contents lists available at ScienceDirect

Micro and Nano Engineering

journal homepage: www.sciencedirect.com/journal/micro-and-nano-engineering

2D BDiode – A switchable bidirectional diode for analog electronic circuits fabricated entirely from 2D materials

Christian D. Matthus [a,*], Phanish Chava [b], Kenji Watanabe [c], Takashi Taniguchi [d], Thomas Mikolajick [e], Artur Erbe [b]

[a] Chair for Circuit Design and Network Theory, Technische Universität Dresden, Dresden 01069, Germany
[b] Institute of Ion Beam Physics and Materials Research, Helmholtz Zentrum Dresden-Rossendorf, Dresden 01328, Germany
[c] Research Center for Electronic and Optical Materials, National Institute for Materials Science, 1-1 Namiki, Tsukuba 305-0044, Japan
[d] Research Center for Materials Nanoarchitectonics, National Institute for Materials Science, 1-1 Namiki, Tsukuba 305-0044, Japan
[e] Chair of Nanoelectronics, Technische Universität Dresden, Dresden 01069, Germany

ARTICLE INFO

Keywords:
2D materials
DC/AC converter
AC/DC converter
Charge pump
SPICE modeling
Heterojunction diode
2D BDiode

ABSTRACT

The advent of two-dimensional (2D) materials has led to innovative and compact electronic devices with remarkable properties. In this work, we introduce a switchable bidirectional diode (2D BDiode), fabricated entirely using different 2D materials, that serves as a fundamental building block for various analog circuit applications. This proof-of-concept diode exhibits the ability to control the flow of current in both forward and reverse bias configurations, enabling advanced functionality in the realm of analog circuit design. We provide a SPICE-based model for the diode based on current-voltage device characterization, capturing its behavior under different biasing conditions, and finally demonstrate a few potential use cases of the 2D BDiode including AC/DC conversion, DC/AC conversion and charge pump circuits.

1. Introduction

The discovery of graphene and its analogous two-dimensional (2D) materials opened up the possibility of investigating electronic devices built entirely using heterostructures of different 2D materials [1]. Semiconducting 2D material-based heterostructures are of great interest due to their wide range of (opto)-electronic applications, especially for flexible electronics [2]. Recently, we reported a proof-of-concept device based on semiconducting WSe_2/MoS_2 heterojunction and showed the usability of such a device as a field effect transistor [3] as well as a cryogenic temperature sensor [4]. Typically, sensor devices need analog frontend circuitry. Hence, there is a need for analog electronic devices based on 2D materials. Compared to conventional semiconductor devices, 2D materials enable the fabrication of hetero-interfaces with minimal defects owing to their atomically sharp surfaces. Furthermore, due to their atomically thin nature, the carrier transport varies compared to traditional semiconductor devices e.g., Si Complementary Semiconductor Metal Oxide Semiconductor (CMOS) devices [4]. Circuits built of 2D materials are in the focus of research since several years. Especially within the last decade, much has happened concerning functional integrated as well as reconfigurable 2D devices and circuits. Some exciting results can be found e.g., in [5–14]. Moreover, recent developments target the applicability of 2D materials for analog circuits [15–17] including SPICE modeling of the devices [18–20].

In this paper, we describe the effect of different carrier transport mechanisms in a heterojunction pn-diode triggered by a back-gate electrode. The physics behind this effect were analyzed and a straightforward SPICE model was implemented. Finally, we show some possible applications in analog circuit design offering new possibilities for future integrated circuits based on 2D materials.

2. Device fabrication

The presented device consists entirely of 2D materials. The fabrication process begins by mechanically exfoliating few-layered graphene (FLGr), hexagonal boron nitride (hBN), WSe_2, and MoS_2 which are transferred onto different poly(dimethylsiloxane) PDMS substrates using scotch tape. Suitable homogeneous flakes for stacking are identified using an optical microscope. These flakes are subsequently stacked together using the dry stamping technique [21]. A step-by-step process

* Corresponding author at: Chair for Circuit Design and Network Theory, Technische Universität Dresden, Dresden 01069, Germany.
E-mail address: christian.matthus@tu-dresden.de (C.D. Matthus).

https://doi.org/10.1016/j.mne.2024.100246
Received 16 November 2023; Received in revised form 11 March 2024; Accepted 16 March 2024
Available online 21 March 2024

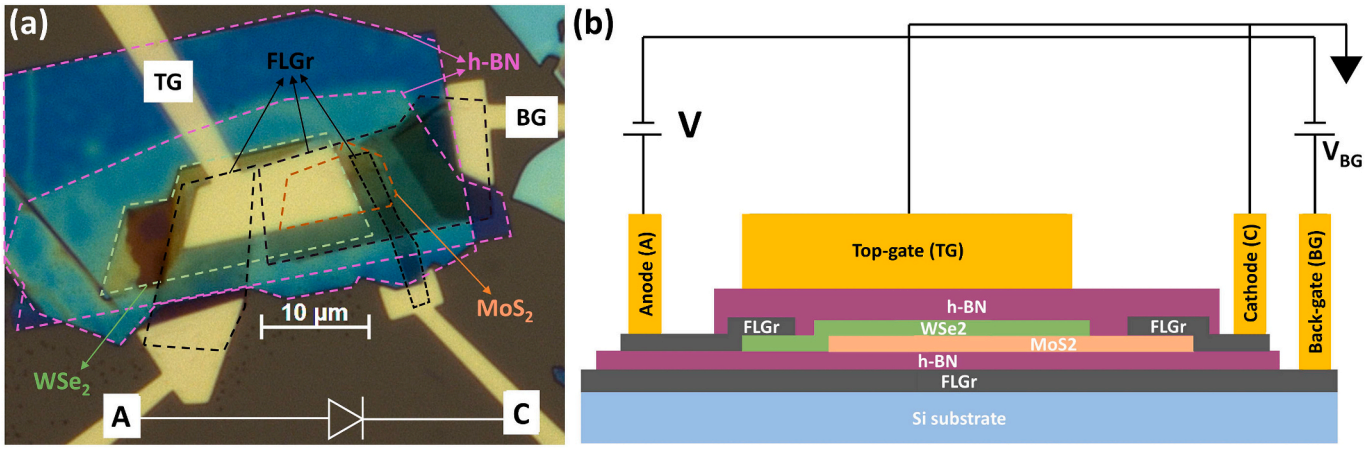

Fig. 1. (a) Optical micrograph of the fabricated device indicating different layers of 2D materials used. (b) Cross-sectional device schematic with electrical connections, which include the anode (WSe_2 contact), cathode (MoS_2 contact), back-gate, and top gate, while the latter is connected to ground for all measurements.

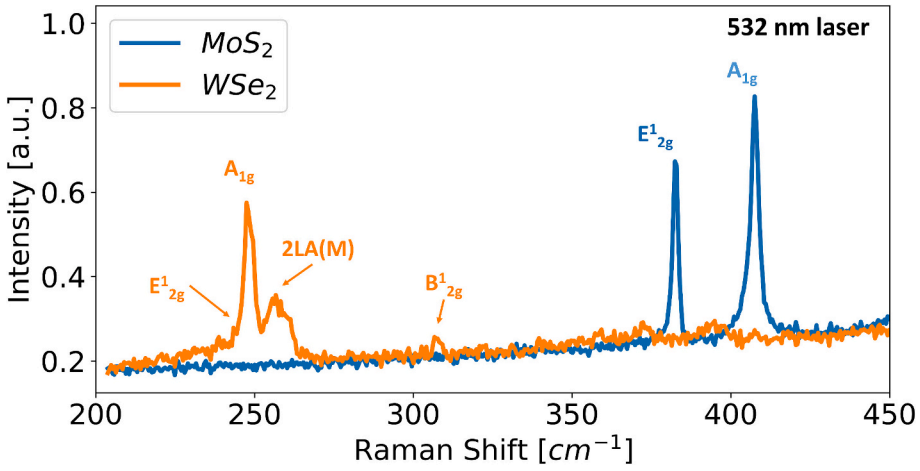

Fig. 2. Raman spectra of the exfoliated MoS_2 and WSe_2 flakes on PDMS substrate.

flow for a similar device is also illustrated in our recent work [4]. The heterostructure assembly is carried out on a highly p-doped silicon substrate with a thermally oxidized surface, having an oxide thickness of 285 nm. The entire assembly process is conducted within a glove-box environment filled with nitrogen to avoid interlayer contamination as well as ambient degradation of sensitive materials. Following the heterostructure assembly, the sample is transferred outside the glove-box to characterize the thicknesses of the individual 2D layers using atomic force microscopy. The thicknesses of the WSe_2 and MoS_2 are approximately 5 nm and 3 nm respectively, while the thicknesses of top and bottom hBN are 9 nm and 12 nm respectively. The thicknesses of the FLGr electrodes are between 6 nm and 10 nm.

The next step is to design and pattern contact electrodes, which is performed with the help of electron beam lithography. Finally, the anode, cathode, and gate electrodes are deposited consisting of a 10 nm/50 nm Ni/Au metal stack. Fig. 1 shows the optical micrograph of the fabricated device along with a cross-sectional device schematic indicating the contact electrodes, measurement configuration, and the vertically stacked 2D layers. We chose semiconducting layers of partially overlapped WSe_2 and MoS_2 to construct the p-n junction diode. The Raman spectra of individual flakes are shown in Fig. 2. The MoS_2 spectrum shows two clear peaks corresponding to the vibrational modes E^1_{2g} and A_{1g} having a separation of about 30 cm^{-1}, which is associated to more than 5 monolayers of MoS_2 [22]. The Raman spectrum of WSe_2 shows multiple peaks between 200-400 cm^{-1}, which corresponds to multilayered WSe_2 as a monolayer spectrum only has a single peak around 250 cm^{-1} [23].

Semi-metallic FLGr is used as the intermediate contact material to the semiconducting layers to suppress the effect of Fermi level pinning of the metal stack to the semiconductors. An additional layer of FLGr and insulating hBN forms the back-gate stack for our diode, the polarity of which controls the direction of current flow in the diode as will be seen in the following sections. The top side is passivated and encapsulated, respectively, by hBN. Additionally, a metal electrode was deposited and patterned on top of the pn-junction, which can be used as another (top gate) electrode. Devices with two gates are currently getting much attention in the field of Si CMOS circuit design for various applications, e.g., using fully-depleted silicon on insulator (FDSOI) technologies. In this case, the back-gate is used, e.g. for calibrating or tuning critical components tackling timing or matching issues [24]. However, the scope of this paper is the investigation of the influence of one gate electrode on the device behavior of a complex new device and its possible applications. Hence, the top gate electrode was connected to ground for all the measurements discussed in this paper.

3. Device characterization and modeling

3.1. Measurement setup

The diode was initially characterized at room temperature inside a

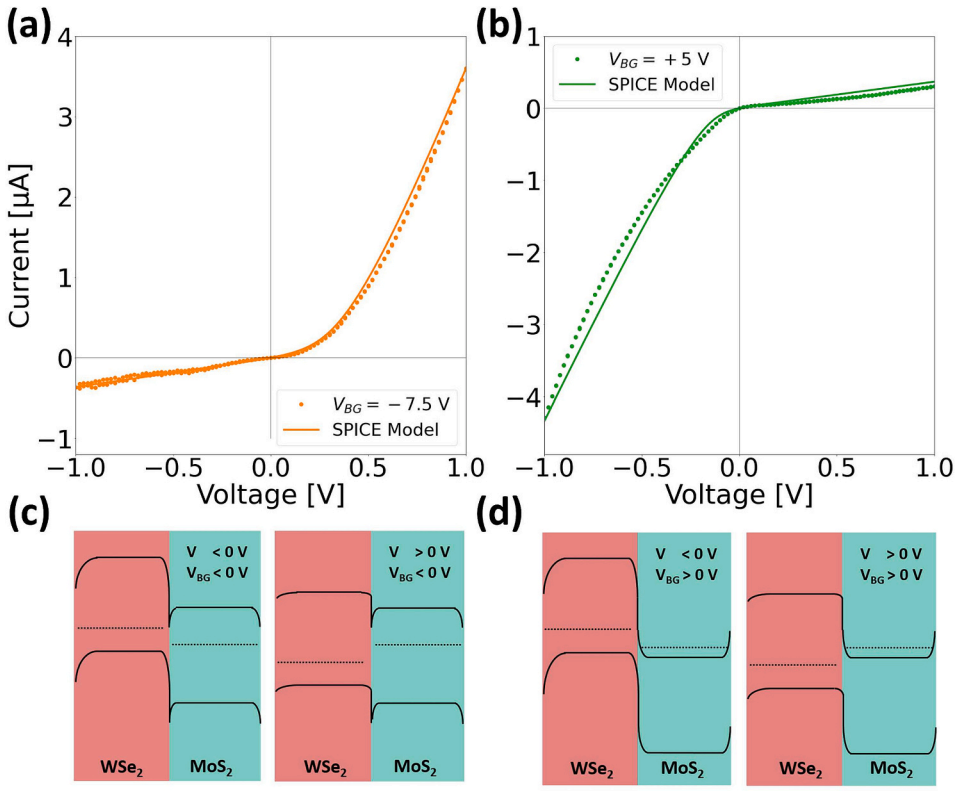

Fig. 3. Measured I-V characteristics and semi-empirical model of the 2D BDiode for back-gate voltage of −7.5 V (a) and 5 V (b) for SPICE simulations, and band diagrams in forward and reverse direction with respect to diode (anode-cathode) voltage for negative (c) and positive back-gate biasing (d).

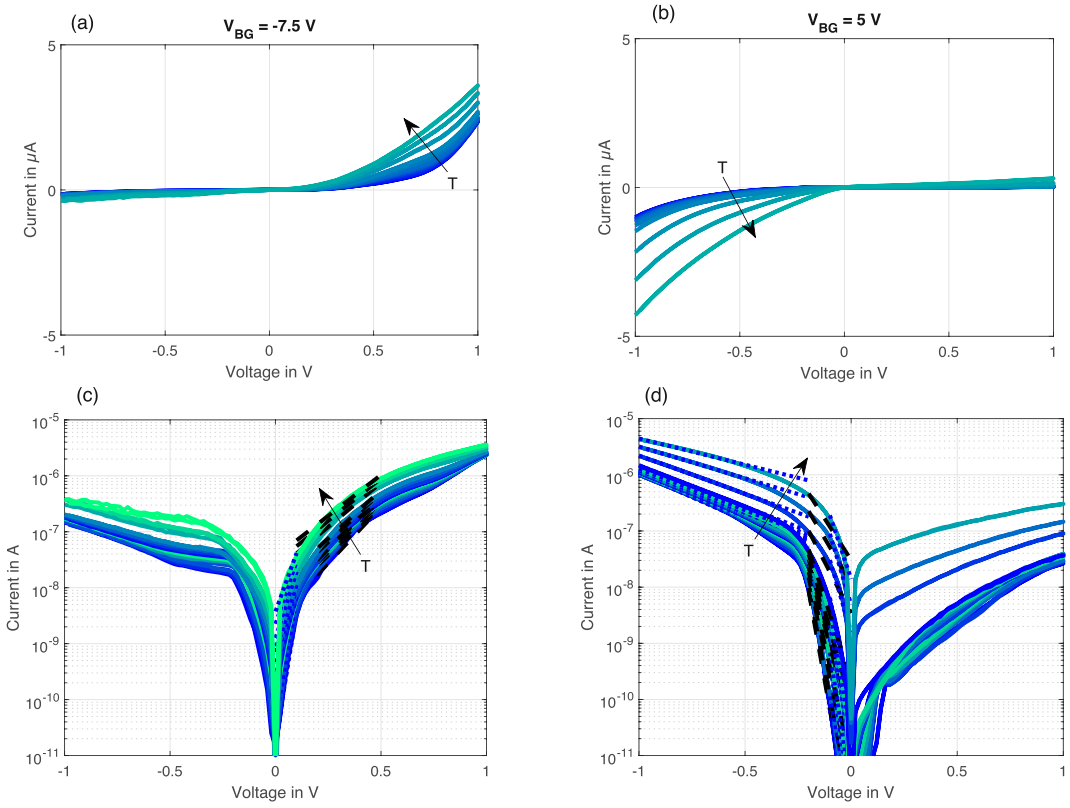

Fig. 4. Temperature dependent I-V characteristics for device 2 at different configurations of back-gate bias ($V_{BG} = -7.5V, V_{BG} = +5V$) in linear (a-b) and semi-logarithmic scales (c-d) respectively. The temperature span is from 20 K to 300 K.

vacuum chamber (Lakeshore Model CPX-VF), with a pressure of about 1×10^{-5} mbar. The electrical measurements were recorded with the help of 4155C Agilent semiconductor parameter analyzer. First, both gates are connected to ground and the diode voltage (V) is swept from −1 V to 1 V while recording the current simultaneously. This measurement is then repeated for different values of back-gate voltage while the top gate is still grounded. Since we source voltages from the WSe_2 side (anode) of the junction and ground the MoS_2 side (cathode), it should be noted that a positive (negative) diode voltage corresponds to forward (reverse) bias according to general p-n junction biasing convention. Additionally, a temperature sweep was also conducted for a detailed analysis of the device physics which includes the study of different transport mechanisms and determination of activation energies using an Arrhenius diagram as discussed in our previous reports for another device (device 1) [3,4]. In the present work, we use a quite similar device (device 2) and we analyzed it in a comparable manner, which is briefly described in the following section, while further information can be found in the supplementary material. However, to demonstrate the applications shown in Section 4, we concentrate specifically on room temperature measurements.

3.2. Device characterization and carrier transport mechanisms

Fig. 3(a) and (b) show the measured diode characteristics for a selected negative ($V_{BG} = -7.5$ V) and positive ($V_{BG} = 5$ V) bias configuration of back-gate voltage. Additional measurements with different back-gate voltages can be found in the supplementary material. We chose appropriate back-gate voltage conditions to achieve the highest symmetry for both directions. Hence, we used dissimilar bias levels on the back-gate for positive ($V_{BG} = 5$ V) and negative ($V_{BG} = -7.5$ V) configurations in order to maintain nearly symmetrical current levels in both cases. We will briefly describe the carrier transport mechanisms for both cases of the back-gate polarity. When a negative voltage is applied to the back-gate, it can be seen that the diode current exponentially increases in forward bias, while it is suppressed in the reverse bias condition. The behavior is similar to that of a conventional pn-junction diode. It is related to the diffusion of carriers into the depletion region and the diffusion areas close to the junction [25]. This can also be understood from the simplified energy band diagrams as illustrated in Fig. 3(c-d). It should be noted that the influence of the back-gate on the WSe_2 side of the junction is negligible, since MoS_2 being under the WSe_2 flake screens the vertical electric field.

On applying a positive bias to the back-gate, the behavior changes completely and the diode is conductive in the reverse bias instead. This behavior is explained by band-to-band tunneling (BTBT) of carriers from the conduction band of MoS_2 to the valence band of WSe_2, which has also been reported previously for the same material system [26–30]. In reverse bias, a tunneling window is formed between the two semiconductors as the heterojunction band alignment transitions from a staggered alignment to a broken alignment [31]. The current is suppressed in the forward bias owing to a large barrier at the WSe_2/MoS_2 junction as also seen in the case of reverse bias when a negative back-gate voltage is applied. Measurements at different temperatures are typically used to get a deeper understanding of the conduction mechanisms involved. As mentioned above, we already performed such an analysis for device 1 in our previous work [4] and we did so in a similar manner for the device investigated here (device 2). The I-V characteristics measured in a temperature range spanning from 20 K up to 300 K are shown in Fig. 4 in linear (a-b) and semi-logarithmic scale (c-d) for the back-gate voltages of −7.5 V and + 5 V respectively.

We performed the simplest regression for the respective conductive regimes of the diode (cf. Eq. 1). Since here parasitics such as the quite high contact resistance limit the diode current, the I-V characteristics do not show a straight line in a semi-logarithmic representation like an ideal diode. In order to derive values for saturation current $I_{D,sat}$ and ideality factor n, we used different regressions for different bias levels for each temperature shown as broken and dotted lines in Fig. 4. The quantitative results of this analysis and a brief discussion can be found in the supplementary material. For the linear regression, we neglected in a first-term approximation the influences of series and parallel resistances. For the modeling of the device for analog circuit application, on the other hand, it is very important to include both in the compact model as shown below. As an overall result, we observed different activation energies and different values for the ideality factor for different back-gate bias levels, especially when changing its polarity. We see this as a proof that our speculation of the different carrier transport mechanisms for different back-gate bias polarities seems to be valid. Note that we observed a similar effects, i.e., possibility of switching the polarity of the diode by the back-gate voltage, for the device of our previous work (device 1) as can be seen in the supplementary material.

Table 1
Empirical values of model parameters used for SPICE modeling.

Model Parameters	$V_{BG} = -7.5V$	$V_{BG} = 5V$
R_{par} [$M\Omega$]	2.8	2.8
$I_{D,sat}$ [nA]	10	8
R_s [$k\Omega$]	185	160
n [−]	1.7	3.1

3.3. SPICE modeling

After investigating the transport mechanisms behind the observed I-V characteristics, we went one step further towards applying this device to an integrated circuit and modeled it by adjusting the parameters of the traditional bipolar diode model represented by the following equation:

$$I(V) = \frac{V}{\boldsymbol{R}_{\mathbf{par}}} + \boldsymbol{I}_{\mathbf{D,sat}}\left[exp\left(\frac{q(V + I\boldsymbol{R}_{\mathbf{s}})}{\boldsymbol{n}kT}\right) - 1\right] \quad (1)$$

where $I_{D,sat}$ is the saturation current determined by different parameters such as minority carrier diffusion length or doping levels. T is the tem-

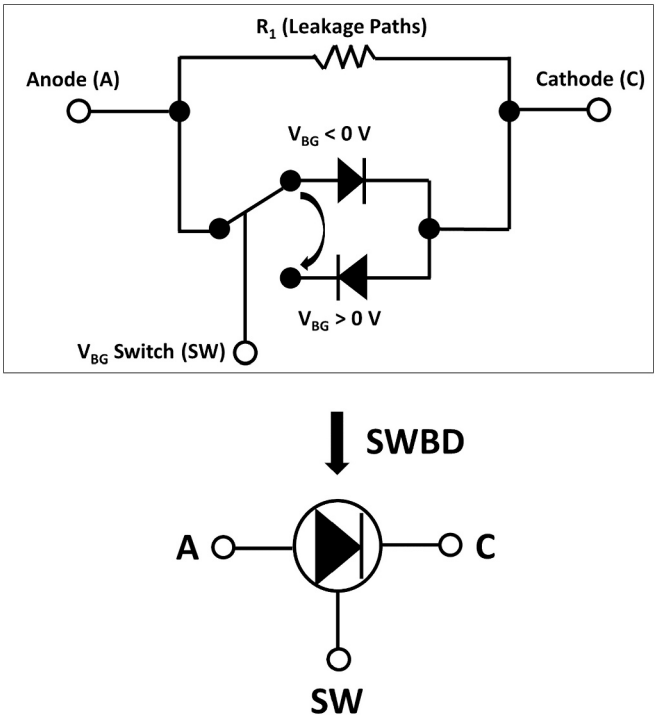

Fig. 5. SPICE equivalent circuit and symbol.

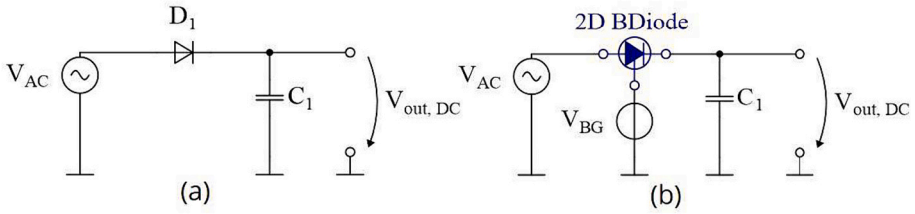

Fig. 6. a) One-way rectifier based on a conventional diode, b) Bidirectional one-way rectifier utilizing the 2D BDiode.

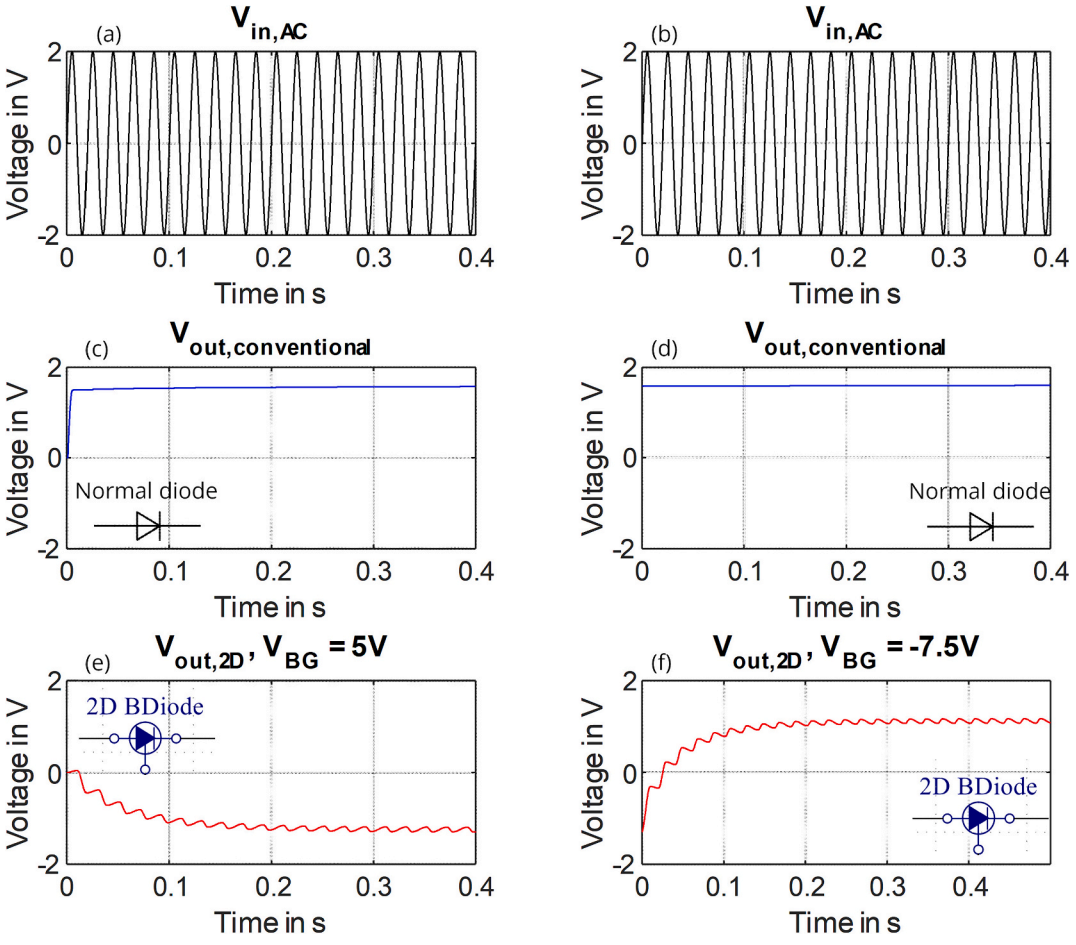

Fig. 7. Simulated transient behavior of one-way rectifier as AC/DC converter: (a-b) input AC signal for conventional and 2D BDiode rectifier, (c-d): output conventional rectifier w/o possibility of changing polarity, (e-f): 2D BDiode output with positive and negative back-gate voltage showing positive and negative output DC.

perature in Kelvin, q is the elementary charge, and k the Boltzmann constant. R_{par} and R_s represent the parasitic parallel resistance caused by leakage paths and the series resistance respectively. The series resistance contains the semiconductor drift resistance of MoS_2 and WSe_2 afar from the junction as well as the contact resistance. Here, it is simplified as an Ohmic resistance. The ideality factor n is an empirical value that is used for non-ideal diodes. It is exactly one for pure diffusion current and two for recombination current. For practical diodes, especially made with novel materials, neither pure diffusion current nor pure recombination current dominates, so the ideality factor is either between one and two, or even higher [32]. Very high values of the ideality factor, however, indicate that the observed current is probably not bipolar diode current at all. Still, the classical diode model does not cover the effect of switching the polarity observed here. Thus, we modeled the forward ($V_{BG} = -7.5$ V) and reverse ($V_{BG} = 5$ V) characteristics separately using Eq. 1. This model does not include the transition for back-gate voltages between the high positive or negative voltages of +5 V and − 7.5 V respectively. The fitting curve according to this equation is plotted along with the experimental data in Fig. 3(a-b), and it can be seen that the models are in good agreement with the measured data. The obtained model parameters for both polarities of the back-gate are summarized in Table 1.

The parallel resistance is identical for both directions since we do not expect a change in the leakage paths depending on the applied back-gate voltage. However, the series resistance is significantly high ($> 100k\Omega$), which is expected due to non-ideal contacts at the metal/2D-material interface [33,34]. Consequently, we implemented a low-complexity circuit model consisting of both diodes in an anti-parallel configuration as well as an ideal switch representing the back-gate triggering the change of the dominant current transport mechanism. This is represented by the SPICE equivalent circuit as shown in Fig. 5, along with a proposed circuit symbol which will be used in the analog circuits

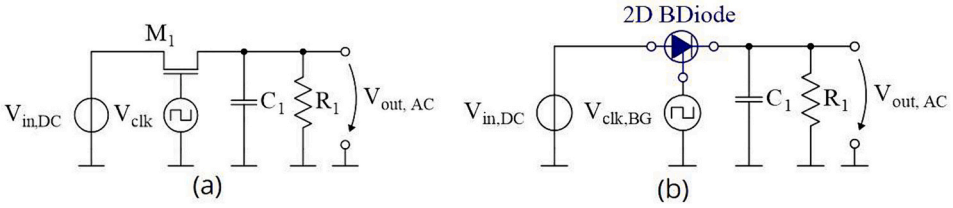

Fig. 8. Simple implementation of a DC/AC converter using (a) a conventional MOSFET and (b) the 2D BDiode for chopping the input DC voltage.

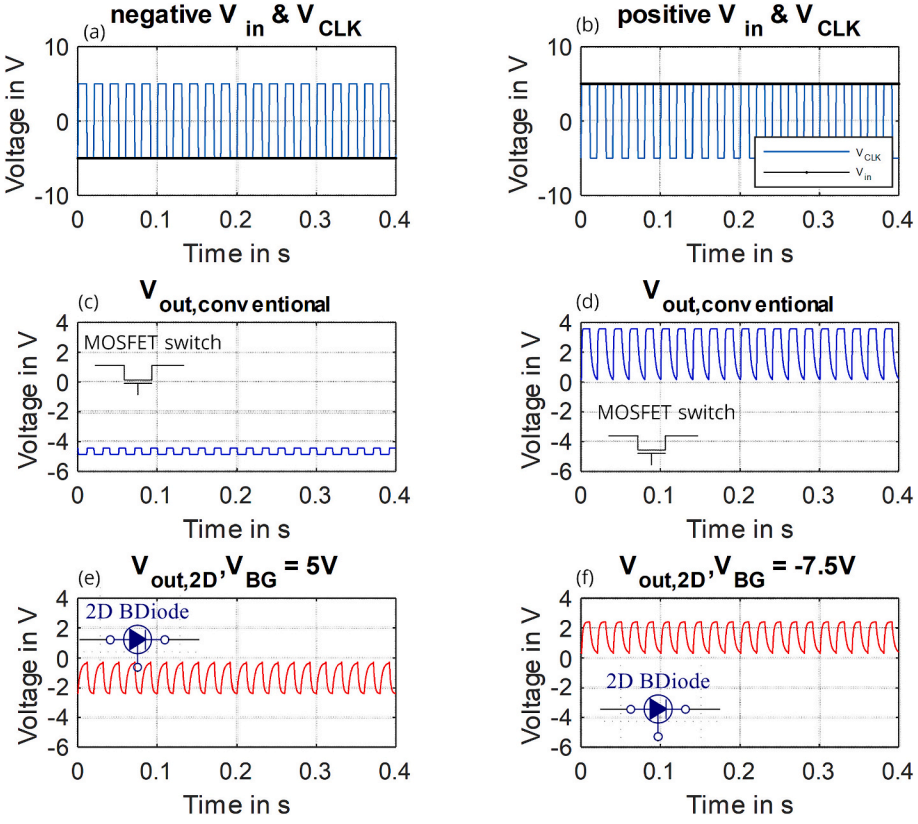

Fig. 9. Simulated V-t characteristics for the DC/AC converter. Input (a) positive and (b) negative DC signal and 50 Hz clock, output for a simple DC/AC converter using just one MOSFET and positive (c) and negative (d) DC input, and AC output for 2D BDiode-based DC/AC converter and positive (e) or negative (f) inputs.

presented in the following section. Still, a comprehensive compact model should be developed for future deeper studies and advanced applications in analog circuit design.

4. Analog circuit applications

In the following subsections, three possible applications are exemplary introduced, for which such devices, we call 2D BDiode, lead to new opportunities in analog circuit design. These results are achieved by transient simulations using LTSpice.

4.1. AC/DC conversion

As a first application, the 2D BDiode can be used for AC/DC conversion. The probably simplest way to implement an AC/DC converter is the one-way rectifier utilizing one diode and one capacitor as shown in Fig. 6(a).

In this case, the upper half-wave of a sine signal (Fig. 7(a) and (b)) passes through the diode and the capacitor flattens the signal to get a DC signal while the lower half-wave is suppressed (Fig. 7(c) and (d). Replacing the diode with our device offers the opportunity to change its polarity by tuning the back-gate voltage as can be seen in Fig. 6(b). Hence, one can decide whether the upper or the lower half-wave is rectified giving the possibility to have either a positive or a negative DC voltage at the output (Fig. 7(e) and (f)). Still, just one diode is necessary, but the flexibility of this circuit is massively increased. An exemplary simulation for both cases and a sine signal with an amplitude of 2 V and a frequency of 100 Hz is shown in Fig. 7. The value of the flattening capacitor C_1 was set to 100 nF in both cases. Note that the remaining ripple in the V-t characteristics of our device is probably not accurate, since we did not properly model the dynamics yet.

4.2. DC/AC conversion

As a second example, we can also use the 2D BDiode for the other way round, i.e., DC/AC conversion. There are many advanced circuits to convert a DC signal to an AC signal. In this paper, we focus again on one of the simplest solutions. This can be done for instance by chopping the input DC signal with a metal oxide semiconductor field-effect transistor (MOSFET) switch and shaping the signal with an RC network as shown in Fig. 8(a). In this case, for a switch implemented by one MOSFET only, a negative DC voltage cannot be converted into an AC signal. This

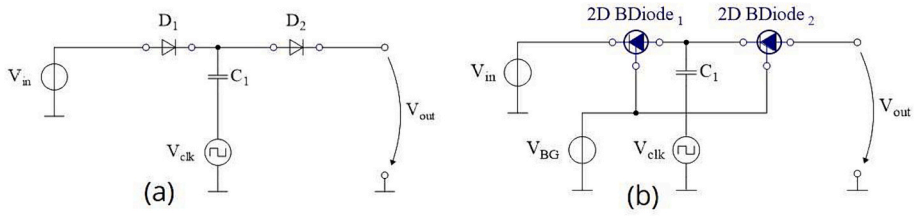

Fig. 10. Circuit of one straightforward implementation of a classical charge pump using (a) two conventional diodes and (b) the 2D BDiode.

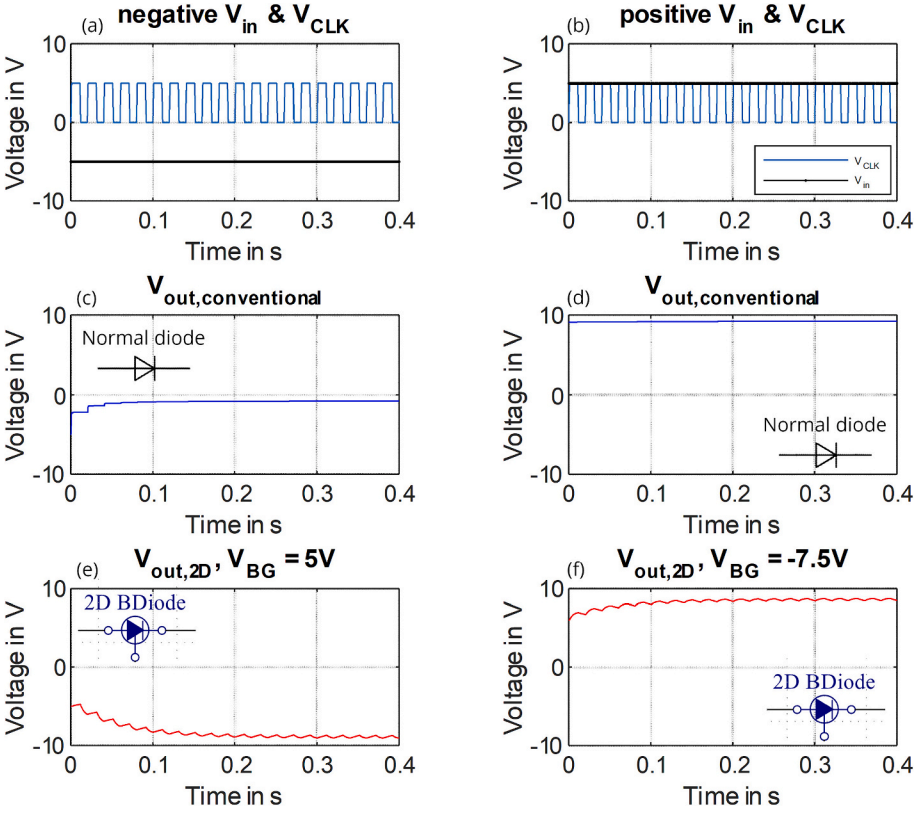

Fig. 11. Simulated V-t characteristics for the charge pump circuit. Input (a) positive and (b) negative DC signal and 200 Hz clock, output for circuit with conventional diodes and positive (c) and negative (d) DC input respectively; (e) output for 2D BDiode-based charge pump and positive or (f) negative inputs.

changes when replacing the MOSFET with the 2D BDiode as sketched in Fig. 8(b). As discussed above, it becomes more conductive, i.e., exponential increase in I-V characteristics in one direction while it suppresses the current efficiently in the other direction depending on the voltage applied to the back-gate. Hence, a clock signal switching between positive and negative voltages will trigger the device to switch its direction periodically. This can be used to chop positive DC voltages, fed through during the back-gate voltage is <0 V and blocked while back-gate voltage is >0 V respectively, and vice versa for negative DC voltages. The results of our simulations are shown in Fig. 9. For the conventional circuit, we used the standard NMOS devices of LTSpice and an input DC voltage of ±5 V (Fig. 9(a-b)). For the passives (R_1 and C_1) we used 180 $k\Omega$ and 17 nF respectively. The clock frequency is 50 Hz in each case. One can see that the approach using the conventional NMOS device (Fig. 9(c-d)) does not support negative DC voltages, i.e., the output signal amplitude is very low in this case. On the other hand, the 2D BDiode is able to chop positive and negative DC voltages (Fig. 9(e-f)). In these simulations, the amplitude of the output signal for positive DC voltages and the conventional device is a little higher than this for the 2D BDiode which is probably caused by the parasitics of our device.

4.3. Charge pump

As a last example, we introduce a bidirectional charge pump based on the 2D BDiode. The charge pump is a well-known circuit used for increasing the level of a DC voltage to a well-defined higher level. This is done by storing charges in a capacitor and periodically discharging the capacitor adding the stored charges to the input DC voltage. An example of a simple implementation of a conventional charge pump is shown in Fig. 10 utilizing two diodes.

The use of 2D BDiodes (Fig. 10) offers the benefit that positive as well as negative input DC voltages can be pumped to the respective higher level which is not possible with this simple topology, and the use of conventional diodes. The results of the transient simulations of this application are shown in Fig. 11. In this example, the input voltage is ±5 V and the targeted output the double of the input voltage, the used capacitor is 80 nF, and the clock frequency is 200 Hz (Fig. 11a-b)). The conventional straightforward circuit shown for comparison can achieve this only for positive input voltages (Fig. 11c-d)) while using the 2D BDiode can also shift negative voltages to higher levels (Fig. 11e-f)).

5. Conclusions and outlook

In summary, a fully-2D device was investigated and modeled for SPICE simulations. The simulations predict outstanding properties offering completely novel opportunities in analog circuit design. The background of this feature is the difference in the carrier transport mechanism depending on the back-gate voltage. The shown examples are very simple circuits for AC/DC conversion, DC/AC conversion, and level shifting of DC voltages (charge pump). There are several possible additional applications, also for high-frequency circuits, e.g., mixers or more complex circuits like amplifiers. However, for such applications a more detailed modeling of the device is mandatory. This includes the dynamic performance and details regarding the transition region between negative and positive back-gate bias. One major issue of such devices is reproducibility, which is affected by device-to-device variations that are inherent to the presented fabrication process. For a large scale and wide range of applications, this needs to be addressed and is a general challenge for 2D-material based devices, where high-quality wafer-scale material growth using different techniques like chemical vapor deposition and epitaxy are still in their infancy. Currently, the physical properties of the deposited materials are not yet satisfactory in comparison to their exfoliated counterparts for advanced device concepts and applications. A more advanced 2D material technology may also lead to new opportunities as the fabrication of top and bottom gates with symmetrical alignments and identical layer stacks. This would also enable reconfigurability from both sides. Nevertheless, in this paper, we demonstrated for the first time a switchable diode as a device entirely made of 2D materials including a simple SPICE model with outstanding properties for next-level analog circuit design and we named it “2D BDiode”.

Data availabiltiy

Data will be made available on request.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

Financial support by the European Social Fund and the Free State of Saxony in the project *Re*-Learning (project number 100382146 and by the Deutsche Forschungsgemeinschaft (DFG) FFlexCom Initiative (project number 270774198) as well as IHRS NANONET (project number VH-KO-606) is gratefully acknowledged. K.W. and T.T. acknowledge support from the JSPS KAKENHI (Grant Numbers 21H05233 and 23H02052) and World Premier International Research Center Initiative (WPI), MEXT, Japan.

Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mne.2024.100246.

References

[1] K. Novoselov, O.A. Mishchenko, O.A. Carvalho, A. Castro Neto, 2D materials and van der Waals heterostructures, Science 353 (6298) (2016) aac9439.
[2] P.V. Pham, S.C. Bodepudi, K. Shehzad, Y. Liu, Y. Xu, B. Yu, X. Duan, 2D heterostructures for ubiquitous electronics and optoelectronics: principles, opportunities, and challenges, Chem. Rev. 122 (6) (2022) 6514–6613.
[3] P. Chava, K. Watanabe, T. Taniguchi, T. Mikolajick, M. Helm, A. Erbe, Tunneling transport in WSe2-MoS2 heterojunction transistor enabled by a two-dimensional device architecture, in: 2022 Device Research Conference (DRC), IEEE, 2022, pp. 1–2.
[4] C.D. Matthus, P. Chava, K. Watanabe, T. Taniguchi, T. Mikolajick, M. Helm, A. Erbe, I-V-T characteristics and temperature sensor performance of a fully-2D WSe2/MoS2 heterojunction diode at cryogenic temperatures, IEEE J. Electron Dev. Soc. 11 (2023) 359–366.
[5] S. Conti, L. Pimpolari, G. Calabrese, R. Worsley, S. Majee, D.K. Polyushkin, M. Paur, S. Pace, D.H. Keum, F. Fabbri, et al., Low-voltage 2D materials-based printed field-effect transistors for integrated digital and analog electronics on paper, Nat. Commun. 11 (1) (2020) 3566.
[6] S. Wachter, D.K. Polyushkin, O. Bethge, T. Mueller, A microprocessor based on a two-dimensional semiconductor, Nat. Commun. 8 (1) (2017) 14948.
[7] Q. Gao, Z. Zhang, X. Xu, J. Song, X. Li, Y. Wu, Scalable high performance radio frequency electronics based on large domain bilayer MoS2, Nat. Commun. 9 (1) (2018) 4778.
[8] S. Zeng, Z. Tang, C. Liu, P. Zhou, Electronics based on two-dimensional materials: status and outlook, Nano Res. 14 (2021) 1752–1767.
[9] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, L. Colombo, Electronics based on two-dimensional materials, Nat. Nanotechnol. 9 (10) (2014) 768–779.
[10] R. Worsley, L. Pimpolari, D. McManus, N. Ge, R. Ionescu, J.A. Wittkopf, A. Alieva, G. Basso, M. Macucci, G. Iannaccone, et al., All-2d material inkjet-printed capacitors: toward fully printed integrated circuits, ACS Nano 13 (1) (2018) 54–60.
[11] W. Fei, J. Trommer, M.C. Lemme, T. Mikolajick, A. Heinzig, Emerging reconfigurable electronic devices based on two-dimensional materials: a review, InfoMat 4 (10) (2022) e12355.
[12] Q. Tao, R. Wu, Q. Li, L. Kong, Y. Chen, J. Jiang, Z. Lu, B. Li, W. Li, Z. Li, et al., Reconfigurable electronics by disassembling and reassembling van der waals heterostructures, Nat. Commun. 12 (1) (2021) 1825.
[13] M. Huang, S. Li, Z. Zhang, X. Xiong, X. Li, Y. Wu, Multifunctional high-performance van der waals heterostructures, Nat. Nanotechnol. 12 (12) (2017) 1148–1154.
[14] A. Avsar, K. Marinov, E.G. Marin, G. Iannaccone, K. Watanabe, T. Taniguchi, G. Fiori, A. Kis, Reconfigurable diodes based on vertical wse2 transistors with van der waals bonded contacts, Adv. Mater. 30 (18) (2018) 1707200.
[15] D.K. Polyushkin, S. Wachter, L. Mennel, M. Paur, M. Paliy, G. Iannaccone, G. Fiori, D. Neumaier, B. Canto, T. Mueller, Analogue two-dimensional semiconductor electronics, Nat. Electro. 3 (8) (2020) 486–491.
[16] S.V. Suryavanshi, E. Pop, S2ds: physics-based compact model for circuit simulation of two-dimensional semiconductor devices including non-idealities, J. Appl. Phys. 120 (22) (2016).
[17] S.-J. Han, A.V. Garcia, S. Oida, K.A. Jenkins, W. Haensch, Graphene radio frequency receiver integrated circuit, Nat. Commun. 5 (1) (2014) 3086.
[18] S.A. Ahsan, S.K. Singh, C. Yadav, E.G. Marin, A. Kloes, M. Schwarz, A comprehensive physics-based current–voltage spice compact model for 2-d-material-based top-contact bottom-gated schottky-barrier fets, IEEE Transact. Electron Dev. 67 (11) (2020) 5188–5195.
[19] S. Ma, Y. Wang, X. Chen, T. Wu, X. Wang, H. Tang, Y. Yao, H. Yu, Y. Sheng, J. Ma, et al., Analog integrated circuits based on wafer-level two-dimensional Mos 2 materials with physical and spice model, IEEE Access 8 (2020) 197287–197299.
[20] S.A. Ahsan, S.K. Singh, M.A. Mir, M. Perucchini, D.K. Polyushkin, T. Mueller, G. Fiori, E.G. Marin, A spice compact model for ambipolar 2-d-material fets aiming at circuit design, IEEE Trans. Electron Dev. 68 (6) (2021) 3096–3103.
[21] A. Castellanos-Gomez, M. Buscema, R. Molenaar, V. Singh, L. Janssen, H.S. Van Der Zant, G.A. Steele, Deterministic transfer of two-dimensional materials by all-dry viscoelastic stamping, 2D, Materials 1 (1) (2014) 011002.
[22] H. Li, Q. Zhang, C.C.R. Yap, B.K. Tay, T.H.T. Edwin, A. Olivier, D. Baillargeat, From bulk to monolayer mos2: evolution of raman scattering, Adv. Funct. Mater. 22 (7) (2012) 1385–1390.
[23] P. Tonndorf, R. Schmidt, P. Böttger, X. Zhang, J. Börner, A. Liebig, M. Albrecht, C. Kloc, O. Gordan, D.R. Zahn, et al., Photoluminescence emission and raman response of monolayer Mos 2, mose 2, and wse 2, Opt. Express 21 (4) (2013) 4908–4916.
[24] S. Buhr, C.D. Matthus, M.M. Khafaji, F. Ellinger, A 1.38-mW 7-bit 1.7-GS/s Single-Channel loop-unrolled SAR ADC in 22-nm FD-SOI with 8.85 fJ/conv.-step for GHz Mobile communication and radar systems, IEEE Transact. Microwave Theory. and Techn. 71 (9) (2023) 3841–3851.
[25] S.M. Sze, Y. Li, K.K. Ng, Physics of Semiconductor Devices, John wiley & sons, 2021.
[26] T. Roy, M. Tosun, X. Cao, H. Fang, D.-H. Lien, P. Zhao, Y.-Z. Chen, Y.-L. Chueh, J. Guo, A. Javey, Dual-gated MoS2/WSe2 van der Waals tunnel diodes and transistors, ACS Nano 9 (2) (2015) 2071–2079.
[27] A. Nourbakhsh, A. Zubair, M.S. Dresselhaus, T. Palacios, Transport properties of a MoS2/WSe2 heterojunction transistor and its potential for application, Nano Lett. 16 (2) (2016) 1359–1366.
[28] I. Lee, S. Rathi, D. Lim, L. Li, J. Park, Y. Lee, K.S. Yi, K.P. Dhakal, J. Kim, C. Lee, et al., Gate-tunable hole and electron carrier transport in atomically thin dual-channel WSe2/MoS2 heterostructure for ambipolar field-effect transistors, Adv. Mater. 28 (43) (2016) 9519–9525.
[29] C. Li, X. Yan, X. Song, W. Bao, S. Ding, D.W. Zhang, P. Zhou, WSe2/MoS2 and MoTe2/SnSe2 van der Waals heterostructure transistors with different band alignment, Nanotechnology 28 (41) (2017) 415201.

[30] M. Yang, Y. Lu, Q. Zhang, Z. Han, Y. Zhang, M. Liu, N. Zhang, H. Hu, L. Wang, Charge transport behaviors in a multi-gated WSe2/MoS2 heterojunction, Appl. Phys. Lett. 121 (4) (2022) 043501.
[31] P. Chava, Z. Fekri, Y. Vekariya, T. Mikolajick, A. Erbe, Band-to-band tunneling switches based on two-dimensional van der waals heterojunctions, Appl. Phys. Rev. 10 (1) (2023).
[32] C.D. Matthus, T. Erlbacher, A. Hess, A.J. Bauer, L. Frey, Advanced 4H-SiC p-i-n diode as highly sensitive high-temperature sensor up to 460 °C, IEEE Transact. Electron Dev. 64 (8) (2017) 3399–3404.
[33] P. Zhang, Y. Zhang, Y. Wei, H. Jiang, X. Wang, Y. Gong, Contact engineering for two-dimensional semiconductors, J. Semicond. 41 (7) (2020) 071901.
[34] S. Batool, M. Idrees, S.-T. Han, V.A. Roy, Y. Zhou, Electrical contacts with 2D materials: current developments and future prospects, Small 19 (12) (2023) 2206550.