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A three-step surface treatment and its impacts on electrical properties of *c*- and *m*-face GaN/Al_2O_3 MOS structures

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ABSTRACT

In this study, a three-step surface treatment, composed of SiO_2 deposition, subsequent annealing, and SiO_2 removal, is adopted for the fabrication of *c*- and *m*-plane n-type GaN/Al_2O_3 MOS structures, and the impact of the proposed process on electrical properties and its crystal face dependence are systematically investigated. While no significant changes are observed after the proposed surface treatment for *m*-face GaN, an identical process causes changes in the properties of *c*-face GaN MOS structures: an about 0.2 V lower flat-band voltage (V_{FB}) and an about 0.2 eV higher conduction band offset, associated with a change in the thickness or crystalline quality of a gallium oxide (GaO_x) layer on the *c*-face GaN surface. The modified energy band alignment leads to a reduced gate leakage current, reducing the V_{FB} drift after high-field positive bias stress (4.5 MV/cm) almost by half only for *c*-face GaN MOS structures. The fact that even an identical process has a crystal face-dependent impact on the properties of GaN MOS structures is important in developing the fabrication process of GaN planar and trench MOSFETs.

1. Introduction

Gallium nitride (GaN) is an attractive wide-bandgap semiconductor material that can improve the trade-off relationship between on-state resistance and blocking voltage in power devices [1–4], mainly thanks to its high critical electric field (2.5–3.5 MV/cm) [5–7]. Following the intensive research and development of GaN-based heterostructure field-effect transistors (HFETs) for high-frequency devices [8,9], GaN vertical metal–oxide–semiconductor FETs (MOSFETs) have become a promising alternative to silicon (Si) insulated gate bipolar transistors (IGBTs) and silicon carbide (SiC) MOSFETs as high-voltage switching devices [10,11]. There are two major structures of power MOSFETs, which are planar and trench structures with a MOS channel formed on *c*- and *m*-plane GaN, respectively. Thus, the formation of a high-quality GaN/dielectric interface on *c*- and *m*-faces is key to improving the performance and reliability of GaN MOSFETs.

In the fabrication of GaN MOS structures, aluminum-based gate insulators, such as aluminum oxide (Al_2O_3) [12–16], aluminum silicate (AlSiO) [17,18], aluminum oxynitride (AlON) [19,20], and so forth, have been widely adopted. A low interface state density ($D_{it} \sim 10^{11}$ $cm^{-2}eV^{-1}$) near the conduction band edge (E_C) has been reported using n-type GaN MOS structures [21–23]. Reflecting a low D_{it} near E_C, besides, a very high channel mobility exceeding 100 $cm^2V^{-1}s^{-1}$ has been demonstrated [24,25], making the GaN MOS structures with an aluminum-based gate dielectric promising for high-performance power MOSFETs.

On the other hand, the long-term reliability of the MOS structure is still a concern. Few reports have performed stress tests and investigated charge-trapping behavior for aluminum-based gate insulators [26–28]. For example, it was indicated for a GaN/AlSiO system that the flat-band voltage (V_{FB}) drift after applying positive-bias stress (PBS) reaches over 1.5 V in 300 s unless the temperature of post-deposition annealing (PDA) is optimized. Hence, it is crucial to establish a formation process of GaN MOS structures that does not cause any degradation of electrical properties during device operation.

To improve the reliability of GaN MOS structures, we have focused on surface treatment before the gate dielectric formation. According to previous studies, the D_{it} value of *c*- and *m*-face at GaN/Al_2O_3 MOS interfaces is effectively reduced by post-metallization annealing (PMA) even at a low temperature (300 °C) [21,23], indicating that the surface of GaN and/or the native oxide layer [29,30] is inherently unstable. In this sense, we recently proposed a three-step surface treatment, named the dummy SiO_2 process [31]. In this method, (1) deposition of silicon

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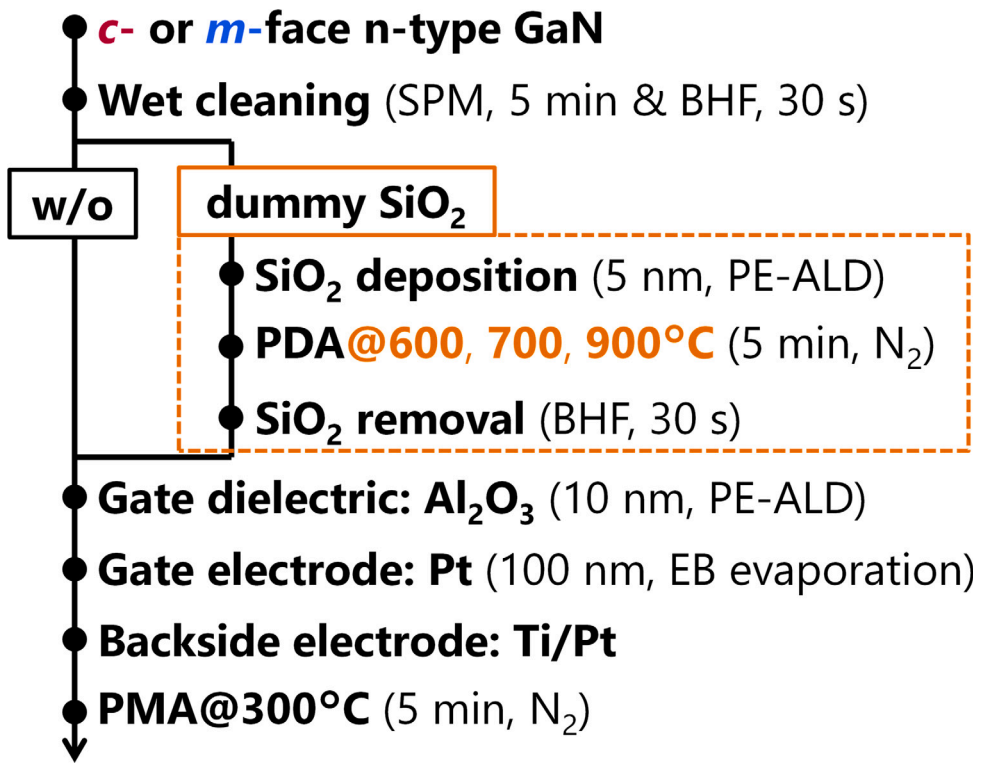

Fig. 1. Flow for fabricating *c*- and *m*-face GaN/Al_2O_3 MOS capacitors with and without the dummy SiO_2 process.

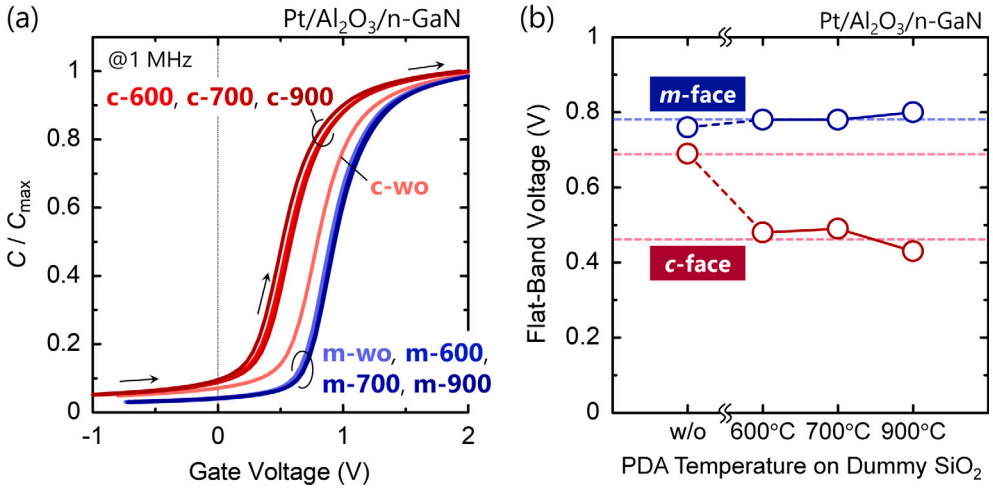

Fig. 2. (a) Typical *C*–*V* characteristics and (b) flat-band voltage of *c*- and *m*-face GaN/Al_2O_3 MOS structures. The dummy SiO_2 process caused a negative shift of *C*–*V* curves and flat-band voltage only for the *c*-face samples.

dioxide (SiO_2) film, (2) subsequent PDA in nitrogen (N_2) ambient, and (3) SiO_2 removal with buffered hydrofluoric acid (BHF) are performed prior to the gate dielectric formation. Our previous work adopted this process for the fabrication of *c*-face GaN/Al_2O_3 MOS structures with the PDA temperature of 800 °C and investigated the V_{FB} stability against PBS [31]. As a result, the proposed process effectively suppressed the V_{FB} drift during PBS even under a relatively high oxide field of 4 MV/cm. On the other hand, it is still unclear what role the dummy SiO_2 process plays in improving the V_{FB} stability. To elucidate the critical factor contributing to the improved reliability of MOS structures and further develop the proposed process, more detailed investigations of the MOS interface properties are necessary by varying the process condition, such as the temperature of PDA on dummy SiO_2. Besides, it is beneficial to clarify the impact of this process on *m*-face GaN MOS structures, aiming at high-performance and highly reliable GaN trench MOSFETs. In the present study, we fabricated *c*- and *m*-face GaN/Al_2O_3 MOS capacitors with various PDA temperatures on dummy SiO_2 and systematically investigated the electrical properties and the surface chemical bonding, discussing their dependency on the crystal face of GaN.

2. Experiment

Fig. 1 shows the fabrication process of the GaN/Al_2O_3 MOS structures. The *c*-face GaN MOS capacitors were prepared with n-type GaN epitaxial layers (donor density: ~ 2×10^{16} cm^{-3}) grown on n-type GaN(0001) freestanding substrates, while n-GaN epitaxial layers (donor density: 7–8 $\times$ 10^{15} cm^{-3}) on GaN(10$\bar{1}$0) substrates were used

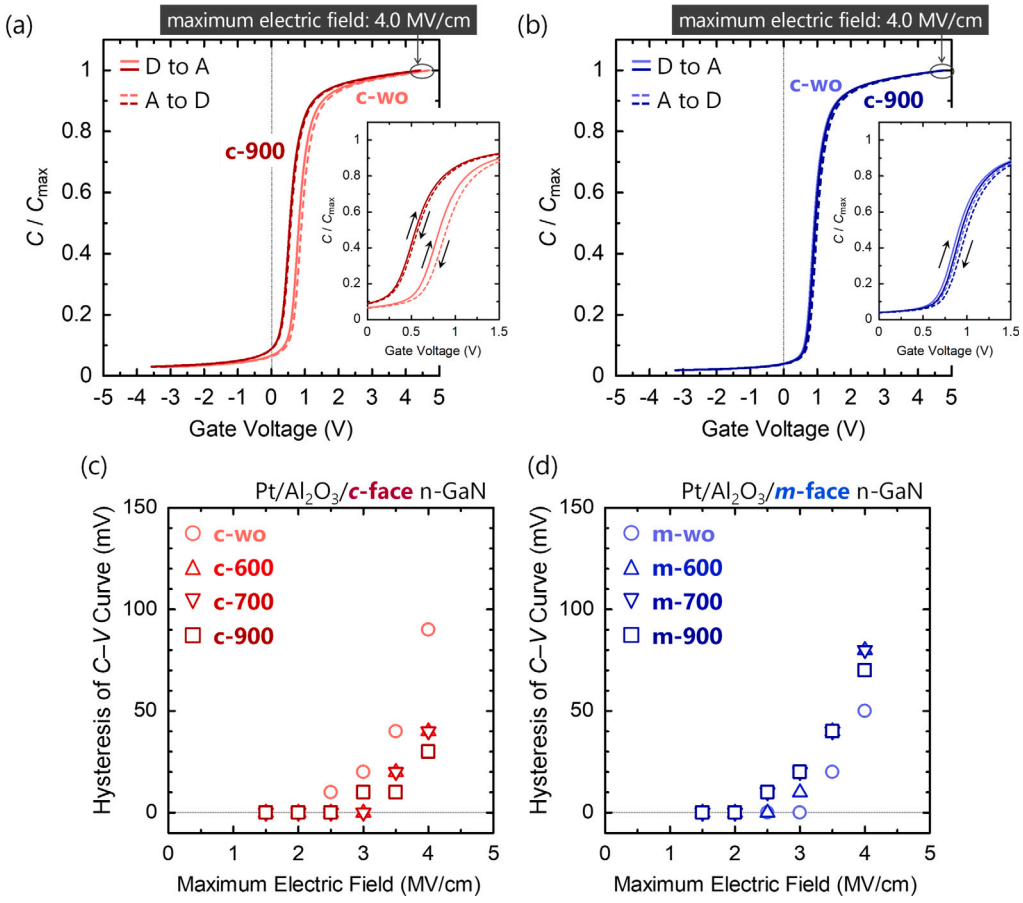

Fig. 3. Bidirectional C–V characteristics of (a) c- and (b) m-face GaN/Al_2O_3 MOS structures. Hysteresis of C–V curve determined using V_{FB} as a function of the maximum electric field in (c) c- and (d) m-face GaN/Al_2O_3 MOS structures. The dummy SiO_2 process reduced the hysteresis under a high electric field only for the c-face samples.

as m-plane samples. The substrates were first cleaned with sulfuric peroxide mixture (SPM) for 5 min and BHF for 30 s. For the dummy SiO_2 process, a 5 nm-thick SiO_2 was deposited on some samples by plasma-enhanced atomic layer deposition (PE-ALD) at the substrate temperature of 300 °C with tris(dimethylamino)silane as a precursor. PDA was then performed at various temperatures (600–900 °C) in N_2 ambient for 5 min, followed by the SiO_2 removal with BHF solution (30 s). Note that the etching rate of β-gallium oxide with BHF was very low (1.4–2.2 nm/h), barely etching a gallium oxide layer that would be formed on the GaN surface [31]. Gate dielectric was formed by depositing a 10 nm-thick Al_2O_3 film by PE-ALD at 300 °C with a precursor and oxidant gas of trimethylaluminum and H_2O, respectively. A circular-shaped gate electrode with a diameter of about 100 μm was formed on Al_2O_3 by electron-beam evaporation of Pt, and then, Ti/Pt electrode stack was deposited on the substrate as backside ohmic contacts. Finally, PMA was conducted at 300 °C in N_2 ambient for 5 min. Hereafter, the samples treated with the dummy SiO_2 process are labeled with the crystal face and PDA temperature (e.g., c-900 and m-900), while non-treated ones are indicated as c-wo and m-wo for the c- and m-plane samples, respectively.

Capacitance–voltage (C–V) characteristics of the MOS capacitors were acquired at room temperature with the probe frequency of 1 MHz by sweeping the voltage from depletion to accumulation (D to A), and then back to depletion (A to D). Current–voltage (I–V) measurements were performed as well. Besides, PBS tests were conducted at room temperature for 300 s in total by systematically varying the stress field from 2.0 to 4.5 MV/cm. After the stress time (t) of 1, 10, 50, 100, 150, 200, 250, and 300 s, C–V characteristics were repeatedly measured, and the V_{FB} drift caused by PBS was characterized. The direction of voltage

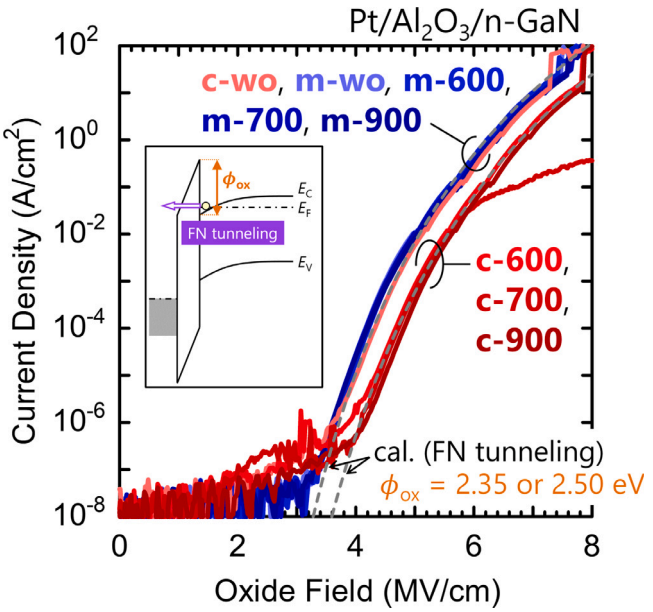

Fig. 4. Current density–oxide field characteristics of c- and m-face GaN/Al_2O_3 MOS structures. The dummy SiO_2 process made the conduction band offset (ϕ_{ox}) about 0.2 eV higher only for c-face GaN.

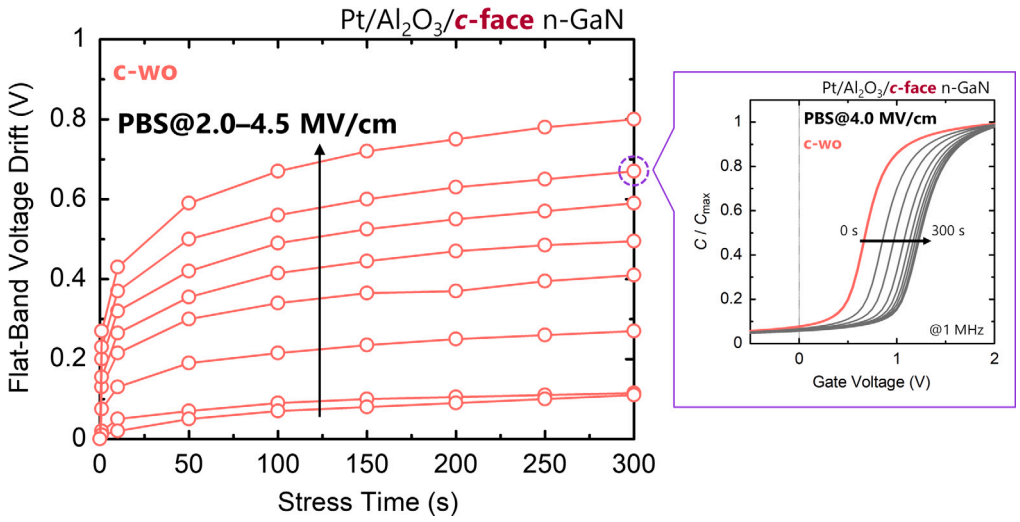

Fig. 5. Flat-band voltage drift versus stress time under various electric field conditions in *c*-face GaN/Al_2O_3 MOS structures fabricated without surface treatment (c-wo). The inset shows an example of the *C*–*V* curve drift under a stress field of 4.0 MV/cm.

sweeping for *C*–*V* measurements after PBS was from accumulation to depletion to avoid electron emission from a trap. Additionally, X-ray photoelectron spectroscopy (XPS) measurements with monochromated Al Kα X-ray ($h\nu$ = 1486.6 eV) were performed on the GaN surface before and after the surface treatment, and Ga 3*d* spectra were compared between different crystal faces. Note that the PDA temperature in the sample preparation for XPS measurement was 800 °C, which is the same PDA condition as the literature [31].

3. Results

Fig. 2 shows (a) the typical *C*–*V* characteristics of the GaN/Al_2O_3 MOS capacitors and (b) V_{FB} versus process condition. Note that V_{FB} was determined at a voltage where the capacitance value measured at a high frequency (1 MHz) is equal to $C_{FB} = C_{ox}C_{s,FB}/(C_{ox} + C_{s,FB})$, where C_{ox} is the oxide capacitance and $C_{s,FB}$ is expressed as $\varepsilon_s\varepsilon_0/L_D$ using the dielectric constant of GaN (ε_s = 10.4ε_0 and 9.5ε_0 for *c*- and *m*-face, respectively [32]) and the Debye length (L_D) [33]. As for the *c*-face GaN MOS capacitors, *C*–*V* curves shifted toward a lower voltage side by the dummy SiO_2 process, and the V_{FB} shift was 0.2–0.3 V, as plotted in Fig. 2(b). On the other hand, no significant change in *C*–*V* characteristics and V_{FB} was observed for the *m*-face samples. Note that there was only a slight PDA temperature dependence of the *C*–*V* characteristics and V_{FB} values.

Fig. 3 shows the bidirectional *C*–*V* curves in (a) *c*- and (b) *m*-face GaN MOS capacitors, varying the maximum value of the sweeping voltage (i.e., maximum electric field). The hysteresis of *C*–*V* characteristics determined by extracting V_{FB} is plotted against the maximum electric field in Figs. 3(c) and (d). While larger hysteresis was observed with increasing the maximum field, the hysteresis was below 100 mV in all the samples. The hysteresis under a higher electric field was reduced by almost half only in the *c*-plane GaN MOS capacitors, while almost no change in the hysteresis was observed for *m*-face.

The crystal face-dependent impact of the dummy SiO_2 process was also found in *I*–*V* characteristics. Fig. 4 shows the current density through the gate dielectric (J_g) as a function of the oxide field (E_{ox}), which is defined as $E_{ox} = (V - V_{FB})/t_{ox}$, where t_{ox} is the thickness of Al_2O_3. The gate current measured under a given E_{ox} was reduced by adopting the dummy SiO_2 process only for the *c*-face samples, while was not affected by the same process for *m*-face. To determine the conduction band offset (ϕ_{ox}) at the GaN/Al_2O_3 interface, Fowler-Nordheim (FN) tunneling current was calculated based on the following analytical formula [34,35],

$$J_{FN} = \frac{e^3 E_{ox}^2}{16\pi^2\hbar\phi_{ox}} \exp\left(-\frac{4\sqrt{2m_{ox}^*}}{3e\hbar E_{ox}}\phi_{ox}^{3/2}\right), \quad (1)$$

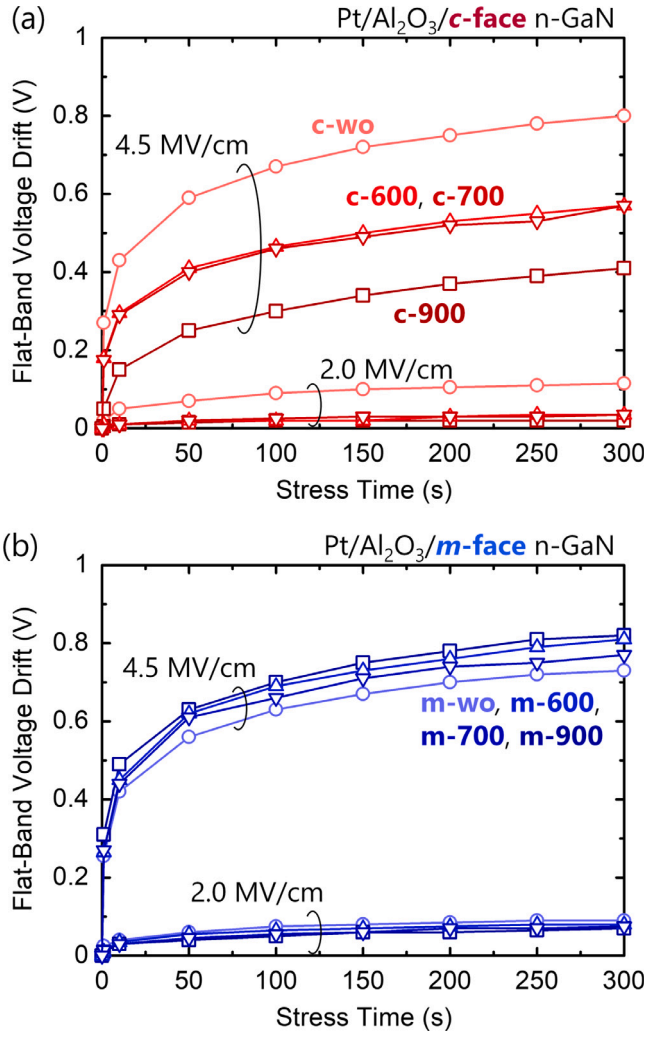

Fig. 6. Flat-band voltage drift versus stress time under the electric field of 2.0 and 4.5 MV/cm in (a) *c*- and (b) *m*-face GaN/Al_2O_3 MOS structures.

where e is the elementary charge, $\hbar$ is the Dirac constant, and m_{ox}^* is the effective mass in Al_2O_3 (0.28m_0 [36]). Note that the barrier

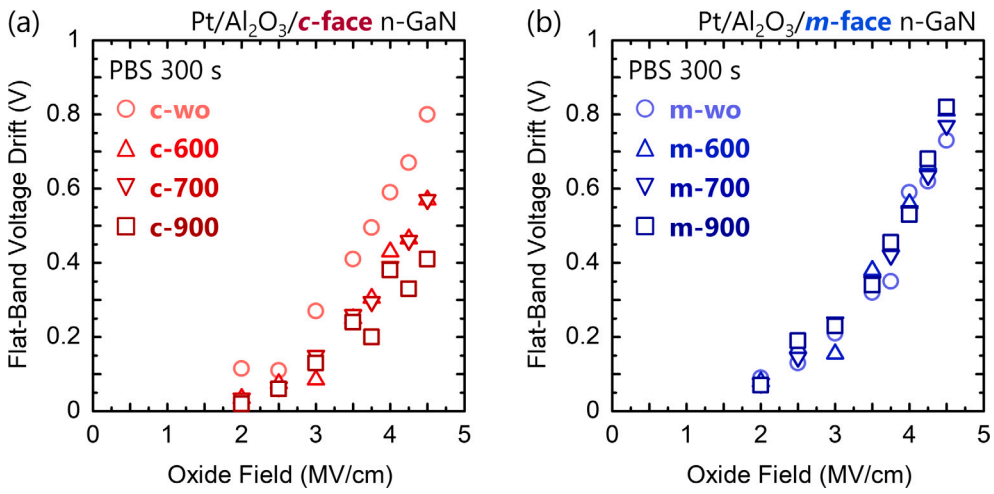

Fig. 7. Flat-band voltage drift after 300 s-stress as a function of electric field in (a) *c*- and (b) *m*-face GaN/Al_2O_3 MOS structures.

height lowering by the image force effect was considered in the calculation [34,35]. The FN tunneling current calculated by varying ϕ_{ox} is plotted by the dashed lines in Fig. 4. The experimental J_g–E_{ox} characteristics for the c-wo and all the *m*-plane samples were well reproduced with ϕ_{ox} = 2.30–2.35 eV, while an increased ϕ_{ox} of 2.50 eV was obtained for the *c*-face samples treated by the dummy SiO_2 process.

In Fig. 5, the V_{FB} drift caused by PBS with various electric fields is plotted against the stress time for the c-wo sample. *C*–*V* curves acquired after each stress time with the electric field of 4.0 MV/cm are shown as an example in the inset of Fig. 5. As seen in Fig. 5, a higher stress field led to a larger drift of the *C*–*V* curves, and the V_{FB} drift by 300 s-stress with 4.5 MV/cm was as large as 0.8 V for the c-wo sample.

Then, we compared the V_{FB} drift by 2.0 or 4.5 MV/cm-stress in the *c*- and *m*-face GaN MOS capacitors, as plotted in Fig. 6(a) and (b), respectively. Fig. 7 summarizes the stress field dependence of the V_{FB} values in the (a) *c*- and (b) *m*-face samples. As for *c*-face, the V_{FB} drift by high-field stress was effectively reduced by the dummy SiO_2 process and was 0.4 V in the c-900 sample, which was about a half of that in the c-wo sample. In contrast to the improved V_{FB} stability by the proposed process for the *c*-face GaN MOS capacitors, almost no changes in the V_{FB} drift were found in the *m*-face sample.

Fig. 8 shows the Ga 3*d* core-line spectra of the (a) *c*- and (b) *m*-face GaN surfaces treated by the dummy SiO_2 process. A fitting analysis with two peaks of Ga-N and Ga-O bonding was performed, and the peak intensity ratio of the two bonding components was characterized, as plotted in Fig. 8(c). Note that the binding energy of Ga-N bonding was 19.6 eV, and the peak value of Ga-O bonding in fitting analysis was given by the energy of 20.4 eV. For *c*-face GaN, the peak intensity ratio of the surface treated by the dummy SiO_2 process was about 1.3 times higher than that of the as BHF-cleaned surface with a native oxide layer, indicating a thicker or denser GaO_x layer on the GaN surface [31]. On the other hand, the peak intensity of Ga-O bonding for the *m*-face GaN surface was smaller than that of *c*-face after BHF treatment and was not changed much by the dummy SiO_2 process. Thus, it is presumed that an *m*-face GaN surface has a thin native oxide and is not easily oxidized compared to *c*-face GaN.

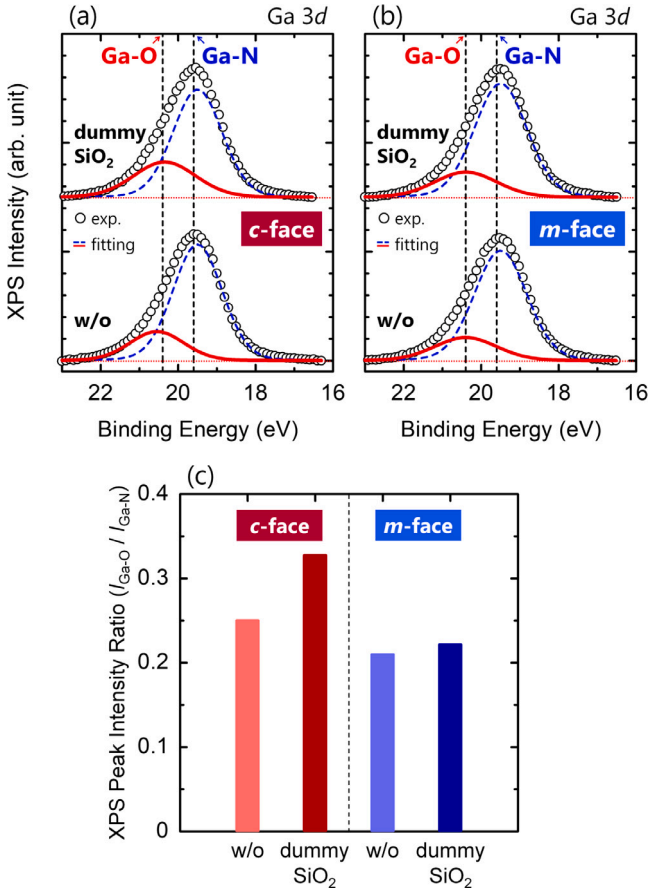

Fig. 8. Ga 3*d* spectra of (a) *c*- and (b) *m*-face GaN surfaces after BHF cleaning (labeled as w/o) and the dummy SiO_2 process. (c) XPS peak intensity of Ga-O bonding normalized by that of Ga-N bonding. A higher peak intensity ratio indicates a thicker or denser GaO_x layer on the surface.

4. Discussion

As presented above, the impact of the dummy SiO_2 process is strongly dependent on the crystal face of GaN. Regarding electrical properties, an about 0.2 V smaller V_{FB} and an about 0.2 eV higher ϕ_{ox} were found only for the *c*-face GaN/Al_2O_3 MOS structures treated with the dummy SiO_2 process. Besides, XPS measurements indicated an increase in the thickness or an improved crystalline quality of a surface GaO_x layer by the proposed process only for *c*-face GaN. Based on these results, changes in the electrical properties of the *c*-face GaN/Al_2O_3 MOS structures can be correlated with the structural change of a GaO_x layer, that is, a change in the GaO_x layer results in a modified surface energy band structure where the conduction band edge near the GaN surface becomes about 0.2 eV lower.

We considered whether the critical factor for the improved V_{FB} stability against high-field stress observed only in the *c*-face GaN MOS

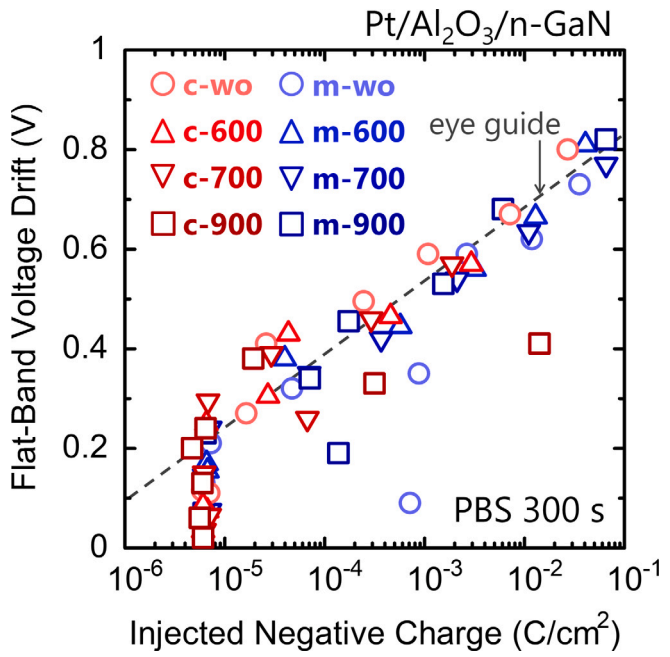

Fig. 9. Flat-band voltage drift after 300 s-stress with various electric fields as a function of the total injected charge in *c*- and *m*-face GaN/Al_2O_3 MOS structures. The total injected charge was determined by taking the integral of the current density–stress time characteristics during stress. A higher stress field leads to a larger FN tunneling current and thereby a larger injected charge.

structures is not the reduction of oxide traps but the change in the energy band alignment and a reduced FN tunneling current. Thus, we calculated the total injected negative charge by taking the integral of the J_g–t characteristics during PBS. Fig. 9 shows the relationship between the V_{FB} drift and the total injected charge after 300 s-stress with various electric fields. Note that the minimum value of the injected charge is about 5×10^{-6} C/cm^2 due to the detection limit of the I–V measurement. As seen in Fig. 9, the V_{FB} drift was almost uniquely dependent on the total injected charge, regardless of the crystal face, electric field, and process condition. Therefore, it turned out that the critical role of the dummy SiO_2 process is the rearrangement of the energy band alignment of the *c*-face GaN surface associated with a structural change in the GaO_x layer, improving the V_{FB} stability in GaN MOS structures. On the other hand, the impact of PDA is not fully understood yet because the V_{FB} drift after PBS was further reduced at a higher PDA temperature, despite PDA temperature-independent C–V and I–V characteristics among the *c*-plane samples. Hence, further investigations, including a two-step treatment without PDA and more detailed structural analyses with various PDA conditions, are required in the future.

Since a higher conduction band offset resulting from the formation of a GaO_x interlayer leads to a lower valence band offset, it will also be a subject of future study to investigate the V_{FB} stability against hole injection by negative bias stress. As for GaN MOS structures, it is reported that a large amount of hole traps exist near the valence band edge [37–40], leading to a significant shift of the threshold voltage and V_{FB} in GaN MOSFETs by applying a negative gate voltage. While the origin of hole traps is not fully understood even now, several theoretical and experimental studies reported that a GaO_x interlayer is one of the origins of high-density hole traps [41–44]. On the other hand, hole traps at a lower energy level in the gate dielectric will become accessible with the reduced valence band offset by the formation of the GaO_x interlayer, which can also affect the V_{FB} drift by hole trapping in GaN MOS structures. In this sense, it is important to adopt the proposed process for *c*- and *m*-face p-type GaN MOS capacitors (or n-channel planar and trench MOSFETs) and to investigate the hole-trapping behavior and its crystal face dependence, discussing based on the formation of a GaO_x interlayer.

5. Conclusions

In summary, using a proposed surface treatment, named the dummy SiO_2 process, the electrical properties and their crystal face dependence of n-type GaN/Al_2O_3 MOS structures were systematically investigated. While the proposed process was not effective on the properties of *m*-face GaN MOS structures, the same process made the flat-band voltage smaller by 0.2–0.3 V and the conduction band offset higher by 0.2 eV for *c*-face GaN, resulting from a modified energy band alignment associated with the structural change of a surface GaO_x layer. It was revealed that the energy band rearrangement at the GaN surface (~ 0.2 eV) and about an order of magnitude smaller FN tunneling current through the gate dielectric are the critical factors of the dummy SiO_2 process that contribute to an improved flat-band voltage stability against high-field stress (> 4 MV/cm) in *c*-face GaN/Al_2O_3 MOS structures. It was demonstrated that even an identical process can have a different impact on the properties of *c*- and *m*-face n-GaN MOS structures, which should be an important insight toward developing the fabrication process of GaN planar and trench MOSFETs.

CRediT authorship contribution statement

Masahiro Hara: Writing – original draft, Visualization, Validation, Methodology, Investigation, Formal analysis, Data curation. **Toshihide Nabatame:** Writing – review & editing, Validation, Supervision, Software, Resources, Project administration, Investigation, Funding acquisition, Data curation, Conceptualization. **Yoshihiro Irokawa:** Writing – review & editing, Validation, Investigation, Formal analysis, Data curation, Conceptualization. **Tomomi Sawada:** Validation, Investigation, Data curation. **Manami Miyamoto:** Validation, Investigation, Data curation. **Hiromi Miura:** Validation, Investigation, Data curation. **Tsunenobu Kimoto:** Writing – review & editing, Validation, Supervision, Resources, Project administration, Methodology. **Yasuo Koide:** Writing – review & editing, Validation, Supervision, Resources, Project administration, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

The data that support the findings of this study are available from the corresponding author upon a reasonable request.

References

[1] S.J. Pearton, J.C. Zolper, R.J. Shul, F. Ren, J. Appl. Phys. 86 (1) (1999) 1–78.
[2] B.J. Baliga, Semicond. Sci. Technol. 28 (7) (2013) 074011.
[3] T. Kachi, Japan. J. Appl. Phys. 53 (10) (2014) 100210.
[4] F. Roccaforte, P. Fiorenza, G. Greco, R. Lo Nigro, F. Giannazzo, F. Iucolano, M. Saggio, Microelectron. Eng. 187–188 (2018) 66–77.
[5] L. Cao, J. Wang, G. Harden, H. Ye, R. Stillwell, A.J. Hoffman, P. Fay, Appl. Phys. Lett. 112 (26) (2018) 262103.
[6] D. Ji, B. Ercan, S. Chowdhury, Appl. Phys. Lett. 115 (7) (2019) 073503.

[7] T. Maeda, T. Narita, S. Yamada, T. Kachi, T. Kimoto, M. Horita, J. Suda, J. Appl. Phys. 129 (18) (2021) 185702.
[8] M.A. Khan, A. Bhattarai, J.N. Kuznia, D.T. Olson, Appl. Phys. Lett. 63 (9) (1993) 1214–1215.
[9] F. Bernardini, V. Fiorentini, D. Vanderbilt, Phys. Rev. B. 56 (16) (1997) R10024–R10027.
[10] T. Oka, Japan. J. Appl. Phys. 58 (SB) (2019) SB0805.
[11] T. Kimoto, H. Watanabe, Appl. Phys. Express 13 (12) (2020) 120101.
[12] Y.C. Chang, W.H. Chang, H.C. Chiu, L.T. Tung, C.H. Lee, K.H. Shiu, M. Hong, J. Kwo, J.M. Hong, C.C. Tsai, Appl. Phys. Lett. 93 (5) (2008) 053504.
[13] T. Hossain, D. Wei, J.H. Edgar, N.Y. Garces, N. Nepal, J.K. Hite, M.A. Mastro, C.R. Eddy, Jr, H.M. Meyer, III, J. Vac. Sci. Technol. B 33 (6) (2015) 061201.
[14] X. Wu, R. Liang, L. Guo, L. Liu, L. Xiao, S. Shen, J. Xu, J. Wang, Appl. Phys. Lett. 109 (23) (2016) 232101.
[15] W. Li, H.G. Xing, K. Nomoto, K. Lee, S.M. Islam, Z. Hu, M. Zhu, X. Gao, M. Pilla, D. Jena, IEEE Trans. Electron Devices 65 (6) (2018) 2558–2564.
[16] K. Yuge, T. Nabatame, Y. Irokawa, A. Ohi, N. Ikeda, L. Sang, Y. Koide, T. Ohishi, Semicond. Sci. Technol. 34 (3) (2019) 034001.
[17] C. Gupta, S.H. Chan, A. Agarwal, N. Hatui, S. Keller, U.K. Mishra, IEEE Electron Device Lett. 38 (11) (2017) 1575–1578.
[18] M. Kanechika, T. Hirata, T. Tokozumi, T. Kachi, J. Suda, Appl. Phys. Express 17 (1) (2023) 016502.
[19] K. Watanabe, M. Nozaki, T. Yamada, S. Nakazawa, Y. Anda, M. Ishida, T. Ueda, A. Yoshigoe, T. Hosoi, T. Shimura, H. Watanabe, Appl. Phys. Lett. 111 (4) (2017) 042102.
[20] J. Song, S.-W. Han, H. Luo, J. Rumsey, J.H. Leach, R. Chu, Appl. Phys. Lett. 119 (12) (2021) 122105.
[21] T. Hashizume, S. Kaneki, T. Oyobiki, Y. Ando, S. Sasaki, K. Nishiguchi, Appl. Phys. Express 11 (12) (2018) 124102.
[22] Y. Ando, K. Nagamatsu, M. Deki, N. Taoka, A. Tanaka, S. Nitta, Y. Honda, T. Nakamura, H. Amano, Appl. Phys. Lett. 117 (10) (2020) 102102.
[23] S. Kaneki, T. Hashizume, AIP Adv. 11 (1) (2021) 015301.
[24] K. Ito, S. Iwasaki, K. Tomita, E. Kano, N. Ikarashi, K. Kataoka, D. Kikuta, T. Narita, Appl. Phys. Express 16 (7) (2023) 074002.
[25] M. Kanechika, K. Ito, T. Narita, K. Tomita, S. Iwasaki, D. Kikuta, T. Kachi, Phys. Status Solidi Rapid Res. Lett. (2024) 2400010.
[26] R. Yeluri, X. Liu, M. Guidry, O.S. Koksaldi, S. Lal, J. Kim, J. Lu, S. Keller, U.K. Mishra, Appl. Phys. Lett. 105 (22) (2014) 222905.
[27] D. Bisi, S.H. Chan, X. Liu, R. Yeluri, S. Keller, M. Meneghini, G. Meneghesso, E. Zanoni, U.K. Mishra, Appl. Phys. Lett. 108 (11) (2016) 112104.
[28] D. Kikuta, K. Ito, T. Narita, T. Kachi, Appl. Phys. Express 13 (2) (2020) 026504.
[29] Y. Irokawa, T.T. Suzuki, K. Yuge, A. Ohi, T. Nabatame, K. Kimoto, T. Ohnishi, K. Mitsuishi, Y. Koide, Japan. J. Appl. Phys. 56 (12) (2017) 128004.
[30] J.H. Dycus, K.J. Mirrielees, E.D. Grimley, R. Kirste, S. Mita, Z. Sitar, R. Collazo, D.L. Irving, J.M. LeBeau, ACS Appl. Mater. Interfaces 10 (13) (2018) 10607–10611.
[31] Y. Irokawa, T. Nabatame, T. Sawada, M. Miyamoto, H. Miura, K. Tsukagoshi, Y. Koide, ECS J. Solid State Sci. Technol. 13 (8) (2024) 085003.
[32] A.S. Barker, M. Ilegems, Phys. Rev. B 7 (2) (1973) 743.
[33] D.K. Schroder, Semiconductor Material and Device Characterization, third ed., John Wiley & Sons, Hoboken, NJ, USA, 2005.
[34] M. Lenzlinger, E.H. Snow, J. Appl. Phys. 40 (1) (1969) 278–283.
[35] S.M. Sze, Y. Li, K.K. Ng, Physics of Semiconductor Devices, fourth ed., John Wiley & Sons, 2021.
[36] O. Blank, H. Reisinger, R. Stengl, M. Gutsche, F. Wiest, V. Capodieci, J. Schulze, I. Eisele, J. Appl. Phys. 97 (4) (2005) 044107.
[37] W. Huang, T. Khan, T. Paul Chow, J. Electron. Mater. 35 (4) (2006) 726–732.
[38] K. Zhang, M. Liao, M. Imura, T. Nabatame, A. Ohi, M. Sumiya, Y. Koide, L. Sang, Appl. Phys. Express 9 (12) (2016) 121002.
[39] M. Akazawa, Y. Tamamura, T. Nukariya, K. Kubo, T. Sato, T. Narita, T. Kachi, J. Appl. Phys. 132 (19) (2022) 195302.
[40] K. Tomigahara, M. Hara, M. Nozaki, T. Kobayashi, H. Watanabe, Appl. Phys. Express 17 (8) (2024) 081002.
[41] M.D. McCluskey, J. Appl. Phys. 127 (10) (2020) 101101.
[42] S. Hattori, A. Oshiyama, K. Shiraishi, J. Appl. Phys. 135 (17) (2024) 175303.
[43] S. Hattori, A. Oshiyama, K. Shiraishi, Appl. Phys. Lett. 125 (16) (2024) 161601.
[44] M. Hara, T. Kobayashi, M. Nozaki, H. Watanabe, Appl. Phys. Lett. 126 (2) (2025) 022113.