Diamond Metal-Oxide-Semiconductor Field-effect Transistors on a Large-area Wafer

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***Abstract*—**Diamond is promising for high-power, high-frequency, and high-temperature applications. By now, most of diamond metal-oxide-semiconductor field-effect transistors (MOSFETs) are fabricated on small-area diamond wafers (3 × 3 mm^2). In order to push forward the diamond electronic devices for future practical application, it is necessary to investigate the electrical properties of them on the large-area wafers. In this study, we fabricate planar-type and T-type hydrogen-terminated diamond MOSFETs on a large-area wafer (8 × 8 mm^2). Electrical properties of them are investigated and discussed.

Keywords—Diamond, MOSFET, large-area wafer, T-type

I. Introduction

It is well-known that diamond has been studied for applications in high-temperature, high-power, and high-frequency electronic devices because of its wide band gap energy, high breakdown field, high carrier mobility, and large thermal conductivity [1].

Development of diamond-based electronic devices has been limited by the low free carrier densities at room temperature due to the high activation energies of boron (370 meV) and phosphorus (570 meV) dopants. Fortunately, *p*-type hydrogen-terminated diamond (H-diamond) channel layer can accumulate two-dimensional hole gases on the surface with sheet hole density of 10^{12}~10^{13} cm^{-2}. Notably, after exposing the H-diamond in the NO_2 ambient or annealing in the NH_3 + H_2 ambient [2, 3], its hole density can be increased to be as high as 10^{14} cm^{-2}. Therefore, the H-diamond is believed to be a promising channel layer for fabricating high-performance diamond electronic devices, such as metal-oxide-semiconductor field-effect transistors (MOSFETs).

In the previous studies [4-9], most of the H-diamond MOSFETs were fabricated on small-area diamond wafers with size of 3 × 3 mm^2. They showed excellent electrical properties with high output current, large extrinsic transconductance, and high breakdown voltage. Recently, the 3-inch single-crystalline diamond wafer has been grown in laboratory successfully [10]. Further, the 0.5-inch wafer has been commercially available. Therefore, it is assumed that the diamond-based MOSFET power devices can be used in our common lives in the near future.

In order to push forward the diamond electronic devices for practical application, it is necessary to investigate the electrical properties of them on the large-area wafer. In this study, we fabricate the planar-type and T-type diamond MOSFETs on a large-area wafer (8 × 8 mm^2). Electrical properties of them are investigated and discussed.

II. Experimental

Figure 1 shows fabrication process for the H-diamond MOSFETs. An Ib-type diamond (100) substrate with a dimension of 8 × 8 × 0.3 mm^3 was cleaned in the H_2SO_4+HNO_3 acid solution at 300 ºC for 3 hours [Fig. 1(a)]. The H-diamond homoepitaxial layer was grown via a microwave plasma-enhanced chemical vapor deposition system [Fig. 1(b)]. The H_2 and CH_4 flow rates were 500 and 0.5 sccm, respectively. The deposition temperature, chamber pressure, and growth time for the H-diamond epitaxial layer were 900~940 ºC, 80 Torr, and 1.5 h, respectively. Thickness was around 150 nm. Mesa-structure was formed by etching the H-diamond in an O_2 ambient using a capacitively-coupled plasma reactive ion etching system [Fig. 1(c)]. The O_2 flow rate, chamber pressure, source power, and etching time were 100 sccm, 10 Pa, 50 W, and 90 s, respectively.

Source/drain Ohmic contact electrodes of Pd/Ti/Au with thickness of 10/20/200 nm were formed using an electron-gun evaporation system [Fig. 1(d)]. Oxide insulators of Al_2O_3/$HfSiO_2$ bilayer were deposited by atomic layer deposition (ALD) and sputtering deposition (SD) techniques, respectively [Fig. 1(e)]. The ALD-Al_2O_3 with a thickness of 4.0 nm contacted with the H-diamond directly. It impacts as a buffer layer to protect the hydrogen surface from damaged by the plasma discharge during the SD-$HfSiO_2$ deposition. The high dielectric constant SD-$HfSiO_2$ oxide insulator was employed to response the high hole density at a small gate voltage. Gate contact electrodes of Ti/Au (10/200 nm) were formed via the electron-gun evaporation system. Electrical properties for the H-diamond MOSFETs were measured with a four-probe system at room temperature.

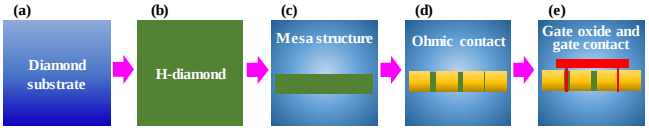

Fig. 1 Fabrication process for the H-diamond MOSFETs: (a) Cleaned diamond substrate, (b) H-diamond epitaxial layer growth, (c) mesa-structure formation, (d) Ohmic contact formation, and (e) Gate metal and gate contact formation.

III. Results and Discussion

A. Surface Morpholoy and Schematic Diagram

Figures 2(a), 2(b), and 2(c) show top views for the entire H-diamond MOSFETs, one planar-type MOSFET, and one T-type MOSFET, respectively. There are 720 H-diamond MOSFETs on the wafer. Gate width (W_G) for all of them is the same as 100 μm. Figs. 2(d) and 2(e) show schematic diagrams for the planar-type and T-type MOSFETs, respectively.

For the planar-type H-diamond MOSFETs, there are interspaces between source/drain and gate electrodes with the distances of 3.5 μm. The gate length (L_G) increases from 3.0 μm to 31.0 μm. For the T-type H-diamond MOSFETs, there are no interspaces between source/drain and gate electrodes. Therefore, on-resistance (R_{ON}) of the T-type H-diamond MOSFET is lower than that of the planar-type one with the same L_G.

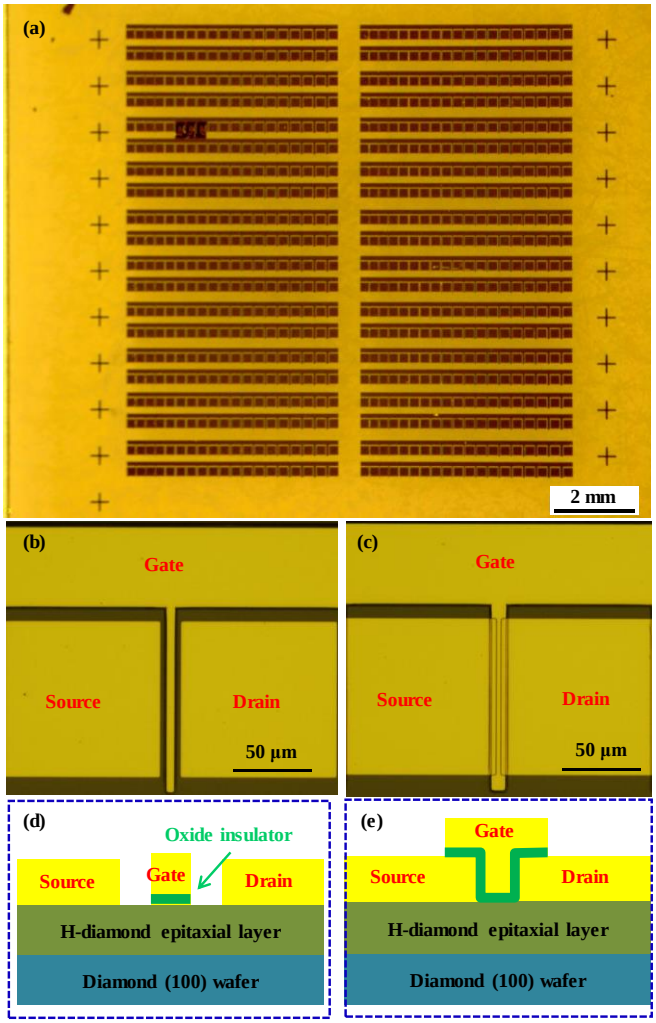

Fig. 2. (a), (b), and (c) Top views for the entire H-diamond MOSFETs, one planar-type MOSFET, and one T-type MOSFET, respectively. (d) and (e) Schematic diagrams for the planar-type and T-type MOSFETs, respectively.

B. Electrical properties for the H-diamond MOSFETs

Figures 3(a) and 3(b) show drain current (I_D) as functions of drain voltage (V_D) for the planar-type and T-type H-diamond MOSFETs, respectively. The L_G for both of them is the same as 3.0 μm. The I_D is normalized by the W_G of 100 μm. The measurement gate-to-source voltage (V_{GS}) is increased from −20.0 V to 10.0 V in steps of +1.0 V.

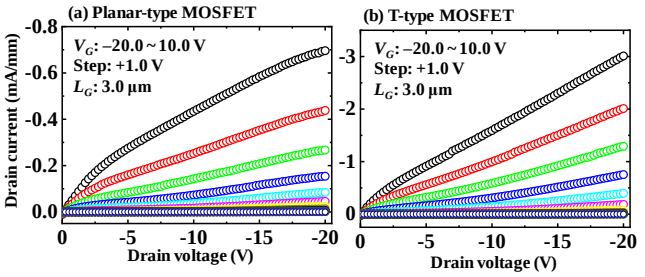

Fig. 3. (a) and (b) Drain current as functions of drain voltage for the planar-type and T-type H-diamond MOSFETs, respectively.

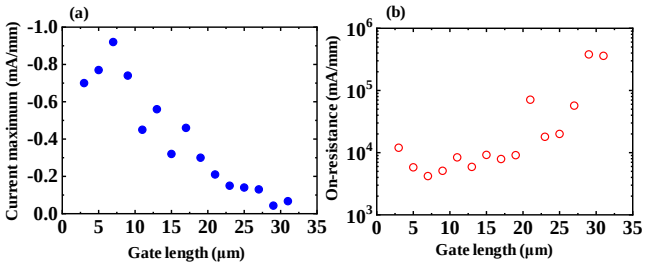

Fig. 4. (a) and (b) Current maximum and on-resistance as a function of gate length for the planar-type H-diamond MOSFETs, respectively.

Both planar-type and T-type MOSFETs show *p*-type characteristics and distinct pinch-off behaviors. The maximum I_D ($I_{D,max}$) values for the planar-type and T-type MOSFETs are −0.8 and −3.0 mA/mm, respectively. At V_{GS} = −20.0 V, the R_{ON} for the planar-type H- diamond MOSFET is 1.2×10^4 Ω mm, which is three times larger than that of the T-type MOSFET of 3.0×10^3 Ω mm. There are three kinds of resistances for the R_{ON} of planar-type H-diamond MOSFET, which are Pd/Ti/Au Ohmic contact resistance, channel resistance under oxide insulator, and the H-diamond surface resistance at the interspaces between source/drain and gate electrodes. Since the surface resistance for the T-type H-diamond MOSFET do not exist, it demonstrates smaller R_{ON} and larger $I_{D,max}$.

Figure 4(a) and 4(b) summarize the $I_{D,max}$ and R_{ON} as a function of the L_G for the planar-type H-diamond MOSFETs. With the L_G increasing from 3.0 μm to 31.0 μm, the $I_{D,max}$ has a decrease tendency and the R_{ON} has a increase tendency. The increase of the L_G indicates the enhancement of the channel resistance for the H-diamond MOSFETs, which leads to the variation of the $I_{D,max}$ and R_{ON}.

IV. Conclusions

In this study, we have fabricated the planar-type and T-type H-diamond MOSFETs on a large-area diamond wafer and investigated their electrical properties. This study is an initial stage to push forward the development of diamond MOSFETs for future practical applications.

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