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Communication—A Powerful Method to Improve Dielectric/GaN Interface Properties: A Dummy SiO_2 Process

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We report a simple and effective method for improving dielectric/GaN interface properties. In the process, a 5 nm thick SiO_2 layer was deposited onto a GaN(0001) substrate via plasma-enhanced atomic layer deposition, followed by annealing at 800 °C for 300 s under a flowing N_2 atmosphere. The SiO_2 layer was then removed using buffered HF solution, and Pt/Al_2O_3/GaN metal-oxide-semiconductor capacitors were fabricated on the substrate. Positive-bias stress tests revealed that the flat-band voltage shifts were substantially reduced for devices fabricated using this process, probably because of improved interface crystallinity. This method can also be applied to other dielectric/GaN systems.

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With the goal of efficient energy utilization, power devices based on a wide variety of semiconductor materials have been investigated. GaN is one of the most promising semiconductor materials because of its wide bandgap (3.4 eV) and well-developed device fabrication processes.[1–4] Metal-oxide-semiconductor field-effect transistors (MOSFETs) are a key component in such power devices; therefore, dielectric/GaN interfaces have been intensively studied since the late 1990s.[5] Among dielectrics, SiO_2/GaN has been the mainstream in such research because of its excellent interface properties.[6] As early as the 2000s, post-deposition annealing (PDA) was found to reduce the interface state density (D_{it}) to the lower 10^{11} cm^{-2} eV^{-1} range.[7,8] In-depth research has revealed that gallium oxide (GaO_x) interface layers formed at the SiO_2/GaN interfaces play a critical role in the outstanding interface properties;[9–14] however, the precise mechanism for the D_{it} reduction remains unclear. We have previously reported that the GaO_x interface layer exhibits a crystalline structure[15,16] that might be related to the lower D_{it}. In addition, some institutes, including ours, have reported that even the native oxide layers on GaN are crystalline rather than amorphous.[17–19] This finding is consistent with the difficulty associated with removing the native oxide layers on GaN.[20] Meanwhile, we have also found that the native oxide layers on GaN might be defective.[18] Thus, defective native oxide layers on GaN, which remain even after the cleaning process, can adversely affect the dielectric/GaN interface properties. We therefore speculate that PDA reduces the D_{it} for SiO_2/GaN via the following mechanism: PDA of SiO_2/GaN induces oxygen diffusion from SiO_2 toward the native oxide layer (i.e., the GaO_x interface layer), and Ga concurrently diffuses from the GaO_x interface layer toward the SiO_2, enhancing the crystalline quality of the interfacial GaO_x. Notably, oxygen diffusion from dielectric layers such as SiO_2 and HfO_2 toward GaN, and Ga diffusion from GaO_x interface layers toward SiO_2 during PDA have been confirmed.[14,21,22] On the basis of this proposed mechanism, we conceived a simple and effective method for improving the dielectric/GaN interface properties: a dummy SiO_2 process in which SiO_2 deposited onto GaN would enhance the crystalline quality of the GaO_x interface layers as follows. First, a SiO_2 layer is deposited onto GaN, followed by PDA, which enhances the GaO_x crystalline quality, as previously mentioned. The PDA temperature was set at 800 °C to diffuse unstable Ga from the GaO_x interface layers toward the SiO_2. Second, the SiO_2 layer is removed using a buffered HF solution because the SiO_2 quality is lowered as a result of the diffused Ga.[23] Third, a dielectric layer is deposited again to fabricate the MOS device. In this process, the initially deposited SiO_2 functions as a sacrificial layer; such layers are typically generated by sacrificial oxidation in the case of Si or SiC.[24] In the present study, we found that the flat-band voltage (V_{fb}) shifts that occur during positive-bias stress (PBS) tests were considerably reduced in devices fabricated using this process, suggesting that the crystalline quality of the GaO_x interface layer was increased, as expected.

Experimental

Figure 1 shows the process flow for the proposed method. We fabricated Pt/Al_2O_3/GaN MOS capacitors according to this process flow to confirm the effectiveness of the proposed method. Initially, a 5 μm-thick Si-doped n^- GaN homoepitaxial layer with a carrier concentration of 2×10^{16} cm^{-3} was grown on a free-standing n^+ GaN(0001) wafer via metal-organic vapor phase epitaxy. The carrier concentration and dislocation density in the wafer were 1×10^{18} cm^{-3} and on the order of 10^6 cm^{-2}, respectively. The wafer was subsequently cleaned with a H_2SO_4–H_2O_2 mixture, followed by treatment with a buffered HF solution for 30 s. Note that the presence of a crystalline native oxide layer with a thickness of ∼1 nm was confirmed after the GaN film was cleaned with the H_2SO_4–H_2O_2 mixture.[17,18] We also confirmed that buffered HF hardly etched β-Ga_2O_3 (at a rate of approximately 1.4–2.2 nm h^{-1}); therefore, crystalline native oxide layer was considered to remain on the GaN after the treatment with buffered HF solution for 30 s. Three different processes were then applied to the samples in parallel. In the first process, referred to as the standard process, the sample was not subjected to further treatment. In the second process, referred to as the pre800C process, the sample was annealed at 800 °C for 300 s under a flowing N_2 atmosphere in a rapid thermal annealing (RTA) system. In the third process, referred to as the dummy process, a 5 nm-thick SiO_2 layer was deposited on the sample via plasma-enhanced atomic layer deposition (PE-ALD) with a precursor of tris (dimethylamino)silane at 300 °C. After PDA at 800 °C for 300 s under a flowing N_2 atmosphere in an RTA system, the SiO_2 layer was removed with buffered HF solution. Note that the N_2 pressure and flow rate were 0.1 MPa (1 atm) and 0.3 slm, respectively, in the pre800C and dummy processes. Immediately after these three procedures, a 10 nm-thick Al_2O_3 layer was deposited onto the GaN via ALD at 300 °C using trimethylaluminum as a precursor and H_2O as an oxidant gas. As circular gate electrodes, a 100 nm-thick Pt layers (∼100 μm in diameter) was deposited onto the Al_2O_3 layer through a shadow mask via electron-beam deposition, followed by the deposition of a Ti (20 nm)/Pt (100 nm) Ohmic contact on the backside of the substrate to form a vertical capacitor. Post-metallization annealing (PMA) was finally performed at 300 °C

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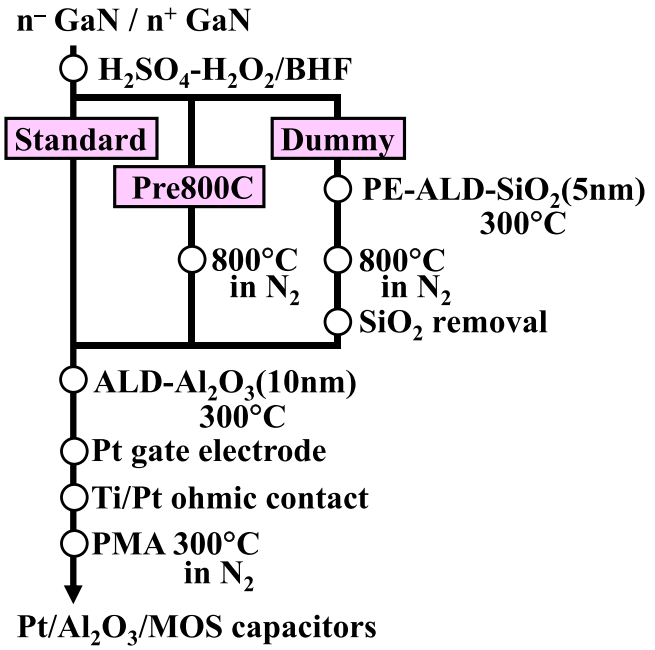

Figure 1. Process flow for fabricating MOS capacitors.

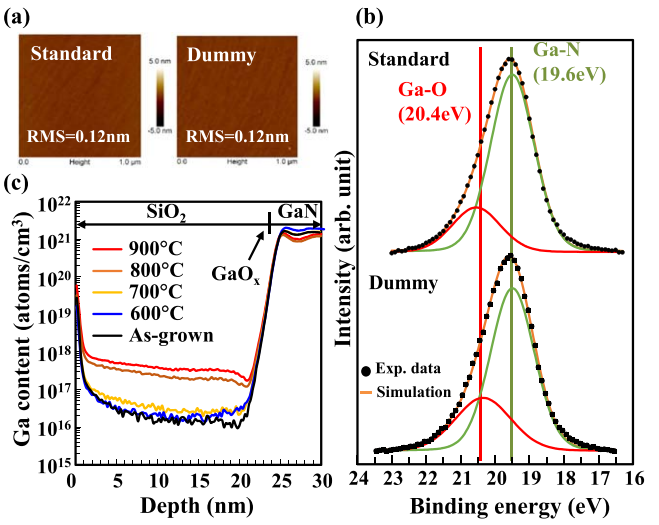

Figure 2. (a) AFM images of GaN surfaces after the standard (left) and the dummy (right) processes. (b) Ga 3*d* core-line XPS spectra of GaN surfaces after the standard (top) and the dummy (bottom) processes. (c) Ga depth profile in SiO_2/GaN subjected to various PDA conditions, as determined by SIMS measurements.

for 5 min under a N_2 flow in an RTA system.[25] The surfaces of the GaN samples after the standard and dummy processes were characterized by atomic force microscopy (AFM) before Al_2O_3 was deposited. In addition, the GaO_x layers on the GaN surfaces were investigated by X-ray photoemission spectroscopy (XPS) using monochromatized Al Kα X-ray radiation ($h\nu = 1486.6$ eV) with an energy resolution of 1 eV or better. For samples prepared by the dummy process, secondary-ion mass spectrometry (SIMS) analyses were carried out using O^{2+} primary ion bombardment with an energy of 1.5 keV before the SiO_2 layers were removed with a buffered HF solution, where positive atomic ions were monitored for the Ga signals (both ^{69}Ga and ^{71}Ga were monitored to confirm that the signals were due to real Ga and not from a mass interference). For fabricated Pt/Al_2O_3/GaN MOS capacitors, the capacitance–voltage (*C*–*V*) characteristics were evaluated using a semiconductor device parameter analyzer (B1500A, Agilent) at room temperature under dark conditions.

Results and Discussion

We first acquired AFM images of the GaN surfaces after the standard and dummy processes (Fig. 2a). The surface of the GaN sample after the dummy process was as smooth as that after the standard process, with the dummy GaN exhibiting a root mean square (RMS) surface roughness of 0.12 nm over a $1.0 \times 1.0\ \mu m^2$ field of view, suggesting that the dummy process did not lead to any surface roughness. We next used XPS to characterize the differences between the GaO_x layers on the GaN surfaces following the standard and dummy processes before Al_2O_3 deposition. Figure 2b shows Ga 3*d* core-line XPS spectra of the GaN surfaces after the standard (top) and the dummy (bottom) processes. The binding energy in the XPS spectra is displayed with reference to that of the N 1 s peak (397.4 eV). As shown in Fig. 2b, the Ga 3*d* peaks were deconvoluted into two components: a Ga–N bond peak at 19.6 eV and a Ga–O bond peak at 20.4 eV. The Ga–O signal after the dummy process (bottom) is slightly stronger than that after the standard process (top); therefore, the GaO_x layer on the GaN surface of the dummy sample may be denser and/or thicker than that on the GaN surface of the standard sample. We used SIMS to measure the diffusion of Ga in the SiO_2 layer after the annealing step in the dummy process; Fig. 2c shows the depth profile of the Ga concentration. Data corresponding to annealing temperatures in the range 600 –900 °C are displayed for comparison, along with the data for an as-grown sample. As can be seen, no noticeable Ga diffusion into SiO_2 was observed for samples annealed at temperatures of less than 700 °C. By contrast, the depth profiles for samples annealed at 800 or 900 °C show Ga diffusion to some extent. Given the results of a previous study,[14] we assume that unstable Ga atoms diffused from the GaO_x interface layer in samples annealed at 800 or 900 °C. Meanwhile, we have not obtained SIMS data for N atoms. According to the XPS data shown in Fig. 2b, the GaO_x interface layer could be thicker after the 800 °C annealing since the Ga-O signal after the annealing slightly stronger than that after the standard process, suggesting that some N atoms in GaN are replaced by O atoms diffused from the SiO_2 layers. Therefore, N atoms could diffuse from GaN toward SiO_2.

We conducted *C*–*V* measurements to investigate the interface properties of the fabricated Pt/Al_2O_3/GaN MOS capacitors. Figure 3 shows the results for devices fabricated on GaN samples using (a) the standard, (b) the pre800C, and (c) the dummy processes. The gate bias was swept from inversion to accumulation and back to inversion with various measurement frequencies ranging from 1 kHz to 1 MHz to reveal hysteresis. Notably, the measurement voltage was swept within a 2.0 V range with reference to the determined V_{fb} and the ideal V_{fb}, which was defined as the metal–semiconductor work function difference and was calculated to be 1.04 V for an effective Pt work function of 5.23 eV, an electron affinity of 4.1 eV for GaN,[26] and an intrinsic carrier concentration of 2×10^{-11} cm^{-3} for GaN.[27] As for the effective Pt work function, we deduced the value from a plot of V_{fb} as a function of oxide thickness for Pt/SiO_2/Si capacitors.[28] As shown in Figs. 3a–3c, no noticeable hysteresis was observed in any of the bidirectional sweeps; however, in the magnified views of the regions near V_{fb}, a small amount of hysteresis was confirmed, especially in the insets of Figs. 3a and 3b. We carried out *C*–*V* measurements with various voltage amplitudes at 1 MHz; the results are summarized in Fig. 3d, which shows the V_{fb} hysteresis as a function of the applied $|V-V_{fb}|$ at 1 MHz. Note that the maximum applied $|V-V_{fb}|$ was 4 V, which corresponds to 4 MV cm^{-1}. As shown in Fig. 3d, V_{fb} hysteresis was negligible for all of the samples prepared using the three processes when the applied $|V-V_{fb}|$ was less than 2.5 V. However, when the applied $|V-V_{fb}|$ was greater than 3.0 V, the V_{fb} hysteresis rapidly increased for samples prepared using the standard and pre800C processes. In particular, the pre800C samples exhibit the largest V_{fb} hysteresis among the samples prepared using the three processes, likely as a

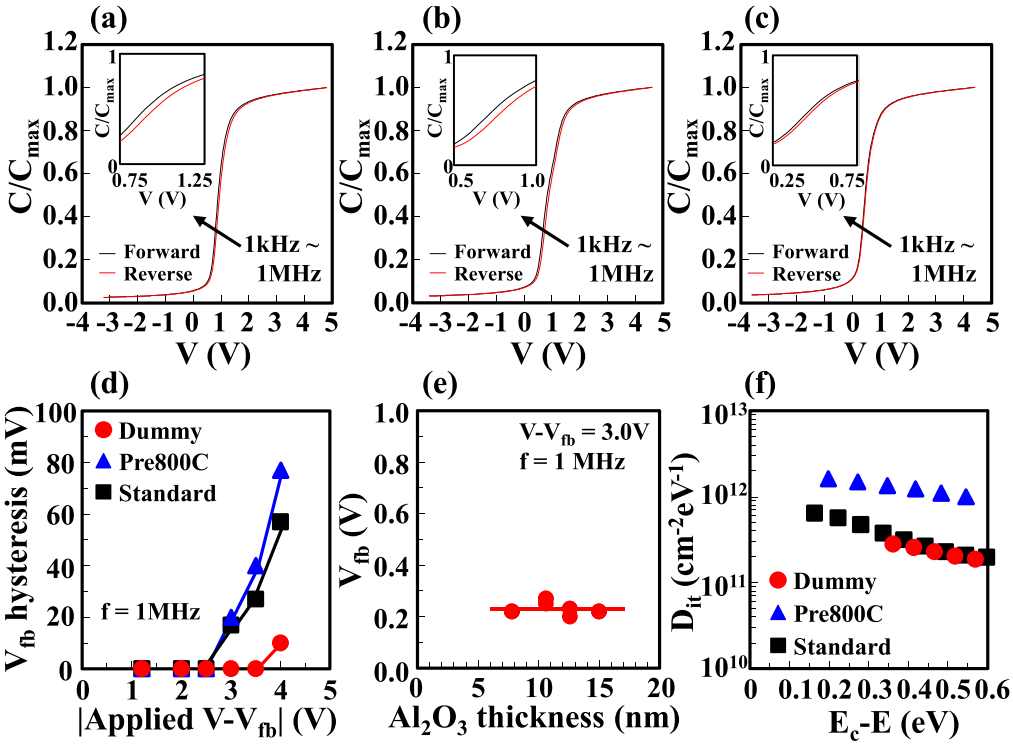

Figure 3. *C–V* characteristics for Al_2O_3/GaN MOS capacitors fabricated on GaN samples via (a) the standard, (b) the pre800C, and (c) the dummy processes. In (a)–(c), the measurement voltage was swept within a 2.0 V range with reference to the determined V_{fb}, and the insets show magnified views of the regions near V_{fb}. (d) Summary of the obtained V_{fb} hysteresis as a function of the applied $|V-V_{fb}|$ at 1 MHz. (e) V_{fb} at a measurement frequency of 1 MHz, plotted as a function of the Al_2O_3 thickness for Al_2O_3/GaN MOS capacitors fabricated on GaN samples via the dummy process. (f) D_{it} distribution for Al_2O_3/GaN MOS interfaces fabricated via three different processes. Here, black squares, blue triangles, and red circles show D_{it} values for samples fabricated using the standard process, the pre800C process, and the dummy process, respectively.

result of degradation of the surface after annealing at 800 °C. However, the dummy process drastically reduced the V_{fb} hysteresis, suggesting that the dummy process decreases the density of Al_2O_3/GaN interface traps by enhancing the crystalline quality of the interfacial GaO_x. We note an issue regarding V_{fb}: the V_{fb} for samples prepared using the dummy process slightly shifts in the negative voltage direction compared with that for samples prepared using the standard and pre800C processes (Figs. 3a–3c). The same trend has been reported for SiO_2/GaN MOS capacitors subjected to PDA.[14,29–31] To investigate this phenomenon, we acquired the V_{fb} values for Pt/Al_2O_3/GaN MOS capacitors with various Al_2O_3 thicknesses, prepared using the dummy process (Fig. 3e). If charges exist at the Al_2O_3/GaN interface, a plot of V_{fb} vs Al_2O_3 thickness should show a slope that is proportional to the charge density.[28] However, since this plot is not linear, we therefore assume that the negative-bias-direction V_{fb} shift for a sample obtained using the dummy process does not originate from charges at the Al_2O_3/GaN interface. In addition, charges in the Al_2O_3 layers were not responsible for the V_{fb} shift because all the Al_2O_3 layers were deposited under the same conditions in all three of the investigated processes. A possible explanation is GaN surface modification. That is, the GaN surfaces might no longer be GaN after the samples with SiO_2 layers are annealed; they might have transformed into GaON, as reported previously,[32,33] where the ideal V_{fb} might be less than 1.04 V. The Al_2O_3/GaN interface properties were further investigated using conductance measurements (Fig. 3f).[34] As shown in Fig. 3f, D_{it} for samples prepared using the standard and dummy processes was found to be on the order of 10^{11} cm^{-2} eV^{-1}, and that for samples prepared using the pre800C process was found to be in the lower 10^{12} cm^{-2} eV^{-1} range. In contrast to the drastic difference in V_{fb} hysteresis between the standard and dummy processes (Fig. 3d), the D_{it} values for samples prepared using these two processes are similar. This is attributable to the difference in trap energy levels; that is, the D_{it} shown in Fig. 3f corresponds to shallower energy levels and the V_{fb} hysteresis shown in Fig. 3d reflects deeper energy levels. The higher D_{it} for samples prepared via the pre800C process can be explained by the degraded surface after annealing at 800 °C, as previously mentioned. In other words, GaN was annealed at 800 °C for 300 s in N_2 without any encapsulation layers in the pre800C process. We speculate that the native oxide layers on GaN are degraded by the annealing, leading to the higher D_{it} at the Al_2O_3/GaN interface. We also confirmed that HF hardly etched β-Ga_2O_3 and consider that HF treatment has little effect on the native oxide layers on GaN; therefore, the higher D_{it} at the Al_2O_3/GaN interface in the pre800C process does not relate to the HF treatment. For the same reason, if the GaN undergoes HF treatment after the pre800C process, we speculate that the D_{it} at the Al_2O_3/GaN interface would not decrease.

Finally, we performed PBS tests to evaluate the effectiveness of the proposed method in terms of device reliability. Figure 4 shows V_{fb} shifts at a measurement frequency of 1 MHz as a function of stress time under various stress conditions for Al_2O_3/GaN MOS capacitors fabricated on GaN samples via the three processes. In Fig. 4, various bias voltages, $V-V_{fb}$, ranging from 2.0 to 4.0 V were applied for the duration indicated on the abscissa. The same trend observed in Fig. 3d is found. As shown in Fig. 4, the stronger the applied bias and the longer the stress time, the larger the V_{fb} shift for all of the samples, indicating that the time constant and energy depth for traps are diversified. Among samples prepared using the three processes, those prepared via the dummy process display distinct stability irrespective of the applied bias and stress time, presumably because of the enhanced crystalline quality of the interfacial GaO_x. However, the pre800C process resulted in the worst V_{fb} stability, which we attribute to the degraded surface after annealing at 800 °C.

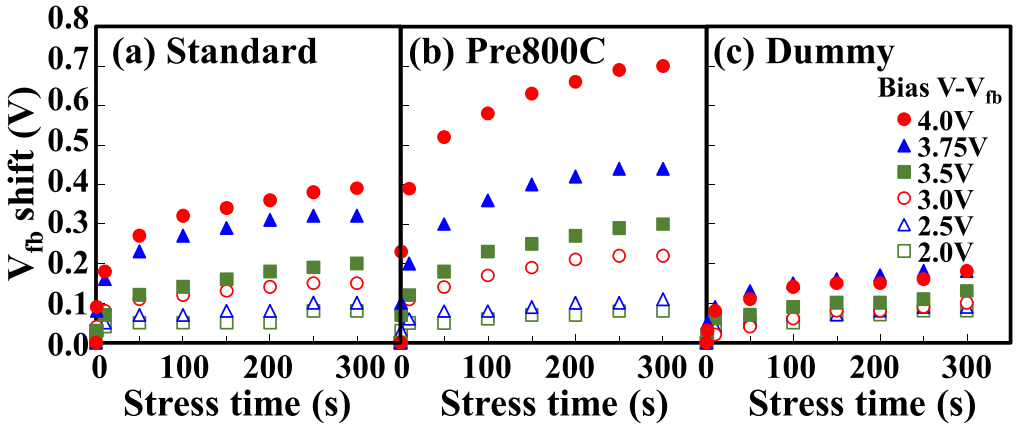

Figure 4. V_{fb} shifts at a measurement frequency of 1 MHz as a function the stress time under various stress conditions for Al_2O_3/GaN MOS capacitors fabricated on GaN samples using (a) the standard, (b) the pre800C, and (c) the dummy processes. Various bias voltages, $V-V_{fb}$, ranging from 2.0 to 4.0 V were applied for the duration indicated on the abscissa.

Conclusions

We proposed a simple and effective method referred to as the dummy SiO_2 process for improving dielectric/GaN interface properties. The process was found to drastically increase V_{fb} stability, possibly as a result of improved GaO_x interfaces. This method can be applied not only to Al_2O_3/GaN but also to other dielectric/GaN systems.

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References

1. T. Kachi, *2018 IEEE International Electron Devices Meeting Proceedings*, 452 (2018).
2. T. Oka, *Jpn. J. Appl. Phys.*, **58**, SB0805 (2019).
3. K. Ito, S. Iwasaki, K. Tomita, E. Kano, N. Ikarashi, K. Kataoka, D. Kikuta, and T. Narita, *Appl. Phys. Express*, **16**, 074002 (2023).
4. Y. Ichikawa, K. Ueno, T. Kondo, R. Tanaka, S. Takashima, and J. Suda, *Jpn. J. Appl. Phys.*, **63**, 02SP31 (2024).
5. S. J. Pearton, F. Ren, A. P. Zhang, and K. P. Lee, *Mater. Sci. Eng. R*, **30**, 55 (2000).
6. H. C. Casey, Jr, G. G. Fountain, R. G. Alley, B. P. Keller, and S. P. DenBaars, *Appl. Phys. Lett.*, **68**, 1850 (1996).
7. T. Sawada, Y. Ito, K. Imai, K. Suzuki, H. Tomozawa, and S. Sakai, *Appl. Surf. Sci.*, **159-160**, 449 (2000).
8. Y. Niiyama, T. Shinagawa, S. Ootomo, H. Kambayashi, T. Nomura, and S. Yoshida, *Phys. Stat. Sol. (a)*, **204**, 2032 (2007).
9. R. Therrien, H. Niimi, T. Gehrke, G. Lucovsky, and R. Davis, *Microelectron. Eng.*, **48**, 303 (1999).
10. R. Therrien, G. Lucovsky, and R. Davis, *Appl. Surf. Sci.*, **166**, 513 (2000).
11. Y. Nakano, T. Kachi, and T. Jimbo, *Appl. Phys. Lett.*, **83**, 4336 (2003).
12. C. Bae and G. Lucovsky, *J. Vac. Sci. Technol. A*, **22**, 2402 (2004).
13. T. Yamada, J. Ito, R. Asahara, K. Watanabe, M. Nozaki, T. Hosoi, T. Shimura, and H. Watanabe, *Appl. Phys. Lett.*, **110**, 261603 (2017).
14. T. Yamada, K. Watanabe, M. Nozaki, H. Yamada, T. Takahashi, M. Shimizu, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe, *Appl. Phys. Express*, **11**, 015701 (2018).
15. K. Mitsuishi et al., *Jpn. J. Appl. Phys.*, **56**, 110312 (2017).
16. Y. Irokawa, K. Mitsuishi, T. Nabatame, K. Kimoto, and Y. Koide, *Jpn. J. Appl. Phys.*, **57**, 118003 (2018).
17. Y. Irokawa, T. T. Suzuki, K. Yuge, A. Ohi, T. Nabatame, K. Kimoto, T. Ohnishi, K. Mitsuishi, and Y. Koide, *Jpn. J. Appl. Phys.*, **56**, 128004 (2017).
18. Y. Irokawa, K. Mitsuishi, T. T. Suzuki, K. Yuge, A. Ohi, T. Nabatame, T. Ohnishi, K. Kimoto, and Y. Koide, *Jpn. J. Appl. Phys.*, **57**, 098003 (2018).
19. J. H. Dycus, K. J. Mirrielees, E. D. Grimley, R. Kirste, S. Mita, Z. Sitar, R. Collazo, D. L. Irving, and J. M. LeBeau, *ACS Appl. Mater. Interfaces*, **10**, 10607 (2018).
20. B. S. Eller, J. Yang, and R. J. Nemanich, *J. Vac. Sci. Technol. A*, **31**, 050807 (2013).
21. S. J. Pearton, H. Cho, J. R. LaRoche, F. Ren, R. G. Wilson, and J. W. Lee, *Appl. Phys. Lett.*, **75**, 2939 (1999).
22. G. K. Bebek, J. H. Woo, S. Nikishin, H. R. Harris, and M. Holtz, *J. Vac. Sci. Technol. B*, **32**, 011213 (2014).
23. Y. Wada, M. Nozaki, T. Hosoi, T. Shimura, and H. Watanabe, *Jpn. J. Appl. Phys.*, **59**, SMMA03 (2020).
24. T. Hosoi, Y. Uenishi, Y. Nakano, T. Nakamura, T. Shimura, and H. Watanabe, *Mater. Sci. Forum*, **778-780**, 562 (2014).
25. T. Hashizume, S. Kaneki, T. Oyobiki, Y. Ando, S. Sasaki, and K. Nishiguchi, *Appl. Phys. Express*, **11**, 124102 (2018).
26. S. J. Pearton, C. R. Abernathy, and F. Ren, *Gallium Nitride Processing for Electronics, Sensors, and Spintronics* (Springer, London), 15 (2006).
27. B. J. Baliga, *Gallium Nitride and Silicon Carbide Power Devices* (World Scientific, Singapore), 22 (2017).
28. D. K. Schroder, *Semiconductor Material and Device characterization* (Wiley, New Jersey), 3rd ed., 336 (2006).
29. T. Yamada, D. Terashima, M. Nozaki, H. Yamada, T. Takahashi, M. Shimizu, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe, *Jpn. J. Appl. Phys.*, **58**, SCCD06 (2019).
30. S. Ogawa, H. Mizobata, T. Kobayashi, T. Shimura, and H. Watanabe, *J. Appl. Phys.*, **134**, 095704 (2023).
31. K. Aoshima, N. Taoka, M. Horita, and J. Suda, *Jpn. J. Appl. Phys.*, **61**, SC1073 (2022).
32. S. D. Wolter, J. M. DeLucca, S. E. Mohney, R. S. Kern, and C. P. Kuo, *Thin Solid Films*, **371**, 153 (2000).
33. Y. Irokawa, K. Mitsuishi, T. Izumi, J. Nishii, T. Nabatame, and Y. Koide, *ECS J. Solid State Sci. Technol.*, **12**, 055007 (2023).
34. K. Yuge, T. Nabatame, Y. Irokawa, A. Ohi, N. Ikeda, L. Sang, Y. Koide, and T. Ohishi, *Semicond. Sci. Technol.*, **34**, 034001 (2019).