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Gating monolayer and bilayer graphene with a two-dimensional semiconductor

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Metals are commonly used as electrostatic gates in devices due to their abundant charge carrier densities that are necessary for efficient charging and discharging. A semiconducting gate can be beneficial for certain fabrication processes, in low light conditions, and for specific gating properties. We determine the effectiveness and limitations of a semiconducting gate in graphene and bilayer graphene devices. Using the semiconducting transition metal dichalcogenides molybdenum disulfide (MoS_2), molybdenum diselenide ($MoSe_2$), tungsten disulfide (WS_2), and tungsten diselenide (WSe_2), we show that two-dimensional semiconductors can be used to suitably gate the graphene devices under appropriate operating conditions. For single-gated devices, semiconducting gates are comparable to metallic gates below liquid helium temperatures but include resistivity features resulting from gate voltage clamping of the semiconductor. In dual-gated devices, we pin down the parameter range of effective operation and find that the semiconducting depletion regime results in clamping and hysteresis from defect-state charge trapping.

Electrostatic gating in graphene devices has evolved over the years. The earliest devices employed highly doped silicon substrates as global back gates or evaporated metals for local top and bottom gates[1–3]. Recently, few-layer graphene has emerged as an ideal gate material for its atomically flat and chemically inert character. This leads to an overall reduction in charge inhomogeneity and observation of intricate correlated states when directly compared with deposited metal gates[4]. There are situations, though in which a semiconducting gate may be more appropriate. Semiconducting gates employed in high-mobility transistors provide over-voltage protection and lower leakage current when compared with metallic gates[5]. In novel high-frequency, on-chip terahertz measurements of graphene, a semiconducting gate is used to avoid absorption of the probing field[6,7]. Semiconducting gates could also play an important role in sensitive photodetectors and bolometers requiring minimal absorption or reflection from a top gate electrode[8,9]. They could boost the already impressive figures of merit for dual-gated bilayer graphene bolometers that take advantage of intrinsic bulk response by minimizing top gate interference thereby further increasing sensitivity[8]. The increased resistance of a semiconducting top gate would also be advantageous in high-bandwidth graphene photodetectors by reducing the RC time constant derived from the gate capacitance[9]. Furthermore, in comparison with semi-transparent nichrome or zinc oxide gates that are grown or deposited[10,11], 2D material stacks provide sharp, charge-homogeneous interfaces. These examples highlight the novelty of using a semiconducting gate but it has not been shown, given the depletion characteristics of a semiconductor, for what conditions electrostatic gating should function properly in a graphene device.

In a simple parallel-plate capacitor configuration with a metal and a two-dimensional electron gas (like graphene), applying a gate voltage (V_G) results in a change in the chemical potential (μ) in the graphene and the electrostatic potential (ϕ) between the two layers: $eV_G = e\phi + \mu$, where ϕ is determined by the geometric capacitance, $\phi = ne/C_G$. If a semiconductor replaces the metal as a gate, the reduction in overall charge density and presence of an electronic band gap will alter the gate response. As the Fermi level is driven into the band gap of the semiconductor while sweeping the gate contact voltage, the effective potential between the gate and the graphene channel will remain unchanged due to a lack of charge carriers in the gate itself. This voltage clamping effect of the gate will have meaningful consequences on the transport characteristics of a graphene device. Moreover, the temperature of the system becomes relevant as the threshold voltage in the gate changes and the thermal energy of carriers varies. This implies that the effect of sweeping beyond the threshold voltage of the semiconducting gate should be more pronounced at lower temperatures.

Here, we investigate the viability of using 2D transition metal dichalcogenides (MoS_2. $MoSe_2$, WS_2, WSe_2) as an electrostatic gate for monolayer and bilayer graphene (BLG) devices. MoS_2 is highlighted in the main text because it has the smallest difference in its electron affinity and graphene's

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work function when compared with the other transition metal dichalcogenides[12,13]. This results in ON state characteristics closest to zero gate voltage. In a single-gate response, we show that both mono- and bilayer graphene can be effectively gated down to liquid helium temperatures, albeit with resistance artifacts associated with clamping of the semiconducting gate. Dual-gated bilayer graphene with a few-layer graphene (FLG) control gate, allows us to clearly demarcate the parameter space applicable to efficient gating. A 1D potential model is modified to support our experimental results and corroborate gate voltages at which clamping occurs. Additionally, we observe significant hysteresis for clamped gate voltages that can be attributed to trap states from intrinsic defects. The onset of hysteresis is directly correlated with the threshold voltage of the semiconducting gate. Finally, we show that all four materials can be used to gate bilayer graphene, and we compare their differences. Our results provide specific guidelines for gating using semiconducting gates in graphene devices and pave the way for their use in sensitive detectors and spectroscopy.

Results

Single-gate characteristics

We construct 2D van der Waals heterostructures to assess the feasibility of a semiconducting gate. The devices are created using a dry stacking and transfer technique[14,15], and a summary of the seven devices measured in this study is shown in Supplementary Table 1 and Supplementary Fig. 1. Flakes of hexagonal boron nitride (h-BN) are employed as dielectric layers separating the gates from the graphene layers for all devices investigated. The Methods section presents the fabrication and measurement details for all devices studied. The single- and dual-gate results for bilayer graphene are presented here in the main text and results for a similar monolayer graphene device with an MoS_2 gate can be found in Supplementary Fig. 2. Figure 1a shows an optical image of a bilayer device with an MoS_2 gate with its stacking order shown as a model in the inset. The resistivity is measured using either the MoS_2 top gate (red layer in Fig. 1a) or the few-layer graphene (FLG) control gate (blue layer in Fig. 1a). By utilizing both the FLG and MoS_2 gates in a single device, we can directly compare the well-known gating behavior of FLG with the unknown gating characteristics of the semiconductor.

Figure 1b shows the individual gate-dependent transport characteristics of BLG at room temperature. Both the MoS_2 gate and FLG gate, when swept separately, yield the characteristic peak in resistivity at the charge neutrality point (CNP)[16–20]. The resistivity reported serves as an upper bound for the device as it includes the ungated regions of the BLG channel as well. The FLG gate achieves a lower resistivity at higher doping than the MoS_2 gate due to a larger area of overlap between the BLG and FLG flakes (the overlap can be seen in Fig. 1a). While the FLG gate shows no significant hysteresis, the MoS_2 gate response displays a shoulder feature with hysteresis between forward (solid) and backward (dashed) sweeps. These are associated with voltage clamping in the MoS_2 and explained in more detail below. Figure 1c–d present color maps of the gate-dependent transport at temperatures from 400 K down to 2.5 K. The CNP is evident as a central peak and does not shift as temperature decreases for either gate, highlighting the capability of MoS_2 for gating down to liquid helium temperatures. The CNP is situated to the left of zero gate voltage indicating some residual doping noticeable for both gates. From the CNP position, we determine the device has a residual n-doping of 0.126×10^{12} cm^{-2} possibly due to trapped contaminants at the BLG layer.

We extract the field-effect mobilities for the BLG holes and electrons from these gate sweeps to better characterize and compare the effects of both gates. Mobilities are calculated based on the Drude model[21] by taking the steepest slope of conductivity versus carrier density and using $\mu_{(h,e)} = \frac{1}{e}\frac{\partial \sigma}{\partial n_{(h,e)}}$. Figure 1e–f show the extracted mobilities as a function of temperature. Throughout the temperature range tested, the MoS_2 gate yields mobilities comparable to the FLG gate, with values similar to previous studies[22–24]. This confirms the efficacy of MoS_2 to operate as a gate over a wide range of temperatures.

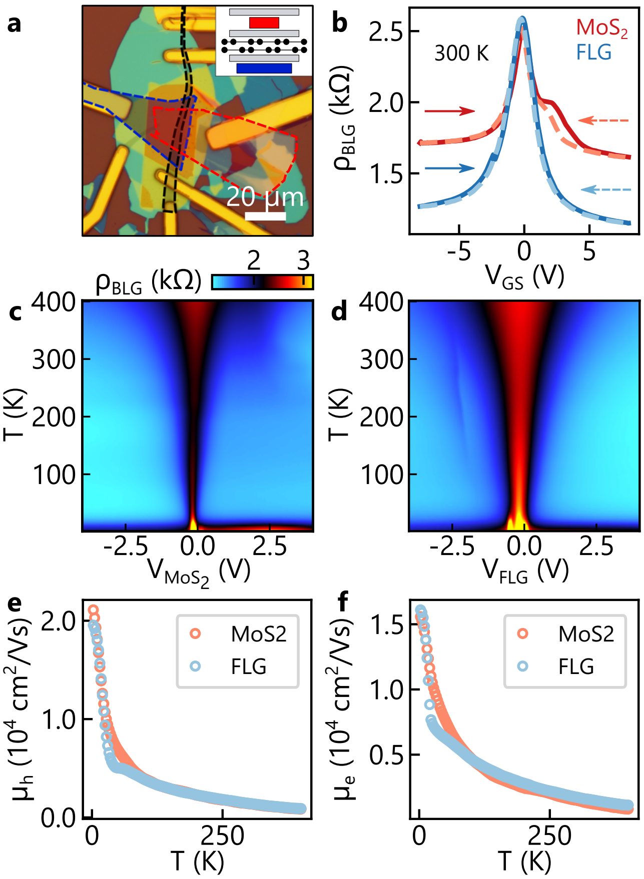

Fig. 1 | Graphite and MoS_2 gate comparison. a Optical microscope image of device. Outlined are the MoS_2 top gate (red), bilayer graphene (black), and graphite bottom gate (blue). Inset: Stacking order of the dual-gated graphene bilayer device with colors corresponding to outlines in main panel. Gray layers represent dielectric layers of h-BN. **b** Four-probe resistivity of the bilayer graphene as a function of gate-source voltage for MoS_2 gate (red) and FLG gate (blue) at 300 K. Solid lines represent forward sweeps, while dashed lines represent backward sweeps. Resistivity of the bilayer graphene mapped as a function of temperature and MoS_2 gate (**c**) or FLG gate (**d**). Color bar above (**c**) applies to (**d**) as well. For each gate sweep in (**b**–**d**), the inactive gate was held at zero volts. Field effect mobility of the holes (**e**) and electrons (**f**) in bilayer graphene as a function of temperature. The legend indicates whether the value is extracted from the MoS_2 data (**c**) or the FLG data (**d**).

Dual-gate characteristics

To more thoroughly investigate the parameter space, we expand our measurement to varying both gates simultaneously. The results of these 2D gate sweeps are presented in Fig. 2, where panels (a–e) show the MoS_2 as the fast forward sweep axis (from negative to positive voltage), and panels (f–j) show it as the fast backward sweep axis. At 400 K (a,f), the BLG resistivity shows two ridges of high resistivity. These ridges correspond to CNPs of different regions of the BLG: the horizontal line about $V_{FLG} = 0$ V corresponds to the region singly-gated by the FLG gate, and the diagonal line corresponds to the dual-gated region. We expect the CNP of the dual-gated region to occur where electrostatic doping by one gate is canceled by the other gate[18,24,25], creating a diagonal line with negative slope across the 2D plot. The total carrier concentration n in the BLG is calculated from the sum of the individual gate influences: $n = (C'_{MoS_2} V_{MoS_2} + C'_{FLG} V_{FLG})/e$, where C'_i is the capacitance per unit area between the BLG and gate i, and V_i is the voltage applied to gate i ($i \in \{MoS_2, FLG\}$). The slope of the CNP line (where $n = 0$ cm^{-2}) is $-C'_{MoS_2}/C'_{FLG} = -d_{FLG}/d_{MoS_2}$, where d_i is the thickness of dielectric layer between the graphene and gate i. An apparent linear portion of the CNP exists in quadrant II of Fig. 2a. Fitting to a line results in a slope of -1.44. This value closely matches the h-BN thickness ratio measured by AFM of $-d_{FLG}/d_{MoS_2} = -1.34$.

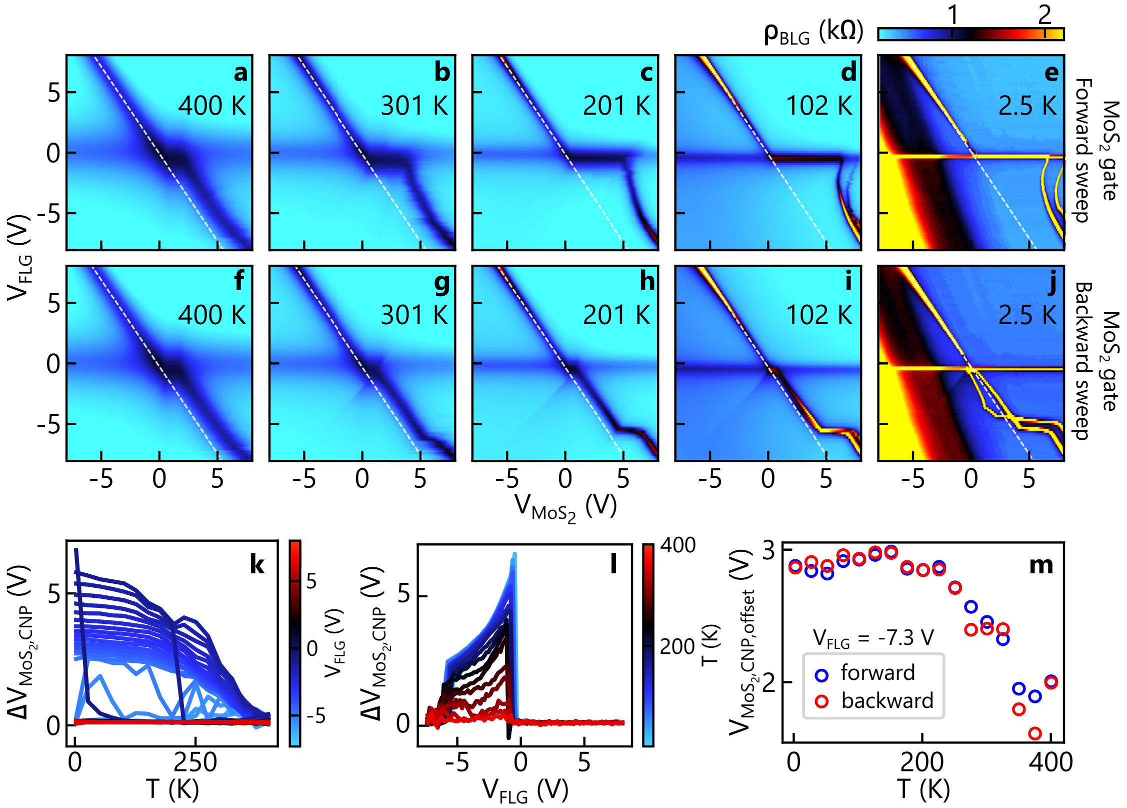

Fig. 2 | Dual-gated bilayer graphene sweeps. a–e BLG resistivity as a function of MoS_2 and FLG gate voltages. MoS_2 gate was swept along the fast axis forward (negative to positive voltage). The panels show the CNP evolution as a function of temperature, from 400 K (**a**) to 2.5 K (**e**). White dashed lines are linear fits to the CNP representing the expected gate voltages the CNP should appear. **f–j** Same as panels (**a–e**), but during the backward sweep (positive to negative voltage) of the MoS_2 gate. Color bar above (**e**) applies to (**a–j**). Hysteresis of BLG CNP appearance in MoS_2 gate voltage as a function of temperature and the graphite gate voltage: (**k**) shows the temperature dependence, while (**l**) shows the graphite gate dependence. **m** CNP offset from expected MoS_2 voltage at $V_{FLG} = -7.3$ V as a function of temperature for the MoS_2 forward sweep (blue) and backward sweep (red).

The definition of n assumes the charge density in each gate varies linearly with applied voltage, but this is not true for the semiconducting MoS_2 gate. This can be seen in quadrant IV of the 2D gate sweeps where the CNP becomes disjoint from that in quadrant II. The shift suggests a limitation of the MoS_2 gate. As the temperature decreases, the shift appears larger, especially in the forward sweep (Fig. 2b–e). Other features appear at lower temperatures as well, such as CNP splitting and non-monotonic CNP contours. These features are reproducible, but depend on both the sweep direction and which gate is being swept fast (MoS_2 or FLG) (see Supplementary Fig. 3). They coincide with the features seen in the 1D gate sweeps of Fig. 1, thus indicating single-gate sweeps must be carefully examined to assess limitations of the MoS_2 gate.

We perform further analysis of the 2D gate sweeps by looking at the hysteresis of the CNP feature with respect to the MoS_2 gate voltage. Figure 2k, l show the hysteresis $\Delta V_{MoS_2,\text{CNP}}$ as a function of temperature (k) and as a function of the FLG gate voltage (l). From panel (k), we see the magnitude of the hysteresis increases as temperature is decreased. Panel (l) shows for $V_{FLG} > 0$ V (corresponding to quadrant II of the 2D gate sweeps), hysteresis is minimal, but sharply increases at lower gate voltages. Notably, the hysteresis appears to drop back to zero at large negative FLG voltages, suggesting that gating becomes effective again. However, in Fig. 2m, we see the new CNP settles to a gate voltage that corresponds to a p-doped value of $\sim 2 \times 10^{12}$ cm^{-2}.

Semiconductor characteristics

Within the same device, we can measure the transport characteristics of the MoS_2 to determine properties such as its threshold voltage and its sheet conductivity[26–28]. For these measurements, two graphite contacts to the MoS_2 layer are used. Figure 3a shows the transconductance of the MoS_2 layer as a function of voltage applied to the BLG and FLG tied together, using both of them as a single global back gate. The conductivity measurements have a noise floor of approximately 10 pS. Most of the transconductance scans fall below this value in the MoS_2 off-state. We determine an on-off ratio of at least 10^6 and a field-effect mobility of roughly 30–70 cm^2/Vs depending on temperature, which is comparable to other reports[26,29–34]. At temperatures above 360 K, a notable leakage current dominates the off-state signal (see Supplementary Fig. 4). The inset of Fig. 3a shows the threshold gate voltage versus temperature, extracted by fitting the linear region of the transconductance with a line and finding its x-intercept[26,28]. The generally monotonic trend aligns with the expectation that thermally excited electrons contribute to turning on MoS_2 at lower gate voltages[32,34].

To better understand the limitations of the MoS_2 gate during electrical measurements of the BLG, we examine the MoS_2 characteristics for the same gating conditions shown in Fig. 2. Figure 3b and c show the conductivity of MoS_2 as a function of gate voltages relative to the BLG at 2.5 K and 300 K. This was achieved by setting a constant bias voltage V_{DS} across the MoS_2 while varying the potential on the BLG and FLG flakes. The relative potentials were adjusted to match the gate voltages applied during the 2D gate sweeps of the BLG resistivity. The voltages can be converted as follows:

$$V_{MoS_2-BLG} = -V_{BLG-MoS_2} \tag{1}$$

$$V_{FLG-BLG} = V_{FLG-MoS_2} - V_{BLG-MoS_2} \tag{2}$$

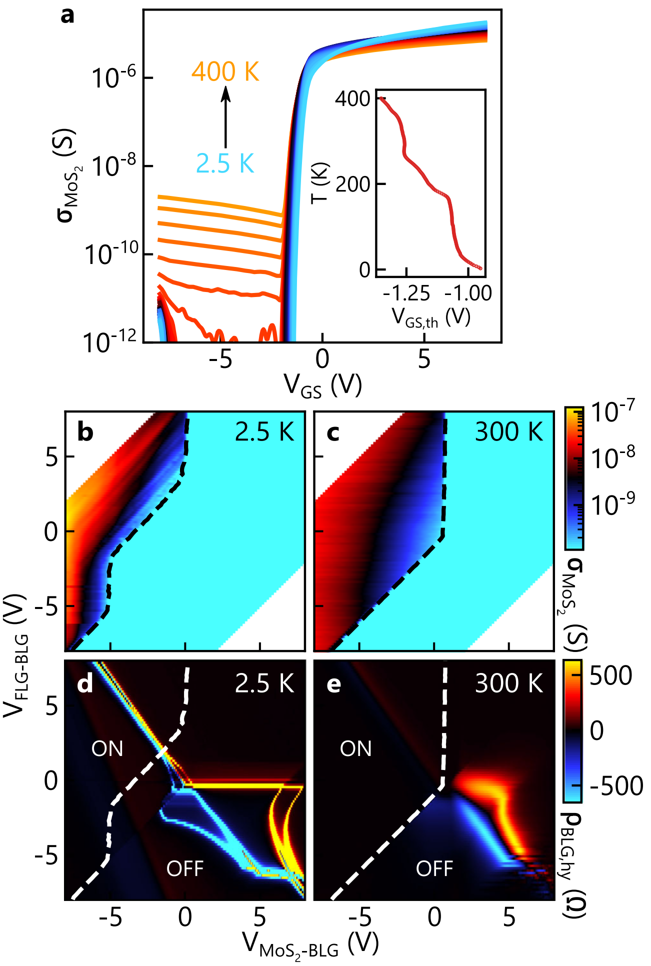

Fig. 3 | MoS_2 gate threshold and gating effectiveness. a MoS_2 conductivity as a function of gate-source voltage applied to electrically-connected BLG and FLG layers acting as a single back gate. Scans were taken from 2.5 K to 400 K, in steps of 7.5 K. Inset: Extracted threshold voltage as a function of temperature. MoS_2 conductivity as a function of gate voltage relative to the bilayer graphene at 2.5 K (**b**) and 300 K (**c**). Dashed line indicates the MoS_2 threshold voltage. Hysteresis of BLG resistivity (forward sweep minus backward sweep) as a function of gate voltage relative to BLG at 2.5 K (**d**) and 300 K (**e**). Dashed lines are the same as from panels (**b**, **c**).

where the convention V_{A-B} indicates a potential difference from layer A (positive side) to layer B (negative side). The dashed lines of Fig. 3b, c indicate the MoS_2 threshold voltage, determined by extracting the V_{MoS_2-BLG} corresponding to a MoS_2 conductivity just above the noise floor. This line effectively demarcates the transition between the on-state and off-state of the MoS_2 for the same gating conditions in Fig. 2.

We match the on-off state threshold voltage of the MoS_2 with the hysteresis of the BLG resistivity and see a distinct overlap. Figure 3d, e shows the difference in BLG resistivity between the forward sweep and backward sweep at 2.5 K and 300 K with the threshold voltage determined from panels (b-c) superimposed. Qualitatively, there is a distinct change in behavior of the CNP hysteresis when MoS_2 is in its on-state versus its off-state. Further analysis of low temperature hysteresis dependence on gate voltage sweep rate is available in Supplementary Fig. 5. In the off-state the hysteresis varies greatly. The forward and backward sweeps significantly misalign, as indicated by the divergence between the positive and negative values in the plot.

We highlight the success of the on-state MoS_2 gate by measuring the band gap opening of BLG as a function of displacement field, as shown in Supplementary Fig. 6. In the on-state of the MoS_2 gate, we determine a band gap of 53 meV at a displacement field magnitude of 0.77 V/nm, which is comparable to previously reported values measured with metallic gates[3].

The onset of hysteresis in the BLG can be explained by a voltage clamping effect of the MoS_2 gate. A 1D model calculating the effective potential between the BLG channel and the MoS_2 gate for different gate contact voltages has been adapted from Qian et al.[5] and is discussed in Supplementary Note 7, see also Supplementary Fig. 7. We find in the MoS_2 on-state, the potential follows the applied gate contact voltage as expected. However, upon entering the off-state above a threshold voltage of 1.2 V, the potential becomes clamped and remains constant for any applied gate contact voltage. This leads to the unchanged charge neutrality point in the forward sweeps shown in Figs. 2 and 3. The hysteresis observed between forward and backward sweeps may be due to intrinsic defects in the MoS_2 that act as trap states. The hysteresis reaches a maximum within the band gap of the MoS_2 and corresponds to a trap state density of $\approx 2 \times 10^{12}$ cm^{-2} (Supplementary Fig. 4d). This agrees with the reported magnitude of sulfur defect densities in MoS_2 flakes at 2.9×10^{12} cm^{-2}[35]. At the highest positive MoS_2 contact gate voltages and for finite negative FLG gate voltages, we observe an unclamping of the MoS_2 gate and re-emergence of a hysteresis-free CNP (Figs. 2l and 3e). We conjecture that the Fermi level in the MoS_2 gate reaches the valence band as a result of partial gating from the FLG flake through the low-density BLG layer. This occurs due to incomplete screening from a sandwiched 2D metal[36]. The splitting of the CNP at the lowest temperatures explored (Figs. 2e, j and 3d) is not expected but may be due to a crack in the MoS_2 flake causing two slightly different gating responses. We have observed cracking of various transition metal dichalcogenides during the van der Waals heterostructure fabrication process.

Comparison with $MoSe_2$, WS_2, and WSe_2

For direct comparison, we also present graphene devices utilizing $MoSe_2$, WS_2, and WSe_2 as semiconductor gates. The room temperature characteristics of three bilayer devices are presented in Fig. 4, and two additional $MoSe_2$ devices, as well as low temperature data, can be found in Supplementary Fig. 8. The architecture for these devices is the same as the MoS_2 bilayer device, with a FLG bottom gate used as a control gate. Figure 4a compares the transistor characteristics at room temperature of the four devices using four different materials. The MoS_2 curve is replotted from Fig. 3a. MoS_2 and $MoSe_2$ present n-type carrier response, WSe_2 presents p-type response, and WS_2 presents ambipolar response. In Fig. 4b–d, the BLG resistivity is plotted as a function of the semiconducting gate and the FLG control gate. As in Fig. 2, a white dashed line is plotted in Fig. 4b–d to identify the expected position of the CNP of BLG given two metallic gates. In the case of $MoSe_2$, the CNP becomes disjointed for electron transport in the BLG, similar to the MoS_2 device, while for WSe_2, the CNP becomes disjoint for hole transport. Given our analysis of the MoS_2 device, these are expected behaviors due to the n- and p-type response of these two semiconductors. The WS_2 device displays a relatively smaller shift in the CNP compared with the other materials due to its ambipolar response. The corresponding hysteresis in forward and backward gate sweeps are plotted in Fig. 4e–g for $MoSe_2$, WS_2, and WSe_2, respectively. The limits of the color scale have been chosen to match those in Fig. 3e for a better comparison between the four materials but note that the intensity of the subtracted hysteresis will also depend on the BLG resistivity itself. In comparison with the MoS_2 device, which had minimal hysteresis in the ON state at room temperature, these new materials present a greater range of hysteresis that spans the gate voltage parameter space.

Discussion

The comparison of all four materials invites strategic engineering of novel devices. For example, if electron transport and investigation around charge neutrality is primarily desired in a graphene device with a semiconducting gate, MoS_2 is the likely candidate, as it provides access to the largest range of density change with hysteresis-free gating. If, on the other hand, p-type transport is desired, WSe_2 provides the best characteristics. WS_2 presents a unique choice if amibpolar transport is needed away from charge neutrality. These general considerations are guidelines for device architecture, but details about the semiconducting gates must be considered. Our semiconducting gates have a range of thicknesses from bilayer to bulk-like (>6 layers). They

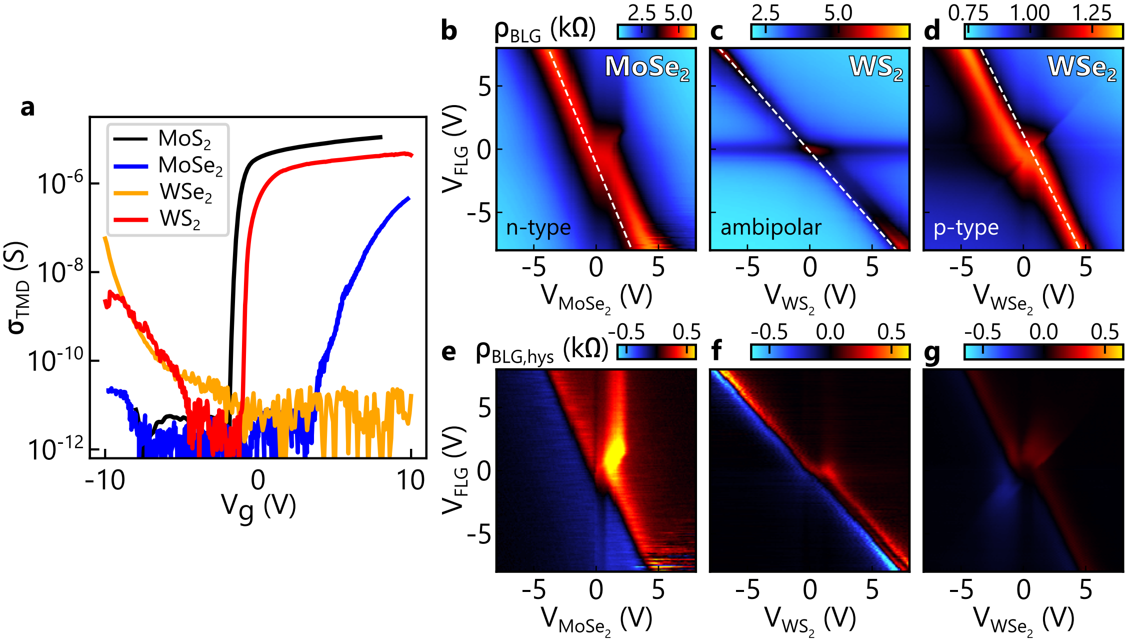

Fig. 4 | Gating bilayer graphene with MoSe$_2$, WS$_2$, and WSe$_2$ at room temperature. **a** Two terminal conductivity at room temperature for all four materials used as a semiconducting gate, as a function of gate-source voltage applied to electrically-connected BLG and FLG layers acting as a single back gate. BLG resistivity as a function of MoSe$_2$ (**b**), WS$_2$ (**c**), and WSe$_2$ (**d**), and FLG gate voltages. Hysteresis of BLG resistivity (forward sweep minus backward sweep) as a function of MoSe$_2$ (**e**), WS$_2$ (**f**), and WSe$_2$ (**g**) gate voltage relative to BLG at room temperature. For all 2D gate sweeps, the TMD gate voltage was the fast sweep axis.

are also contacted using few-layer graphene flakes, which determines the Schottky barrier between the semiconducting gate and its contact electrode. If different contact materials are used or the semiconducting gate enters the few-layer regime where the band gap is known to change[37,38], the detailed gating characteristics of a graphene device will also likely change.

We have demonstrated the ability of semiconducting transition metal dichalcogenides to electrostatically gate mono- and bilayer graphene. As a single gate, MoS$_2$ can effectively induce doping in graphene and bilayer graphene down to temperatures as low as 2.5 K. A shoulder feature in the 1D gate sweeps is identified and associated with voltage clamping in the MoS$_2$ gate. We find similar mobilities when using either the MoS$_2$ gate or a FLG control gate at high doping. In a dual-gate configuration, we identify a region of gate voltage parameter space where MoS$_2$ is in its on-state and provides adequate gating response. In the off-state, we observe voltage clamping of the MoS$_2$ gate leading to an unexpected deviation of the CNP from the linear trend in 2D gate parameter space. A 1D potential model corroborates this clamping effect. Hysteresis of the CNP in the MoS$_2$ off-state agrees with the filling and emptying of trap states from intrinsic sulfur vacancies. Finally, we directly compare bilayer graphene devices using other transition metal dichalcogenides (MoSe$_2$, WS$_2$, and WSe$_2$) showing unqiue n-type, p-type, and ambipolar characteristics. The advantages and disadvantages of using each material is discussed. Our results provide straightforward guidelines for the operation of a semiconducting gate in graphene devices and pave the way toward novel optoelectronic device architectures, high-frequency on-chip measurements, and sensitive detectors.

Methods

Materials were isolated from bulk crystals via mechanical exfoliation[1]. Exfoliated flakes were then assembled into a vertical heterostructure using a dry stacking method[14,15]. Few-layer graphene (graphite) flakes were used as contacts to the semiconducting gates to allow independent measurement of them. The final stack was fully encapsulated with h-BN. h-BN thicknesses are chosen according to optical contrast[39] and range from 20 to 70 nm. For the main text MoS$_2$ device, the thicknesses of the h-BN were measured using atomic force microscopy ($d_{MoS_2} = 26.7$ nm and $d_{FLG} = 35.9$ nm). A dielectric constant of $\epsilon_{BN} = 3.4\epsilon_0$ was also used, where ϵ_0 is the permittivity of free space[40]. A summary of the devices measured is presented in Supplementary Table 1 and optical microscopy images are shown in Supplementary Fig. 1. Standard photolithographic methods were used to pattern the electrodes. Graphite/graphene layers were exposed by etching away the h-BN in a CHF$_3$/O$_2$ plasma, then metal electrodes were either sputtered (Au 50 nm) at 5 mTorr or deposited by electron-beam evaporation (Cr 5 nm, Au 45 nm) at 10^{-6} Torr. Measurements were performed in a Quantum Design Evercool II PPMS and a Quantum Design Opticool cryostat, capable of base temperatures ~ 2.0 K. BLG resistivity measurements were performed in a two (TMDG026) or four-probe (all others) configuration. Semiconducting gate conductivity measurements were performed in a two-probe configuration.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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References

1. Novoselov, K. S. et al. Electric field effect in atomically thin carbon films. *Science* **306**, 666–669 (2004).
2. Zhang, Y., Tan, Y.-W., Stormer, H. L. & Kim, P. Experimental observation of the quantum hall effect and berry's phase in graphene. *Nature* **438**, 201–204 (2005).
3. Zhang, Y. et al. Direct observation of a widely tunable bandgap in bilayer graphene. *Nature* **459**, 820–823 (2009).
4. Zibrov, A. A. et al. Tunable interacting composite fermion phases in a half-filled bilayer-graphene landau level. *Nature* **549**, 360–364 (2017).
5. Qian, Q. et al. 2d materials as semiconducting gate for field-effect transistors with inherent over-voltage protection and boosted on-current. *npj 2D Mater. Appl.* **3**, 24 (2019).
6. Gallagher, P. et al. Quantum-critical conductivity of the dirac fluid in graphene. *Science* **364**, 158–162 (2019).

7. Seo, J. et al. On-chip terahertz spectroscopy for dual-gated van der waals heterostructures at cryogenic temperatures. *Nano Lett.* **24**, 15060–15067 (2024).
8. Yan, J. et al. Dual-gated bilayer graphene hot-electron bolometer. *Nat. Nanotechnol.* **7**, 472–478 (2012).
9. Yoshioka, K. et al. Ultrafast intrinsic optical-to-electrical conversion dynamics in a graphene photodetector. *Nat. Photonics* **16**, 718–723 (2022).
10. Kim, M.-H. et al. Photothermal response in dual-gated bilayer graphene. *Phys. Rev. Lett.* **110**, 247402 (2013).
11. Gopalan, K. K. et al. Mid-infrared pyroresistive graphene detector on linbo3. *Adv. Opt. Mater.* **5**, 1600723 (2017).
12. Liu, Y., Stradins, P. & Wei, S.-H. Van der waals metal-semiconductor junction: Weak fermi level pinning enables effective tuning of schottky barrier. *Sci. Adv.* **2**, e1600069 (2016).
13. Cloninger, J. A. et al. A back-to-back diode model applied to van der waals schottky diodes. *J. Phys.: Condens. Matter* **36**, 455301 (2024).
14. Purdie, D. G. et al. Cleaning interfaces in layered materials heterostructures. *Nat. Commun.* **9**, 5387 (2018).
15. Haley, K. L. et al. Heated assembly and transfer of van der waals heterostructures with common nail polish. *Nanomanufacturing* **1**, 49–56 (2021).
16. Geim, A. & Novoselov, K. The rise of graphene. *Nat. Mater.* **6**, 183–191 (2007).
17. Allen, M. J., Tung, V. C. & Kaner, R. B. Honeycomb carbon: A review of graphene. *Chem. Rev.* **110**, 132–145 (2010).
18. Yan, J. & Fuhrer, M. S. Charge transport in dual gated bilayer graphene with corbino geometry. *Nano Lett.* **10**, 4521–4525 (2010).
19. Kuzmenko, A. B. et al. Infrared spectroscopy of electronic bands in bilayer graphene. *Phys. Rev. B* **79**, 115441 (2009).
20. Efetov, D. K., Maher, P., Glinskis, S. & Kim, P. Multiband transport in bilayer graphene at high carrier densities. *Phys. Rev. B* **84**, 161412 (2011).
21. Gosling, J. H. et al. Universal mobility characteristics of graphene originating from charge scattering by ionised impurities. *Commun. Phys.* **4**, 30 (2021).
22. Cobaleda, C., Pezzini, S., Diez, E. & Bellani, V. Temperature- and density-dependent transport regimes in a *h*-bn/bilayer graphene/*h*-bn heterostructure. *Phys. Rev. B* **89**, 121404 (2014).
23. Tan, C., Adinehloo, D., Hone, J. & Perebeinos, V. Phonon-limited mobility in *h*-bn encapsulated *ab*-stacked bilayer graphene. *Phys. Rev. Lett.* **128**, 206602 (2022).
24. Shimazaki, Y. et al. Generation and detection of pure valley current by electrically induced berry curvature in bilayer graphene. *Nat. Phys.* **11**, 1032–1036 (2015).
25. Henriksen, E. A. & Eisenstein, J. P. Measurement of the electronic compressibility of bilayer graphene. *Phys. Rev. B* **82**, 041412 (2010).
26. Late, D. J., Liu, B., Matte, H. S. S. R., Dravid, V. P. & Rao, C. N. R. Hysteresis in single-layer mos2 field effect transistors. *ACS Nano* **6**, 5635–5641 (2012).
27. Cho, K. et al. Electric stress-induced threshold voltage instability of multilayer mos2 field effect transistors. *ACS Nano* **7**, 7751–7758 (2013).
28. Lee, G.-H. et al. Highly stable, dual-gated mos2 transistors encapsulated by hexagonal boron nitride with gate-controllable contact, resistance, and threshold voltage. *ACS Nano* **9**, 7019–7026 (2015).
29. Jariwala, D. et al. Band-like transport in high mobility unencapsulated single-layer MoS2 transistors. *Appl. Phys. Lett.* **102**, 173107 (2013).
30. Bartolomeo, A. D. et al. Hysteresis in the transfer characteristics of mos2 transistors. *2D Mater.* **5**, 015014 (2017).
31. Lin, M.-W. et al. Thickness-dependent charge transport in few-layer mos2 field-effect transistors. *Nanotechnology* **27**, 165203 (2016).
32. Radisavljevic, B. & Kis, A. Mobility engineering and a metal–insulator transition in monolayer mos2. *Nat. Mater.* **12**, 815–820 (2013).
33. Yang, H., Cai, S., Wu, D. & Fang, X. Humidity-dependent characteristics of few-layer mos2 field effect transistors. *Adv. Electron. Mater.* **6**, 2000659 (2020).
34. Ji, H. et al. Temperature-dependent opacity of the gate field inside mos2 field-effect transistors. *ACS Appl. Mater. Interfaces* **11**, 29022–29028 (2019).
35. Trainer, D. J. et al. Visualization of defect induced in-gap states in monolayer mos2. *npj 2D Mater. Appl.* **6**, 13 (2022).
36. Luryi, S. Quantum capacitance devices. *Appl. Phys. Lett.* **52**, 501–503 (1988).
37. Mak, K. F., Lee, C., Hone, J., Shan, J. & Heinz, T. F. Atomically thin mos 2: a new direct-gap semiconductor. *Phys. Rev. Lett.* **105**, 136805 (2010).
38. Splendiani, A. et al. Emerging photoluminescence in monolayer mos2. *Nano Lett.* **10**, 1271–1275 (2010).
39. Golla, D. et al. Optical thickness determination of hexagonal boron nitride flakes. *Appl. Phys. Lett.* **102**, 161906 (2013).
40. Pierret, A. et al. Dielectric permittivity, conductivity and breakdown field of hexagonal boron nitride. *Mater. Res. Express* **9**, 065901 (2022).

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Author contributions

R.M.S., B.K., A.F., K.L.H., and N.T.P. fabricated the devices. R.M.S. performed the measurements and modified the 1D gating model. K.W. and T.T. grew the hBN crystals. R.M.S. and J.O.I. wrote the manuscript in consultation with K.L.H. and N.T.P.

Competing interests

The authors declare no competing interests.

Additional information

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