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Top-down fabrication of Ge nanowire arrays and hole gas accumulation in Ge/Si core–shell nanowires

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Germanium (Ge) nanowire arrays are expected to be a promising channel material for high-performance field-effect transistors (FETs) due to their excellent electronic transport properties, silicon (Si) compatibility, and high integration. To produce highly ordered Ge nanowires with low contamination, nanoimprint lithography (NIL) and Bosch etching were used and the size of nanowires was reduced from 220 nm to ~30 nm by adjusting the H₂O₂ etching time. Furthermore, Ge/Si core–shell nanowires were fabricated by forming p-Si shells on the Ge nanowires. This structure is used as a high-mobility channel in HEMT-type devices, and the accumulation of hole gas inside the Ge nanowires, which is the most important, was demonstrated.

Introduction

Vertically aligned semiconductor nanowires are of particular interest due to their large surface-to-volume ratio and vertical architecture allow transistors to be integrated perpendicularly to the substrate with surrounding gates, resulting in superior performance, low power consumption, and high-density packaging.^{1,2} As a silicon (Si)-compatible semiconductor, germanium (Ge) has high electron and hole mobilities (about two and four times higher than silicon), which make it extremely appealing for applications in electronics and optoelectronics. Ge nanowire has been proposed to be an ideal channel material for next-generation vertical gate-all-around field-effect transistors (GAAFETs) with high switching speed.

Vertically aligned Ge nanowires are generally fabricated using vapor–liquid–solid (VLS) growth, which is a bottom-up method that uses metal nanoparticles to catalyze the nanowire growth.^{3–6} Metal contamination by the catalysts will introduce deep levels in the forbidden gap of the material, acting as carrier recombination centers and degrading electrical properties. On the other hand, different catalyst compositions and nanowire diameters in VLS growth lead to different preferential growth directions of Ge nanowires,^{7,8} making the fabrication of highly ordered arrays a challenge. Top-down approaches such as electron-beam lithography (EBL) and nanoimprint lithography (NIL) can be used to address these problems. Combined with Bosch etching, these top-down methods have been widely used to realize Si nanowire arrays with small diameters and high aspect ratios.^{9–11} However, due to the challenges associated

with the surface chemistry of Ge, there are few reports on the top-down fabrication of Ge nanowire array.

On the other hand, functionalization of Ge nanowires requires impurity doping, which causes impurity scattering and degrades performance. By constructing a heterostructure of Ge and p-Si, quantum wells can be formed due to its type II band alignment.^{12–19} Therefore, by generating hole gas in the Ge region, impurity doping regions and carrier transport regions can be separated, thereby suppressing impurity scattering and improving carrier mobility. This structure is used as a high-mobility channel in high electron (hole) mobility transistor (HEMT)-type devices. As the hole concentration of Ge increases, the optical phonon peak of Ge shifts to the lower wavenumbers and broadens asymmetrically. This redshift and deformation of the line shape is corresponding to the Fano effect,^{20–25} which can be used to estimate the carrier concentration of semiconductors. Micro-Raman spectroscopy is commonly used to study the optical phonons of Ge and to demonstrate the hole gas accumulation of Ge/p-Si nanowire heterostructures.^{19,26,27}

In this study, we demonstrate a catalyst-free fabrication of uniform Ge nanowire arrays using NIL, which is the most desirable top-down method in terms of low cost, high throughput, and low contamination. Bosch etching produced nanowires with smooth surfaces and high aspect ratios, and the diameter of the nanowires is controlled by wet chemical etching at room temperature. To introduce the carrier in the Ge, Ge/p-Si core–shell nanowire heterostructures with different core sizes are fabricated by the chemical vapor deposition (CVD) method. The hole gas accumulation in the Ge core region is investigated by Raman scattering analysis.

Results and discussion

Fabrication of Ge nanowire arrays

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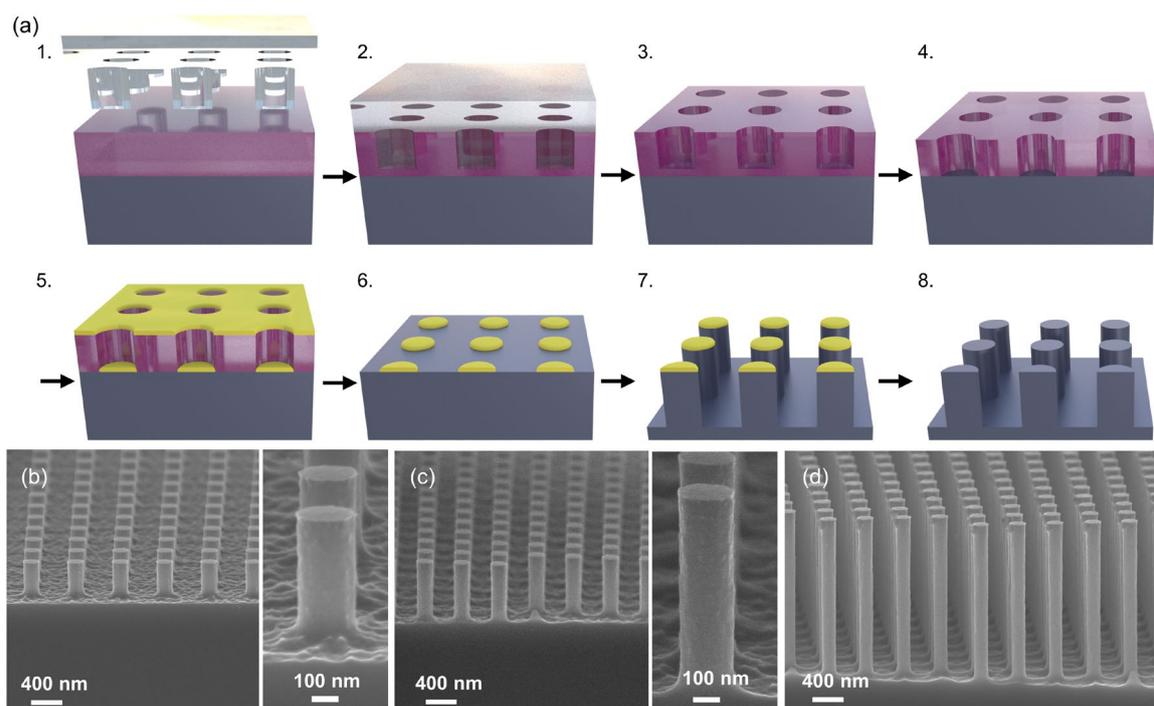


Fig. 1 (a) Illustration of the Ge nanowire fabrication process using nanoimprint lithography: (step 1) Ge substrate with spin-coated photoresist; (step 2) nano-patterned quartz mold attaching to the photoresist followed by a UV irradiation; (step 3) quartz mold detaching; (step 4) removing residual resist by RIE; (step 5) depositing MgO as a hard mask on the imprinted resist; (step 6) lift-off; (step 7) Bosch etching; (step 8) removing hard mask. Quartz mold, photoresist, substrate, and hard mask is represented by transparent, purple, gray, and yellow color, respectively. 75°-tilted SEM images of fabricated Ge nanowire arrays using Bosch process cycle numbers of (b) 15, (c) 25, and (d) 60. The insets show the magnification SEM images of the nanowires.

Fig. 1a shows the fabrication process of Ge nanowire arrays by nanoimprint lithography, which is divided into two parts: fabrication of photoresist nanohole arrays and fabrication of nanowire arrays. First, a UV-curable imprint photoresist is spin-coated onto the Ge substrate, and resist layer thickness can be controlled by the resist composition and spin rate. Next, a quartz mold with a periodic nanopillar pattern on it is placed in contact with the photoresist layer to form an inverted pattern (nanohole arrays) on the photoresist. The transparent quartz mold is then irradiated with UV light to cure the photoresist. After the mold is removed, the nanohole arrays are imprinted onto the resist. Since a thin layer of photoresist remains at the bottom of the nanoholes, a reactive ion etching (RIE) process is used to remove the remaining layer until the substrate surface is exposed. To fabricate nanowire arrays, a MgO thin film is deposited as a hard mask on the imprinted resist pattern. The mask above the resist is lifted off with chemicals, leaving a patterned hard mask on the Ge substrate. Next, a deep etching process (a so-called Bosch process) is performed to etch the Ge substrate vertically to a high depth by alternating anisotropic etching and passivation film deposition. Here, the number of Bosch cycles is set between 15 and 60 to adjust the length of the nanowires. Finally, the MgO mask on the nanowire tip is removed by acid at room temperature.

The scanning electron microscopy (SEM) images in Fig. 1b–d show that Ge nanowires with a well-ordered alignment and smooth surface were successfully fabricated. The nanowire diameter is about 220 nm and the pitch size is 600 nm. 15, 25, and 60 cycles of Bosch processing yielded nanowire arrays with heights of 500, 830, and 2140 nm, respectively. The nanowire,

even the longest ones, appear to have almost no taper (Fig. 1d). This indicates that even longer Ge nanowires can be achieved by increasing the number of Bosch cycles. The Bosch etching rate for Ge here is about 35 nm/cycle, which is about twice that of Si under the same etching conditions.

The nanowire surface formed by Bosch etching is damaged.²⁸ Removal of the surface damaged layer is important for device applications. Furthermore, the electrical and optical properties of nanowires are highly dependent on their size, it is important to control the size of nanowires to tune their physical properties and achieve high integration. In the case of Si, reducing the diameter of Si nanowire arrays with smooth surfaces requires prolonged (8 hours) thermal oxidation at a high temperature (950°C).²⁷ Unlike Si, Ge can be easily etched by wet chemical etching at room temperature^{29,30} and H₂O₂ was chosen here because of its appropriate etching rate. The H₂O₂ etching process is illustrated in Fig. 2a and the SEM images in Fig. 2b–e showing the morphology of Ge nanowire arrays with different etching times. H₂O₂ treatments of 0, 100, 200, and 240 s resulted in the nanowire arrays with diameters of approximately 220, 150, 90, and 30 nm, respectively. The etching rate of Ge here is about 20 nm/min, which is in good agreement with the value reported by D. P. Brunco et al.²⁹ By the way, if the nanowires are too thin, they would be damaged by capillary force during drying. Therefore, in the case of the Ge nanowire arrays in Fig. 2e, samples were washed with IPA immediately after H₂O₂ etching.

Hole gas accumulation in Ge/Si core-shell nanowires

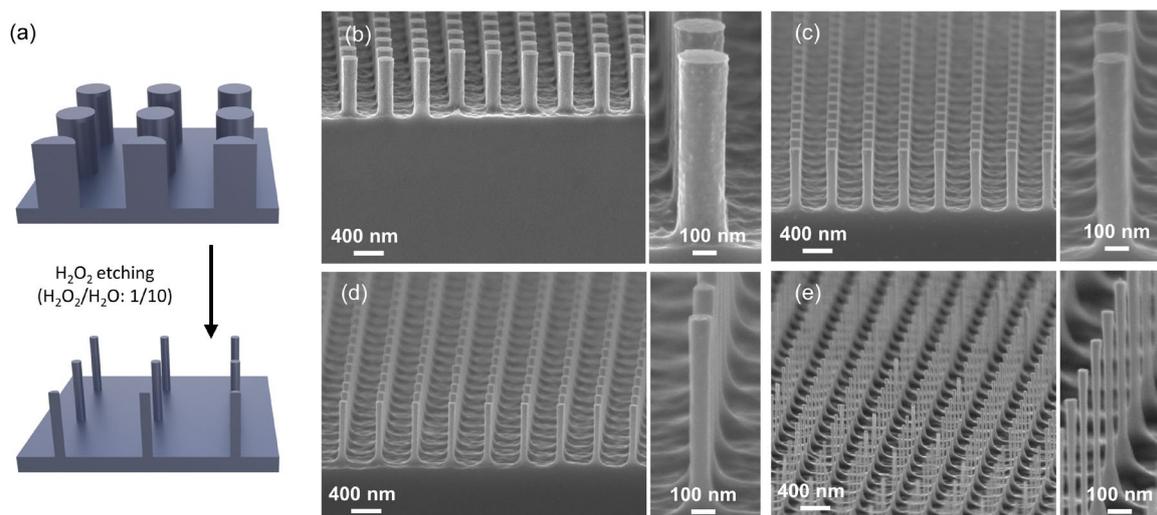


Fig. 2 (a) Schematic illustration of wet chemical etching process for reducing the Ge nanowire size. 75°-tilted SEM images of Ge nanowire arrays treated by H₂O₂ etching with etching times of (b) 0 s, (c) 100 s, (d) 200 s, and (e) 240 s. The insets show the magnification SEM images of the nanowires.

To functionalize the Ge nanowires, a Ge/p-Si core-shell heterostructure is utilized to generate the hole gas in the Ge core. In the conventional p-Si/Ge core-shell structures shown in Fig. 3b, hole gas accumulates in the shell region, which is grown hetero-epitaxially. The lattice mismatch between Ge and Si and contaminants on the Si surface can lead to a high density of defects such as misfit dislocations in the Ge shell, which will reduce its carrier mobility. Conversely, in the Ge/p-Si core-shell nanowire structure in Fig. 3a, hole gas accumulates in the core region. Here, Ge nanowires (core region) are fabricated top-down from the substrate, resulting in very good crystal quality. Therefore, the Ge/p-Si core-shell structure is expected to have higher carrier mobility than the p-Si/Ge core-shell structure. On the other hand, Ge is easier to size than Si as the core, because Si requires higher temperatures, longer time, and more expensive equipment to make it smaller²⁷. Furthermore, the doping concentration can be easily controlled by adjusting the flow rate of dopant precursor gas during shell formation.

Fig. 4a,b shows the morphology of the fabricated Ge/p-Si core-shell nanowire arrays with two different core sizes. For both core sizes, the CVD process yielded a p-Si shell about 40

nm thick with a smooth surface. The growth rate of p-Si is comparable to the previously reported p-Si shells grown on Si/Ge core-shell nanowire arrays²⁷. In order to investigate the hole carriers in Ge core, Raman scattering analysis is carried out using the Fano effect,^{31,32} which can be described as follows

$$I(\omega) = I_0 \frac{(q + \varepsilon)^2}{(1 + \varepsilon^2)} \quad (1)$$

where ω is the wavenumber, I_0 is the prefactor, q is the asymmetry parameter, and $\varepsilon = (\omega - \omega_p)/\Gamma$. Here, ω_p is the phonon wavenumber and Γ is the line width-related parameter²¹. These Fano parameters represent the line shape of Raman optical phonon and can be used to estimate the doping concentration in semiconductors. As the hole concentration increases, the Ge phonon peak shifts to lower wavenumbers and broadens with negative skewness (Fano parameter $q < 0$).

Fig. 4c shows the asymmetric broadening and downshift of Ge optical phonon peaks after the formation of the boron-doped Si shells. The Fano parameters fitted from the Ge peaks using the Fano function are shown in Fig. 4d-f. The Ge phonon peak of Ge/p-Si core-shell nanowire arrays shifts to lower wavenumbers, and the Fano parameters q and Γ increase compared to Ge/i-Si core-shell nanowire arrays, demonstrating hole gas accumulation in the Ge region. Here, the crystal quality of the Ge core should be comparable to that of bulk Ge, and the core size is too large to exhibit phonon confinement effects, so peak shifts and asymmetric broadening due to the phonon confinement effect can be ignored. In the case of nanowire arrays with large core sizes, the peak shifts to higher wavenumbers, and Fano parameters q and Γ are reduced compared to nanowire arrays with small core size, indicating a decrease in the hole gas concentration in the Ge region. This can be explained by the dilution of the accumulated hole gas by the increased area of Ge. Incidentally, the Ge phonon peak of the Ge/i-Si core-shell nanowire arrays is blue-shifted compared to that of the bulk Ge, which is attributed to compressive stress induced by the Ge/Si heterojunction. By comparing the Fano

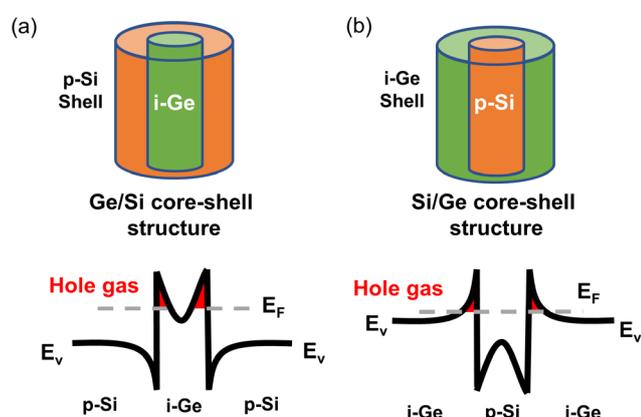


Fig. 3 Schematic illustrations and corresponding band diagrams of (a) Ge/p-Si and (b) conventional p-Si/Ge core-shell nanowires. E_v and E_f are the valence band edge and the Fermi energy, respectively. The hole gas accumulation is represented by red color.

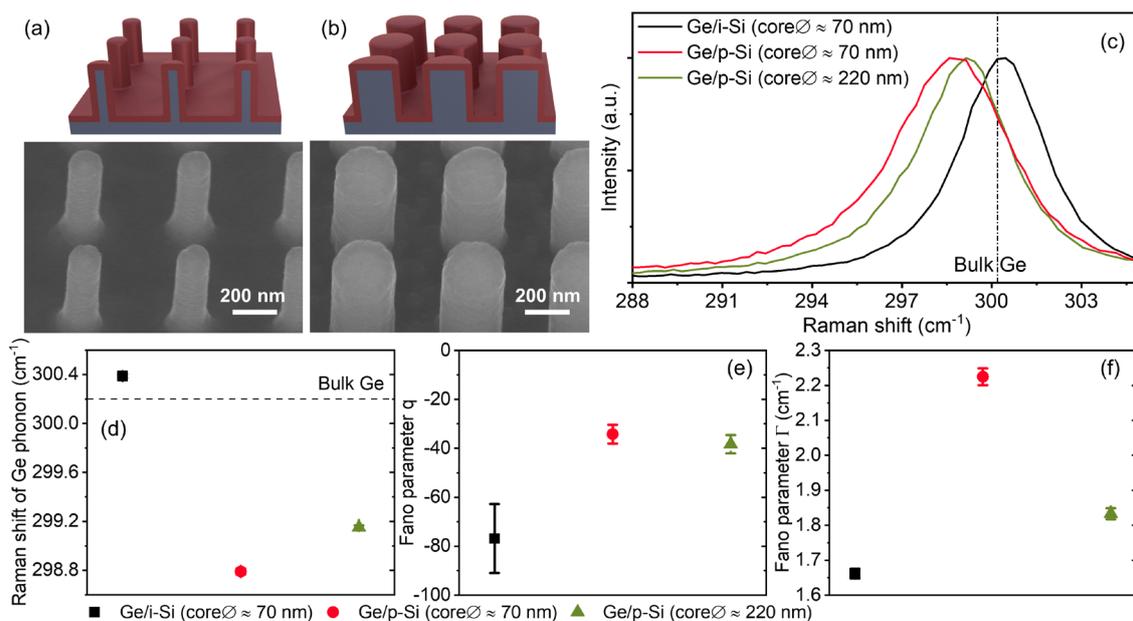


Fig. 4 Illustrations and corresponding 30°-tilted SEM images of Ge/Si core-shell nanowire arrays with core size of (a) 70 nm and (b) 220 nm. (c) Raman spectra of Ge/i-Si nanowire arrays and Ge/p-Si nanowire arrays with different core sizes. (d) Raman shift, (e) Fano parameter q , and (f) Fano parameter Γ obtained by fitting corresponding Ge optical phonon peaks with the Fano function. Standard deviation in Raman measurements is represented by the error bars.

parameters with the previously reported results^{27,33}, the hole concentration in the Ge region of Ge/p-Si core-shell nanowires can be estimated to be on the order of 10^{19} cm^{-3} , although it may be underestimated by the compressive stress in Ge.

Conclusions

In this work, we demonstrate a top-down fabrication of Ge nanowire arrays by NIL and show that different lengths (from 500 nm to 2140 nm) can be achieved by varying the number of Bosch process cycles. The diameter of the Ge nanowire arrays can be controlled from 220 nm to 30 nm by wet chemical etching at room temperature using H_2O_2 solution. Ge/p-Si core-shell nanowire arrays are successfully fabricated by forming a p-Si shell layer on Ge nanowires using a CVD method. The accumulation of hole gas in Ge cores is demonstrated by Raman scattering analysis, and a small core size results in an increased hole gas concentration. The results presented here show the potential for its applications in next-generation vertical high-speed HEMT-type FETs.

Experimental

Fabrication of photoresist nanohole arrays

Prior to the nanoimprint lithography, an excimer UV irradiation system (Multiply EXC-1201) was used to clean the p-Ge(100) wafers at 110 °C for 5 min. Next, the wafers were spin-coated with UV curable imprint photoresist (NIAC70920-DSN2) at 3000 rpm for 40 s. After pre-baking at 70 °C for 20 s, a quartz mold with periodic nanopillars of pitch size 500 nm or 600 nm was brought into contact with the photoresist layer at a pressure of 3.05 kN, followed by UV light irradiation. This process was performed using a nanoimprint system (Toshiba Machine ST50).

After the quartz mold was removed, the cured photoresist was baked again at 70 °C for 5 min. The thickness of the residual photoresist layer in the nanoholes was measured by SEM using a cross-sectional view. Next, the photoresist in the nanoholes was then removed by a capacitively coupled plasma reactive ion etching (CCP-RIE) system (SAMCO RIE-200NL) using O_2 plasma (O_2 : 5 sccm, N_2 : 5 sccm, process pressure: 0.1 Pa). The radiofrequency inductively coupled plasma (RF ICP) was set to 20 W with a bias of 100 W. The dry etching time was 3–8 min for the thickness of the residual layer until the Ge surface was exposed.

Fabrication of Ge nanowire arrays

MgO (30 nm) was deposited on imprinted photoresist nanohole arrays using an electron beam evaporator (R-DEC RDEB-1206K). The resist was then removed by sonication with N-Methyl-2-pyrrolidone (NMP) at 80 °C for one hour and without sonication for one hour, followed by washing with acetone and IPA. Next, a deep etching process (Bosch process) was performed by applying SF_6 plasma (anisotropic etching) followed by C_4F_8 plasma (passivation film deposition) using a Si deep etcher (Sumitomo Precision Products MUC-21 ASE-SRE). Both SF_6 and C_4F_8 flow rates were fixed at 35 sccm, the chamber pressure was 0.75 Pa, and the RF power was 100W. The number of Bosch cycles was set between 15 and 60 to adjust for the length of nanowire arrays. Finally, the MgO mask was removed by H_3PO_4 solution (DI-water: 97 ml, H_3PO_4 : 3 ml) for 30 s at room temperature, followed by plasma ashing (>100 °C) to remove organic contaminants.

To reduce the size of the nanowires, the samples were first immersed in DI-water for 30 s to roughly remove native oxide, and then immersed in H_2O_2 ($\text{H}_2\text{O}_2/\text{H}_2\text{O}$: 1/10) solution for 0 to 240 s at room temperature. The nanowires were then washed with DI water and their morphology was characterized by SEM.

Fabrication of Ge/Si core–shell nanowire arrays.

First, Ge nanowire arrays of two different diameters (220 nm and 70 nm) were fabricated by H₂O₂ etching at different times. These samples were immersed in HCl solution for 10 s at room temperature to roughly remove native oxides and then loaded into a chemical vapor deposition (CVD) chamber at a background pressure of 2×10^{-6} Pa. After pre-annealing at 800 °C in vacuum for 10 min, boron-doped Si shell growth was performed at 700 °C for 2 min using 19 sccm SiH₄ (100%) and 0.5 sccm B₂H₆ (1% in H₂) as precursor gases. The total pressure for shell deposition was set at 700 Pa by mixing with nitrogen gas. After the shell formation, the samples were post-annealed at 800 °C for 10 min to activate the dopant in the Si shell.

Sample characterization

A Hitachi S-8000 (Tokyo, Japan) scanning electron microscopy (SEM) with an acceleration voltage of 10 kV was used to evaluate the morphology of nanowires. A micro-Raman scattering system from Photon Design (Tokyo, Japan) was used to study the hole gas accumulation and stress in nanowires. The power of the excitation light (532-nm) with a 100× objective lens was set to 0.02 mW to prevent local heating.^{34,35}

Author Contributions

Conceptualization, N.F.; methodology, Y.-L.S. and N.F.; validation, Y.-L.S. and N.F.; formal analysis, Y.-L.S. and N.F.; investigation, Y.-L.S. and W.J.; resources, W.J. and N.F.; data curation, Y.-L.S.; writing—original draft preparation, Y.-L.S.; writing—review and editing, N.F.; visualization, Y.-L.S.; supervision, N.F.; project administration, N.F.; funding acquisition, N.F. All authors have read and agreed to the published version of the manuscript.

Conflicts of interest

There are no conflicts to declare.

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