Synthesis of Submillimeter-Scale Laterally-Grown Germanium Monosulfide Thin Films and their Electro-Optic Applications

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ABSTRACT

Layered two-dimensional Group IV monochalcogenide semiconductors, a novel group of functional materials, are a focus of growing research interest. Numerous reports on germanium monosulfide (GeS) provide evidence of its advanced properties that gives it potential for application to electronics and optoelectronics. However, currently synthesized GeS tends to be patchy and discontinuous. In this study, a novel method that takes Mullins-Sekerka instability into account is proposed to grow continuous GeS thin films. By applying a pre-deposited amorphous GeS layer, submillimeter-scale laterally-grown GeS thin films with single domain areas of 800 μm in size and 100 nm in thickness are successfully achieved. Field-effect transistor (FET) arrays with GeS thin films directly grown on a SiO_2/Si substrate at a growth temperature of 420 °C and isolated GeS channel patterns are fabricated for the first time and showing clear gate voltage-dependent current-voltage (I-V) characteristics. We also obtained the hysteresis response of the I-V characteristics, which exhibit notably

restrained behavior under light illumination. The successful synthesis of submillimeter-scale laterally-grown GeS thin films and the fabrication of GeS FET arrays should unlock the significant potential of GeS for use as key functional material in the development of next-generation electronic and optoelectronic applications, such as full-light controlled computing-in-memory devices and sensors.

KEYWORDS Lateral growth, germanium monosulfide, two-dimensional layered semiconductors, field effect transistors, optoelectronics, hysteresis

1. INTRODUCTION

The discovery of free-standing graphene has triggered the development of a wide range of functional devices that use two-dimensional (2D) layered materials [1,2,3,4,5], such as twist-angle Moiré pattern-induced superconductivity [6,7], synaptic transistors [8,9], and terahertz emitters [10, 11]. However, the gapless nature of graphene impedes its use as a key channel material for high-performance next-generation semiconductor devices [12]. After having achieved centimeter-scale synthesis of graphene on a metal-catalyst substrate [13], researchers are endeavoring to give graphene semiconducting properties by top-down nanoribbon fabrication, bottom-up synthesis, and other processes [14]. Although defect management and orientation control are time-consuming processes, they are key challenges in developing nanoribbons for use in practical devices on an industrial level [15]. The successful synthesis of transition metal chalcogenides (TMDs), e.g., molybdenum disulfide (MoS_2), is also prompting progress in the creation of layered semiconductor materials of atomic-layer thickness [16]. Orientation control of TMDs using substrate-growing engineering at the wafer-scale level suggests their considerable potential for mass production of applications beyond Moore's Law [17]. The centrosymmetric structure of TMDs can also be readily modulated using the Janus structure and van der Waals (vdW) stacking for the development of functional semiconducting devices [18,19]. However, the high growth temperature of about 650 - 700 °C needed to obtain good crystallinity of TMDs using salt-assisted techniques still hinders the further integration of practical applications into current semiconductor manufacturing industrial processes [20,21]. TMDs synthesized at low temperatures using atomic layer deposition reveal the barriers to achieving good crystallinity [22,

[23]. In addition to the requirement for high crystallization temperature, the phase control of another group of functional semiconductors, such as the ferroelectric 2D material In_2Se_3, is another key challenge [24].

Of the aforementioned related materials, the rediscovery of pnictogen analogues as a new group of functional semiconductors, including Group IV monochalcogenides, highlights the significant potential for the development of novel applications owing to the lower thermal budget required for crystallization than for TMDs [25]. Germanium monosulfide (GeS), a typical Group IV monochalcogenide, is increasingly being investigated for its unique properties of comprising non-toxic earth-abundant compounds and its puckered atomic structure [26], bandgap of 1.6 eV [27], high Curie temperature of 6400 K [28], Eshelby twist [29], in-plane ferroelectricity [30], photostrictive properties [31] and so forth [32,33]. GeS nanowires [34], nanosheets [35], and nanoflakes [36] have been synthesized by chemical vapor deposition (CVD) [37], physical vapor deposition (PVD) [38], and colloidal synthesis [39]. Moreover, tin monosulfide (SnS), which has an analogous atomic structure, has been provided throughout the PVD [40], CVD [41], or MBE [42]. Synthesized GeS and SnS show that the crystallized adatoms are likely prior to the surface of the grown layer rather than showing lateral growth behavior owing to the lone-pair feature of the structure [43]. The result is discontinuously-grown flakes and facilely thicker crystallized prisms, even in the areas of single crystals that reach several micrometers in size. Previous studies have shown amorphous GeS to be a promising functional material [32, 44], whereas the synthesis of large-area continuous crystallized thin films remains a challenge.

To this end, a novel method with the assistance of a pre-deposited amorphous GeS layer is proposed to synthesize submillimeter-scale GeS thin films. Laterally crystalline behaviors of GeS are confirmed at a growth temperature of 420 °C. Submillimeter-scale GeS thin films with a single domain area of 800 μm in size are successfully attained with no limitation from the boundary layer diffusion effect at the edge of the substrate [45]. This proposed method for the direct growth of GeS thin films on the target substrate, namely no requirement for the assistance of a metal catalyst for the growth process or the subsequent dry or wet transfer process, may in addition effectively exclude unwanted impurities and defects, enabling these thin films to be used in high-performance applications [5,13,17,29]. Back-gated GeS field-effect transistor (FET) arrays are fabricated following the direct growth process. Clear gate voltage-dependent current-

voltage (I-V) characteristics are observed. Analogous to previous investigations, I-V hysteresis is successfully demonstrated, which is attributed to the in-plane ferroelectricity of Group IV monochalcogenides [30,40]. The light-induced restrained hysteresis of the I-V characteristics is also observed for fabricated GeS-FETs. This is likely due to the photostrictive relaxation [31,46] of the in-plane net polarization among the van der Waals stacked layers [30,40]. Ideally, laterally-grown GeS is anticipated to successfully result in wafer-scale single-crystal GeS thin films with the synergy of substrate engineering, analogous to other 2D materials. Group IV monochalcogenide layered semiconductors are promising 2D layered functional materials and show significant potential for the development of next-generation electronic and optoelectronic applications.

2. RESULTS AND DISCUSSION

To achieve submillimeter-scale continuous GeS thin films, a novel method using the assistance of pre-deposited amorphous GeS layer is proposed herein. The synthesis of GeS thin films is conducted by using a physical vapor transport system with two independent heating zones. Figure 1 (a) shows the heating profile as illustrated by Zone 1 and Zone 2. Figure 1 (b) shows the schematics for different processes of pre-deposition of GeS and growth of GeS, correspondingly numbered #2 and #3. The temperature of Zone 1 (T_c1) is raised to 440 °C 20 min prior to that in Zone 2. Since the temperature of Zone 2 (T_c2) is well below the crystallization temperature, only amorphous GeS is deposited on the substrate. The temperature of T_c2 is then increased to 420 °C to provide a sufficient thermal budget for the initialization of the nucleation and crystallization processes with the assistance of the pre-deposited amorphous GeS films, as indicated by the #3 process in Figure 1 (a) - (b). After the growth process, the quartz tube is allowed to cool down to room temperature. Cross-section scanning electron microscopy (SEM) images of processes #2 and #3 are shown in the upper and lower insets of Figure 1 (c), respectively. Here, the targeted Si substrates with a 100-nm-thick thermally oxidized layer are utilized for the growth processes. After the pre-deposition process with a growth time (t_g) of 0 min, a flat layer with a total thickness of about 200 nm is observed by SEM. Since the imaging contrast between the deposited GeS layer and the natural SiO_2 layer shows no

significant difference for the overall 200 nm-thick layer, the upper 100 nm-thick layer is concluded to consist of amorphous GeS. On the other hand, a clear imaging contrast with growth time (t_g) of 50 min is obtained from the lower SEM image. The silvery color of the top 100 nm-thick layer is akin to that of the Si substrate, indicating that the GeS films appear to have crystallized after the growth process.

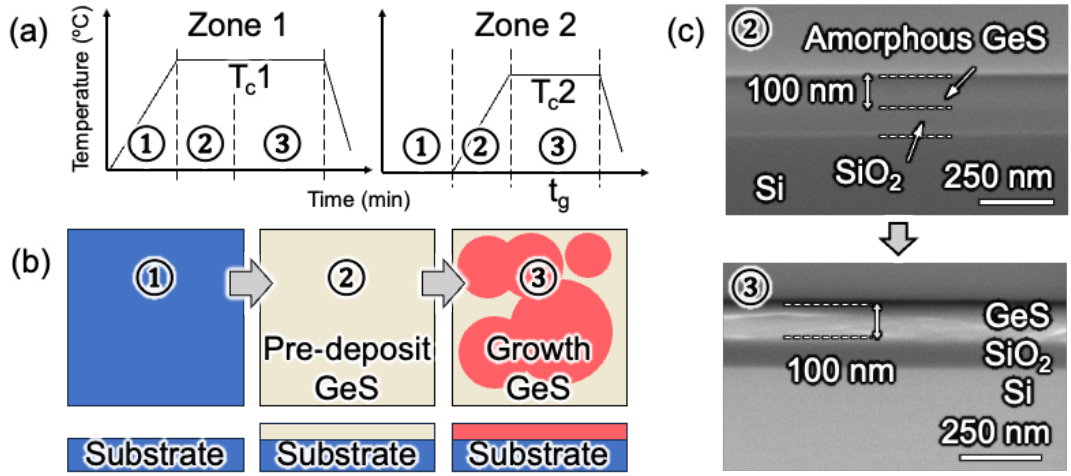

Figure 1. (a) Heating profile of the two zones for growth of submillimeter-scale continuous GeS thin films. **(b)** Schematic images of top and section views for individual processes, #1 for heating up, #2 for pre-deposited amorphous GeS, and #3 for grown GeS, corresponding to (a), respectively. **(c)** Sectional views of SEM images for the corresponding processes of #2 and #3, respectively.

To further evaluate the growth behaviors of the synthesized GeS, the time-dependent growth processes are investigated, as shown in Figure 2. SEM images with t_g values of 20, 35, and 50 min are shown in Figure 2 (a) - (c), respectively. At a t_g of 20 min, it shows a small clustering feature. When the t_g is increased to 35 min, a circular feature is observed. Eventually, for a t_g of 50 min, a circular feature with a diameter of about 800 μm is confirmed. The Raman spectra measured at different positions of the submillimeter-scale single domain are shown in Figure 2 (d). The black line is the Raman signal of the #1 spot pointed at the center of the domain. It shows the three typical Raman phonon modes for GeS [47] as indicated by B_{3g} at 211 cm^{-1}, indicating the zigzag edge direction vibration mode, A_g, at 239 cm^{-1}, indicating the layer breathing mode, and A_g at 269 cm^{-1}, indicating the armchair edge direction vibration mode,

respectively. However, an unknown peak at around 308 cm^{-1} is obtained in addition to that at the #1 spot. It is likely attributable to the incorporation of impurities with smaller atomic radius, such as Si or O or GeS_x ($x > 1$), during the initial nucleation process of GeS. The three typical clean vibration modes of GeS without the unknown signals are obtained at spots #2 and #3. The Raman signal at 521 cm^{-1} corresponds to the Si substrate. Thus, the lateral crystallization of GeS films is validated by the area-dependent Raman spectra. The circular periphery of the domain at spot #3 exhibits a dendrite-like diffusion pattern with a lower intensity of Raman signals than those at spot #2. Supersaturation likely occurs at the interface between the re-sublimated portion of the pre-deposited amorphous GeS layer and the GeS vapor from the source. This facilitates the condensation of the GeS vapor into a dendrite-like crystalline GeS film [48,49]. A high precursor concentration interface parallel to the surface of the substrate and a concentration gradient normal to the surface of the substrate are likely formed simultaneously and promote the lateral growth of the GeS, due to the possible mechanism termed Mullins-Sekerka instability [50,51,52]. This is not limited to the growth of GeS thin films described here. In previous studies, analogous features exhibiting the circular domain of the synthesized two-dimensional materials for the rapid growth of graphene and In_2Se_3 have also been demonstrated [53,54]. The X-ray diffraction (XRD) results confirm the orthorhombic structure of GeS, in accordance with the standard GeS reference of the PDF#00-009-0231, as shown in Figure 2 (e), highlighted by the blue line. In the 2θ scan mode, only the diffraction peaks located at about 34.2° for (004) and 16.9° for (002) are observed, indicating that the crystal orientation matches well with the c-axis, which is normal to the van der Waals stacking layers. It suggests that GeS thin films, which are directly grown on SiO_2/Si substrates using the pre-deposited amorphous GeS method, consist of layered structures.

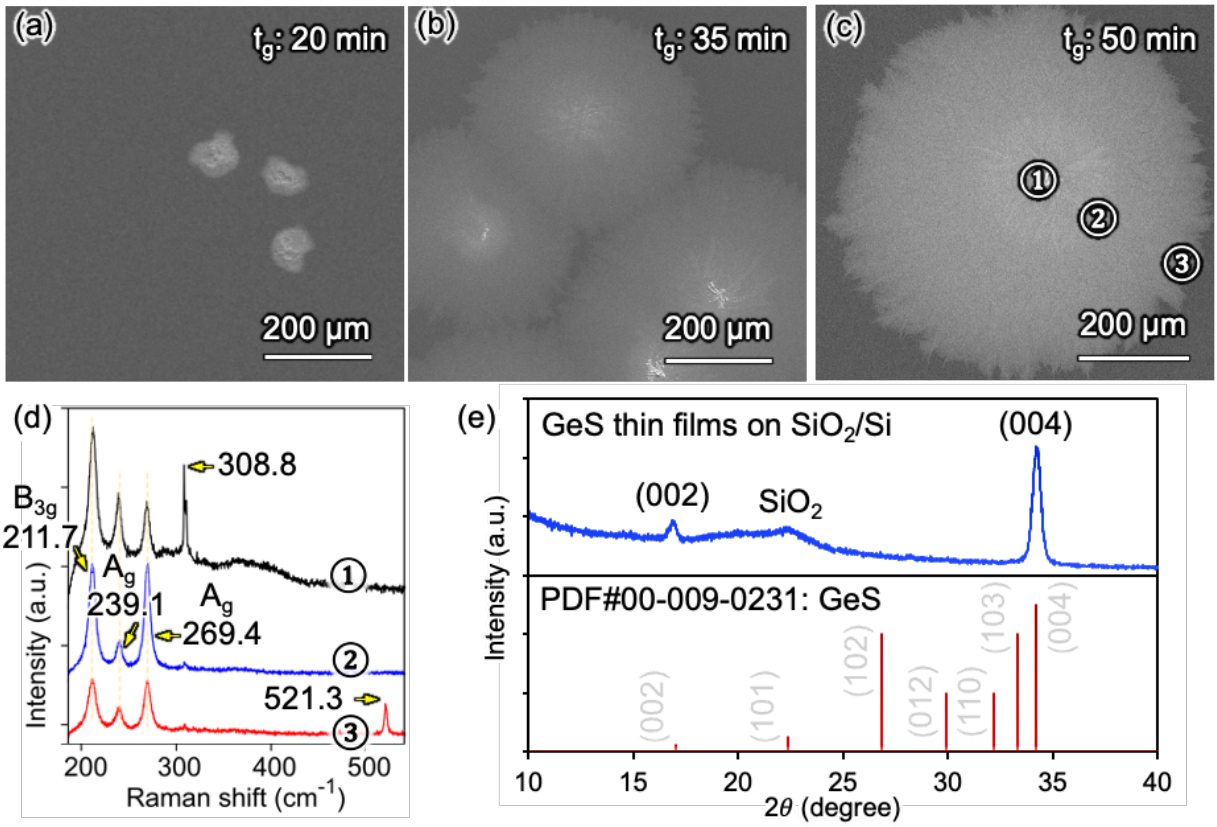

Figure 2. SEM images for the observation of lateral growth features of GeS during growth times t_g of **(a)** 20 min, **(b)** 35 min, **(c)** 50 min, respectively; **(d)** Raman spectra of spots #1 to #3 measured in (c) from the center to the periphery of the circle domain; **(e)** XRD spectrum of the GeS thin films directly grown on a SiO_2/Si substrate and the standard GeS reference of the PDF#00-009-0231.

To clarify the atomic structure and the single-crystallized area of the grown GeS synthesized using the pre-deposited amorphous GeS layer method, the evaluation of crystallinity is investigated using transmission electron microscopy (TEM) as shown in Figure 3. The as-grown GeS on the 100-nm SiO_2 layer is immersed in hydrofluoric acid solution to dissolve the SiO_2 layer. The etched substrates with GeS are then transferred to another beaker filled with deionized (DI) water. The surface tension of the DI water is strong enough to instantly delaminate the GeS films from the Si substrate; they then float on the DI water. An amorphous carbon-enhanced copper microgrid is then utilized as the support for the transferred GeS films for TEM observations. The high-angle annular dark field scanning TEM (HADDF-STEM) images corresponding to energy-dispersive X-ray detector (EDX) color mappings are shown in

Figure 3 (a). The venation-like contrastive colors in the HADDF image are likely ascribable to the dendrite-like structure of the grown GeS films or the ripple structure introduced during the wet transfer process. The EDX images of pictured GeS film show the presence of the element components of Ge and S. To rapidly identify the size of the single-crystal GeS, selected-area electron diffraction (SAED) is utilized with the pre-identified area of observation shown in Figure 3 (b). The insets from left to right are SAED patterns with diameters of aperture of 200 nm, 800 nm, 4 μm, and 16 μm, respectively. GeS films tend to adopt a single-crystalline structure that is 200 nm in size. Separate individual SAED patterns with three rotated points are also observed for the aperture diameter of 800 nm, likely due to the different orientation of the GeS stitched at the grain boundary or the ripple structure resulting from the wet transfer process. At diameters of 4 and 16 μm, the SAED patterns show circular rotation features indicating the polycrystalline features of the synthesized GeS. High-resolution TEM (HRTEM) images show the lattice fringe of the synthesized GeS, which clearly exhibits an orthorhombic structure with a zigzag (along *a*) and the armchair (along *b*) edge directions with the vdW stacking direction along the *c* axis, as illustrated in Figure 3 (c) [38]. The fast Fourier transform (FFT) pattern of the observed area is shown in the inset on the right-hand side, confirming the crystallization of the synthesized GeS. Since identification of grain boundaries is difficult, expensive, and out of the scope of this study, single-crystalline areas of GeS conceivably exceeding 200 nm in size were confirmed owing to the aperture limitations of TEM.

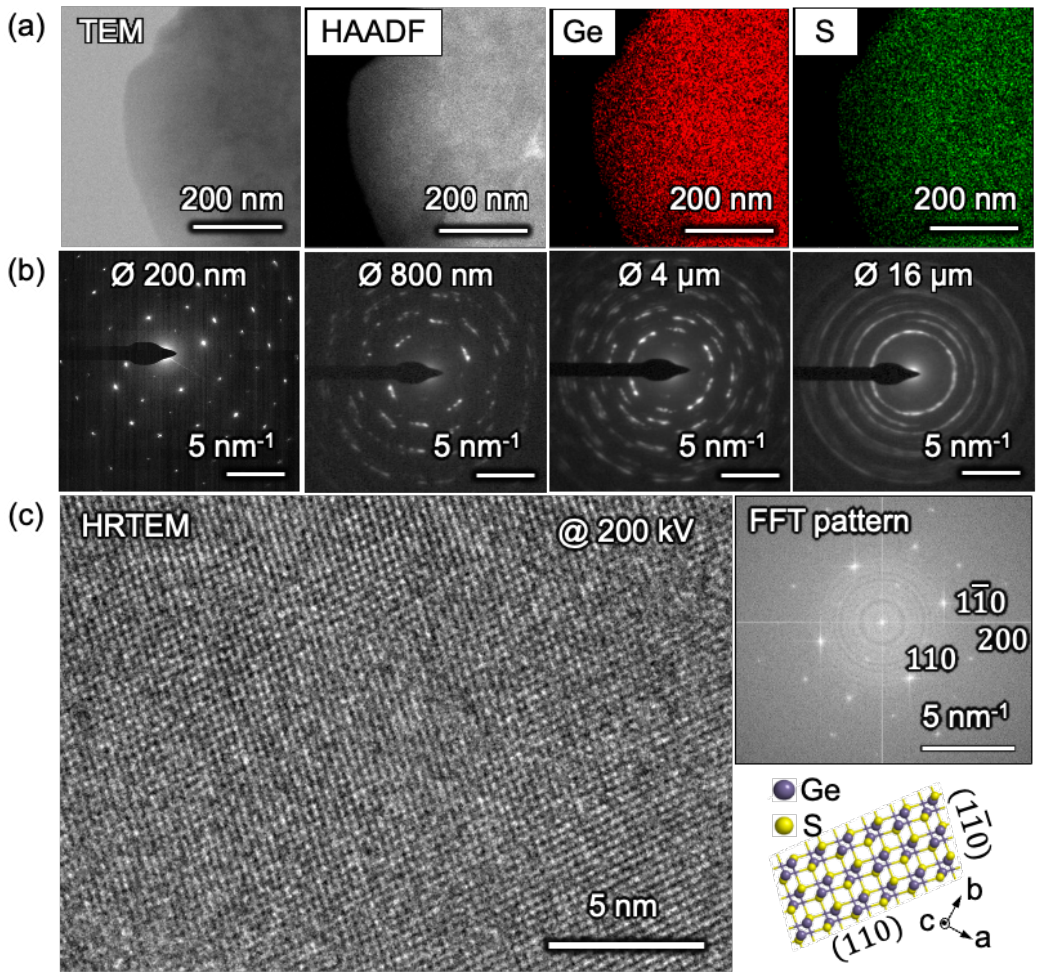

Figure 3. (a) TEM and HAADF images, EDX element mappings of the transferred GeS film. **(b)** SAED patterns of the transferred GeS film with aperture diameters of about 200 nm, 800 nm, 4 μm, and 16 μm. **(c)** High-resolution TEM image of the lattice fringe of the transferred GeS film observed at 200 kV with its FFT pattern, and a schematic image of the corresponding atomic structure of GeS.

Herein, back-gate GeS field-effect transistor (FET) arrays are fabricated on a highly doped p-type Si substrate with a 300-nm SiO_2 layer, adopting the direct growth process of GeS thin films. The device structure and the optical images of fabricated GeS FETs are illustrated in Figure 4 (a). To fabricate the GeS FETs, the same recipe as in the previous sections is applied for preparing the channel GeS thin films. The standard micro-electromechanical systems (MEMS) process with common photoresist recipes is utilized to fabricate GeS FET arrays (See Experimental Methods for details). Before the direct growth of GeS, the target substrate is

cleaned using the same procedure as described in the previous sections. The grown GeS is then isolated for the channel using laser lithography as illustrated in the highlighted dashed square. Capacitively-coupled plasma (CCP) reactive ion etching (RIE) is applied to dry-etch the unwanted GeS using SF_6 mixed with Ar. The dark navy color indicates the etched GeS area. Certain as-grown GeS areas remain on the substrate, as identified by the yellow arrow. The yellow patterns are the metal electrodes of Ti/Au deposited using an electron beam (EB) evaporation system. Figure 4 shows the current-voltage (I-V) characteristics of the fabricated GeS FETs and their demonstrations for the functional semiconductor devices. The channel length and width of the represented FET are 6 and 160 μm, respectively. The drain-source I-V (I_{ds}-V_{ds}) characteristics of the gate voltage (V_g), ranging from 60 to –60 V in decrements of 20 V, are shown in Figure 4 (b), highlighted in purple and red, respectively. The V_{ds} range is from –60 to 60 V. The measurements are conducted under dark conditions at room temperature (RT) maintained by a cooling system. When the applied gate voltage V_g falls from 60 to –60 V, the I_{ds} in the range of positive V_{ds} increases to a greater extent than in the negative V_{ds} range. It is interesting to observe this diode-like I_{ds}-V_{ds} characteristic. To understand this behavior, the effect of the remaining photoresist is first considered. However, there is no improvement of the I_{ds} in the range of negative V_{ds} after the isolated GeS patterns and fabricated FETs are thoroughly cleaned with *N*-methylpyrrolidinone (NMP). Tens of samples with hundreds of fabricated GeS FETs exhibit diode-like behaviors. The diode-like behaviors are therefore likely attributable to the sulfur-rich crystallized, amorphous, or glassy GeS synthesized during the cooling process [38]. A previous study claims that the GeS flakes synthesized using the vapor transport method exhibit a core-shell structure, with the GeS_x shell encapsulating the core, resulting in better chemical stability [38]. Since we are prone to focusing on the investigation of the I-V characteristics of the synthesized submillimeter-scale GeS thin films for use in functional semiconductor devices in this study, the further investigation of these diode-like behaviors will be carried on in our next work. Figure 4 (c) shows the V_g dependent I_{ds}-V_{ds} characteristics of the same GeS FET (i.e., channel length of 6 μm, channel width of 160 μm) under white light illumination. The clear enhancement of I_{ds} by approximately sevenfold is observed in the range of positive V_{ds}. Interestingly, the I_{ds} in the range of negative V_{ds} show a significant increase, likely due to the photo-generated carriers in both the crystallized GeS core and the amorphous GeS_x shell. The

photo-generated carriers may penetrate the barriers developed by the amorphous GeS_x shell, giving rise to the substantial observed increase of I_{ds} in the range of negative V_{ds}.

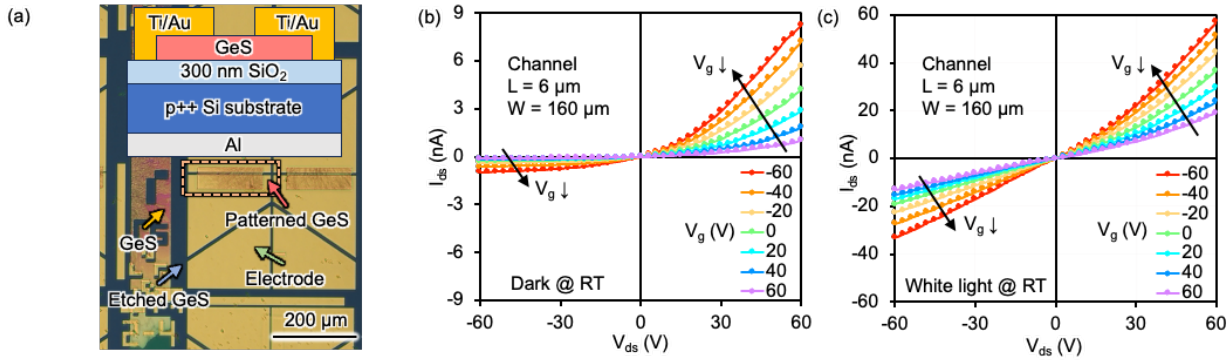

Figure 4. (a) Schematic image of the device structure and an optical image of the fabricated GeS FETs. **(b)** Output characteristics of the represented GeS FET with channel length of 6 μm and width of 160 μm measured in the dark and at room temperature. **(c)** Output characteristics of the represented GeS FET in (b) measured under white light illumination.

Figure 5 (a) shows the transfer characteristics over a range of V_g from –60 to 60 V and the applied V_{ds} of 60 V under dark conditions. All measurements are conducted at RT. A typical p-type conducting behavior with a clear hysteresis response of I_{ds} is obtained for the fabricated GeS FET. The obtained dark on-current is about 9 nA at a V_{ds} of 60 V. The dark off-current should also be further improved down to the femto-ampere level at V_{ds} of 0 V in subsequent studies to achieve a higher on/off ratio for GeS FETs. The field-effect mobility is calculated using the equation $\mu = (dI_{ds}/dV_g)(L/C_iWV_{ds})$, where dI_{ds}/dV_g is the transconductance, L and W are the length and width of the channel, respectively; and C_i is the capacitance per unit area of the 300-nm SiO_2 layer. The obtained mobility of GeS FETs is about 1.4×10^{-5} cm^2/Vs. This is much lower than the mobility obtained using the first-principles calculation method and the van der Pauw method [56, 57], whereas it is close to the mobility of single-crystal GeS FET using the exfoliation method, with a similar order of magnitude [58]. This low mobility has been confirmed in ultrawide-bandgap semiconductor $MnPS_3$, $GaPS_4$ and hBN FETs [59,60,61]. A low mobility of about 10^{-5} is likely to be found in early ovonic threshold switch materials in their amorphous phase [62,63,44]. Alternatively, GeS is also likely suitable for low operating current devices with an intrinsic ovonic threshold switching function. The low mobility of the fabricated GeS FET is

likely not only ascribed to the suggested GeS_x shell, but also to numerous scattering centers owing to low crystallinity, damage caused during the fabrication processes of FETs, and roughness at the gate-channel interfaces. There is still considerable potential to raise the performance of GeS FETs in future studies.

It has been claimed that the hysteresis response is likely ascribed to the in-plane ferroelectricity of IV-VI compounds [30,40] and that it can be tuned electrostatically. The function V_g was therefore applied to further investigate the hysteresis response of the I_{ds}-V_{ds} characteristics shown in Figure 5 (b). Here, only the positive range of V_{ds} is selected to investigate the hysteresis response. Since the electrons are injected into the GeS channel, the hole current decreases at a positive V_g, as indicated by the blue and purple lines. The hysteresis response increases with rising p-doping level under the applied negative V_g, as indicated by the yellow and red lines. It is clear that the gate bias alters the ferroelectric polarization of the GeS channel. Analogous functions have been reported in SnS and In_2Se_3 planar devices [40,64]. Previous studies have suggested that the in-plane ferroelectricity is due to the lack of centrosymmetry in the stacking sequence [19,30,40,65]. However, the hysteresis response behavior is generally obtained with no significant difference among all the devices, demonstrating that the layer-dependent hysteresis response of the grown GeS is less marked in this study. The hysteresis response observed in the GeS FETs fabricated in this study is likely due to the strain-induced non-centrosymmetric stacking of GeS under the supersaturation-induced condensation process as affected by Mullins-Sekerka instability. A clear hysteresis response is also observed at the maximum V_{ds} range of 20 V as highlighted by the salmon color visible in Figure 5 (b). However, the absence of a coercive electric field is questionable in the light of other studies using exfoliated single-crystal GeS **[30]**. It is likely that a large number of defects and strains are introduced into the crystallized films during the growth process.

The hysteresis response of I_{ds}-V_{ds} characteristics was further investigated under light illumination as shown in Figure 5 (c), since the GeS FET exhibits photo-sensitive behaviors owing to its band gap of about 1.6 eV [27] as illustrated in Figure 4 (c). Of great interest is that the hysteresis response under light illumination (blue line) is restricted to a significantly narrower range than that measured under dark conditions (red line). Other than the light-induced thermal expansion in GeS channels, previous studies have stated that the ferroelectric Group IV

monochalcogenides exhibit an ultrafast optomechanical strain of about 0.1% with GeS owing to the photostrictive effect on the puckered atomic structures [28,31,46,66,67]. The significantly restrained hysteresis response observed here may be confidently attributed to the relaxation of the strained structure into the centrosymmetric stacking sequence. In addition to the photostrictive effect, defects resulting in heavy charge trapping centers may also contribute to the hysteresis response. However, previous studies have stated that light illumination yields an enhanced hysteresis response [68], which contradicts our observed results, whereas ferroelectric materials exhibit a restrained hysteresis response [69]. Observations of the relationship between hysteresis response and light illumination have prompted us to investigate, in our next investigation, the photostrictive effect on in-plane ferroelectricity. Overall, the growth behaviors of GeS thin films and the fabricated GeS FETs demonstrated in this study show significant potential for the development of next-generation electronic and optoelectronic applications using 2D-layered Group IV monochalcogenides as key functional semiconductors.

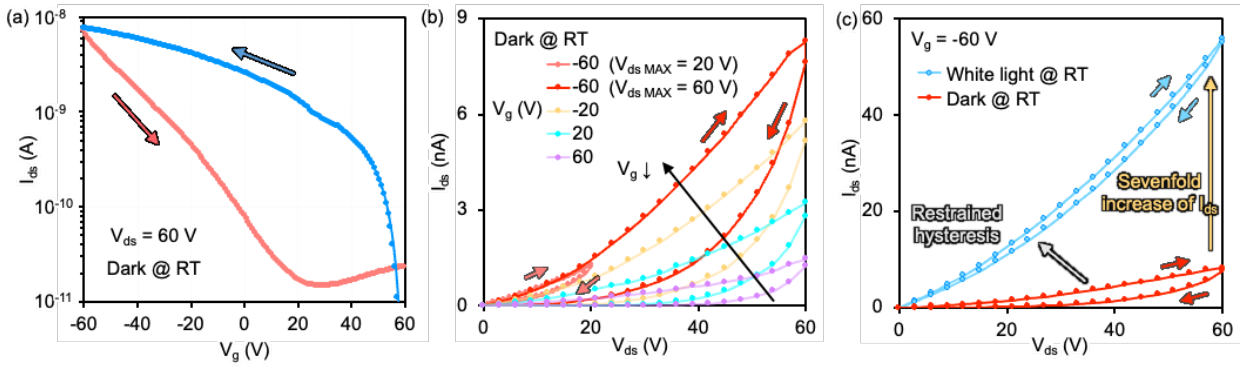

Figure 5. (a) Transfer characteristics, **(b)** hysteresis response, and **(c)** the effect of light illumination on the hysteresis response of the GeS FET shown in Figure 4.

3. CONCLUSIONS

In this study, we are the first to experimentally demonstrate the lateral growth of the submillimeter-scale GeS thin films with the single domain size of 800 μm and the thickness of about 100 nm, fabrication of GeS FET arrays with the isolated GeS channels, and the light-induced hysteresis responses of fabricated GeS FETs. The single-domain area of GeS thin films being on the approximately submillimeter-scale is the clear positive point for the fabrication of

next-generation transistors. With the lateral growth behavior of GeS thin films, patterning the pre-deposited amorphous GeS makes it possible to attain the selective growth of single domains of GeS within distinct and pre-defined areas to create channels in transistors. The directly-grown GeS on a SiO_2/Si substrate exhibits a significant advantage that there is no requirement for the transfer processes (including exfoliation) from as-grown substrates comparing to that of other 2D layered materials. A low thermal budget of about 420 °C to obtain the single-crystalline area larger than 200 nm in size and the one crystal orientation on a SiO_2/Si substrate shows the major superiority of GeS among other 2D layered functional semiconductors. A brief comparison of relevant parameters of the grown GeS with other 2D layered materials is shown in Table 1. Fabricated GeS FET arrays clearly show gate voltage-dependent current-voltage characteristics, whereas the mobility is only about 1.4×10^{-5} cm^2/Vs. Although this is much lower than the mobility obtained by first-principles calculations [56] and the van der Pauw method [57], it still exhibits a similar order of magnitude to that of GeS FETs using exfoliated single-crystal GeS that have a limited area [58]. The low mobility is analogous to that of FETs using ultra-wide bandgap semiconductor material [59,60,61] as listed in Table 1. Therefore, a thin GeS_x layer, developed using the vapor transport method [38], likely exhibits a significant effect on the behaviors and properties of the fabricated FETs. In addition to their low mobility, the fabricated GeS FETs exhibit clear gate-dependent hysteresis responses, with the magnitude of their hysteresis behavior subject to modulation by illumination with light. One assumption regarding the restrained hysteresis behavior is that of the photostrictive effect in ferroelectric Group IV monochalcogenides [31,46,66,67,68,69]. The gate-dependent I-V characteristics and light-induced changes in hysteresis behaviors observed in this investigation reveal significant potential for GeS to be applied as a key channel material for next-generation electronic and optoelectronic devices, such as full-light controlled in-memory computing applications and sensors. Moreover, with the advantage of the proposed method for synthesizing submillimeter-scale GeS thin films, success in fabricating GeS FET arrays provides a good starting point for the research and development of 2D layered Group IV monochalcogenides as major functional semiconductors on the industrial level.

Table 1. Comparison of relevant parameters of GeS with other 2D layered materials.

Ref.	Materials	Crystalline size	Thickness	Method	Substrate	Mobility type	Mobility (cm^2/Vs)
This study	**GeS**	**800~ μm (lateral growth)**	**100~ nm**	**PVD**	**SiO_2/Si**	**Field-effect mobility**	**1.4×10^{-5} (RT)**
45	GeS	~10 μm (vertical growth limited at edge)	30~50 nm	PVD	SiO_2/Si	N/A	N/A
37	GeS	~7.5 mm (growth) & 13~ μm (device)	500 μm (growth) & 28 nm (device)	CVT (growth) & exfoliation	SiO_2/Si	Field-effect mobility	1.5×10^{-3} (RT)
58	GeS	~10 μm	60 & 120 nm	Exfoliation	SiO_2/Si	Field-effect mobility	4×10^{-5} (300 K)
57	GeS	~2 cm (growth) & 5 mm (evaluation)	1 cm (growth) & 300 μm (cleaved)	CVT (growth) & cleaved	N/A	Hall mobility	25 (300 K)
44	GeS	Amorphous	10 nm	Sputter	SiO_2	N/A	N/A
56	GeS	N/A	Monolayer	DFT (simulation)	N/A	N/A	3680 (0 K)
59	$MnPS_3$	~100 μm (growth) & ~10 μm (device)	1.2~110 nm (device)	CVT (growth) & exfoliation	SiO_2/Si	Field-effect mobility	$\sim8.3\times10^{-3}$ (RT)
60	$GaPS_4$	~5 mm (growth) & ~200 μm (device)	1.1~109 nm (device)	CVT (growth) & exfoliation	SiO_2/Si	Field-effect mobility	4.1×10^{-6} (RT)
61	hBN	1~ cm	Single layer (1.33 nm)	CVD & transfer	Copper	Field-effect mobility	$\sim10^{-2}$ (RT)
62	a-As_2Se_3/ a-$Ge_{0.03}Se_{0.97}$	N/A	N/A	Calculation	N/A	N/A	10^{-5}~10^{-2} (RT)
1	Graphene	10~100 μm	Single~few atomic layers	Exfoliation	SiO_2/Si	Field-effect mobility	~10,000 (300 K)
13	Graphene	1~ cm	Single layer	CVD & transfer	Copper	Field-effect mobility	~4,050 (RT)
53	Graphene	~300 μm	N/A	CVD & transfer	Copper	Hall mobility	~6,500 (1.4 K)
2	MoS_2	~10 μm	Single layer	Exfoliation	SiO_2/Si	Field-effect mobility	200 (RT)
3	WS_2	~10 μm (device)	Single layer	CVT (growth) & exfoliation	SiO_2/Si	Field-effect mobility	~57 (RT) ~140 (83 K)
4	$MoTe_2$	~10 μm	2~4 layers	Exfoliation	SiO_2/Si	Field-effect mobility	~0.3 (300 K)
16	MoS_2	1~ cm	Trilayer (2 nm)	CVD & transfer	Sapphire & SiO_2/Si	Field-effect mobility	~6 (RT)
24	In_2Se_3	~10 μm	2~16 nm	CVD & transfer	Mica	N/A	N/A
54	In_2Se_3	1~ cm	1~10 layers	CVD & transfer	Mica	Field-effect mobility	5 (RT)
64	In_2Se_3	~5 μm	25~95 nm	Exfoliation	Silica & gold	N/A	N/A
5	Black phosphorus	10 μm~2 cm	2.3~598.7 nm	CVD	SiO_2/Si	Field-effect mobility	~800 (300 K)
40	SnS	~10 μm	3~36 nm	PVD	Mica	N/A	N/A
55	SnS	~5 cm	190~260 nm	Sputter	SiO_2 glass	Hall mobility	0.1~1 (RT)

4. EXPERIMENTAL METHODS

A quartz tube furnace with two independent heating zones, named Zone 1 and Zone 2, is utilized to synthesize the submillimeter-scale single domain GeS thin films. Approximately 20 mg of GeS powder, the source material, is loaded in the quartz boat located in Zone 1. The target Si substrate, with a 100-nm oxide layer, is cleaned by sonication in acetone for 15 min, then by the multiple-time rinses in isopropyl alcohol (IPA), and deionized (DI) water, and finally by cleaning in Piranha solution with a 3 : 1 mixture of sulfuric acid and hydrogen peroxide for 15 min, followed by the multiple-time rinses. The substrate is then immersed in 1.5% diluted HF solution for 1 min to clean the surface oxide, followed by the multiple-time rinses. The substrate is placed in the quartz tube and the quartz tube is evacuated to 0.015 Pa, followed by the supply of high-purity Ar carrier gas to reach the base pressure of 90 Pa by adjusting the needle valve in the gas feed-in line. Fluxed Ar gas for cleaning the growth environment of the quartz tube is maintained for at least 10 min. The growth temperature of T_c1 is increased to 440 °C, and T_c2 is increased to 420 °C 20 min later. The growth pressure is then maintained at around 6500 Pa by adjusting the vacuum valve in the exhaust line. After the growth process, the quartz tube is cooling down naturally. Characterization of the grown GeS on the SiO_2/Si substrate is conducted using Raman microscopy. These observations are conducted at an excitation wavelength of 532 nm with a laser strength of about 20 μW to prevent any damage to the crystallized GeS. The XRD data is collected using a PANalytical X'Pert PRO MRD X-ray diffractometer (XRD) with a Cu Kα source, in the range of 2θ from 10° to 40° with a step of 0.01°. The morphology of the GeS is investigated using transmission electron microscopy (TEM) and selected area electron diffraction in an FEI Talos F200X field emission microscope operated at 200 kV with an EDX detector.

For the fabrication of GeS FET arrays, highly boron-doped p-type Si substrates (0.001 - 0.005 Ω·cm) with a 300-nm thermally oxidized layer are applied. The substrate cleaning follows the same procedures, using acetone, IPA, to Piranha and HF solutions. After the main growth process, the grown GeS is isolated for the channel material using laser lithography (DL-1000) at an exposure power of 90 mJ/cm^2 with an AZ5214E photoresist (spin coating at 5000 rpm for 60

sec, pre-bake at 110 °C for 2 min). Instead of using hexamethyldisilazane (HMDS) to increase the adhesive force between the photoresists and GeS, rapid heating, namely dry bake, using a hotplate at 120 ˚C for 1 min is applied to remove the adsorbed water on the surface of the GeS films. Omitting this rapid heating or applied HMDS results in significantly problematic patterning of the photoresist after the developing process. A standard solution of tetramethylammonium hydroxide-2.38% (TMAH-2.38%) is applied to develop AZ5214E for 90 sec, followed by two times of resins in DI water for 60 sec each and N_2 gun blow for drying. CCP-RIE is applied to dry-etch the unwanted GeS for 90 sec using SF_6 at 10 sccm and Ar at 30 sccm at an RF power of 35 W and chamber pressure of 10 Pa. After the etching process, the patterned AZ5214E is removed with *N*-methylpyrrolidinone (NMP) as the standard lift-off process. The drain and source electrodes (0.5 nm Ti/120 nm Au) are then formed by laser lithography at an exposure power of 100 mJ/cm^2 and electron beam (EB) evaporator. The titanium used here is solely to increase the adhesive force between GeS and Au for the subsequent lift-off process while providing ohmic-like contacts for p-type GeS. A double layer resist of PMGI SF6 (spin coating at 5000 rpm for 60 sec, pre-bake at 180 °C for 3 min)/OFPR-800 LB (spin coating at 5000 rpm for 60 sec, pre-bake at 90 °C for 3 min) is applied and its developing process uses TMAH-2.38% for 60 sec, two times of DI water resins for 60 sec each, and N_2 gun blow for drying. The applied double layer resist here is subject to a problem when AZ5214E photoresist is used, which may result from the heat applied during the EB evaporation: difficulties in removing AZ5214E persist for several hours, even after the NMP lift-off process. Next, the electrode patterns are developed using a lift-off process employing NMP and cleaning sequentially in acetone, IPA, and DI water. After the electrode formation and lift-off processes, samples are baked at 180 °C for 5 min to achieve a better contact between metal electrodes and GeS thin films. Eventually, the current-voltage characteristics are measured using a Nagase semi-auto prober station and an Agilent Technologies Keysight 4156C under a vacuum of 10^{-3} Pa. The measuring stage is maintained at room temperature by means of a cooling system.

ACKNOWLEDGMENTS

This work is supported by JSPS Kakenhi (Grants no. JP20K14796 and JP23K13370). Part of this work is also supported by the Advanced Research Infrastructure for Materials and Nanotechnology in Japan (ARIM), MEXT, Japan, proposal number 23NM5171 and 24UT1037.

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