Supplementary Information

Physical Reservoir Computing with Graphene-based Solid Electric Double Layer Transistor and the Information Processing Capacity Analysis

Hina Kitano[1,2], Daiki Nishioka[1,3], Kazuya Terabe[1], and Takashi Tsuchiya[1,2*]

[1]Research Center for Materials Nanoarchitectonics (MANA), National Institute for Materials Science (NIMS), 1-1 Namiki, Tsukuba, Ibaraki, 305-0044, Japan.
[2]Department of Applied Physics, Faculty of Advanced Engineering, Tokyo University of Science, Katsushika, Tokyo 125-8585, Japan
[3]International Center for Young Scientists (ICYS), NIMS, 1-1 Namiki, Tsukuba, Ibaraki, 305-0044, Japan.

*E-mail: TSUCHIYA.Takashi@nims.go.jp

Device fabrication

A monolayer graphene was grown using a chemical vapor deposition (CVD) on Cu foil and transferred on SiO_2/Si substrate. The channel was fabricated with photolithography and dry etching. During etching, H_2O gas was introduced at 10 Pa, and graphene was scraped at 100 W for 1 minute to for the channel shape. The IGR-EDLT were fabricated with six channels, lengths were 5, 20 and 100 μm, and widths were 30 and 80 μm. Au/Cr thin films (50/10 nm) were deposited as source and drain electrodes using photolithography and electron-beam evaporation. 400 nm of Li^+ conducting amorphous Li-Nb-O (*a*-LN) and 100 nm Li^+-hole mixed conducting $LiCoO_2$ thin films were then deposited by pulsed laser deposition. Pt (50 nm) was also deposited on top of the $LiCoO_2$ layer as a current collector.

Measurement method

IGR-EDLT measurements were carried out at room temperature in a vacuum chamber evacuated. Probers were used to connect the IGR-EDLT in the chamber, and electrical measurements were carried out using the source measure unit and pulse measure unit of semiconductor parameter analyzer (4200A-SCS, Keithley).

IPC calculation method

The memory capacity and nonlinearity of RC are quantitatively characterized by IPC. The target data $y_m(k)$ is an orthogonal polynomial that covered all linear and nonlinear combinations of inputs.

$$y_m(k) = \prod_{d=0}^{D} P_{n_{m,d}}[u(k-d)] \tag{S1}$$

P_n is an orthogonal polynomial of degree *n*' (*n*'=1, 2, …), *m*, *d*, and *D* represent the polynomial index, delay and maximum delay, respectively. The input $u(k)$ is a uniformly distributed random sequence. The capacity C_m of each component is calculated from the NMSE when reconstructing the target y_m expressed by Eq. S1 from the reservoir state $X(k)$, obtained by injecting $u(k)$ into the reservoir as follows:

$$C_m = 1 - \mathrm{NMSE}' \tag{S2}$$

The NMSE' is the sum of squared errors divided by the target sum of squares. The total capacity C_{tot} is the sum of these component capacities.

$$C_{\mathrm{tot}} = \sum_{m=1}^{M} C_m \tag{S3}$$

M is the total number of indexes determined by the combination of order and delay length. The capacity by order, C_n, was calculated as the sum of the capacity by components where the total number of orders of interest is n:

$$C_n = \sum_{m(n)} C_m \tag{S4}$$

$m(n)$ represents all the indices of all orders n. To prevent overestimation of IPC, we used a surrogate method [S1, S2]. The threshold set at 1.5 times the surrogate capacity.

Electrical responses in each condition and the results of the NARMA2 task

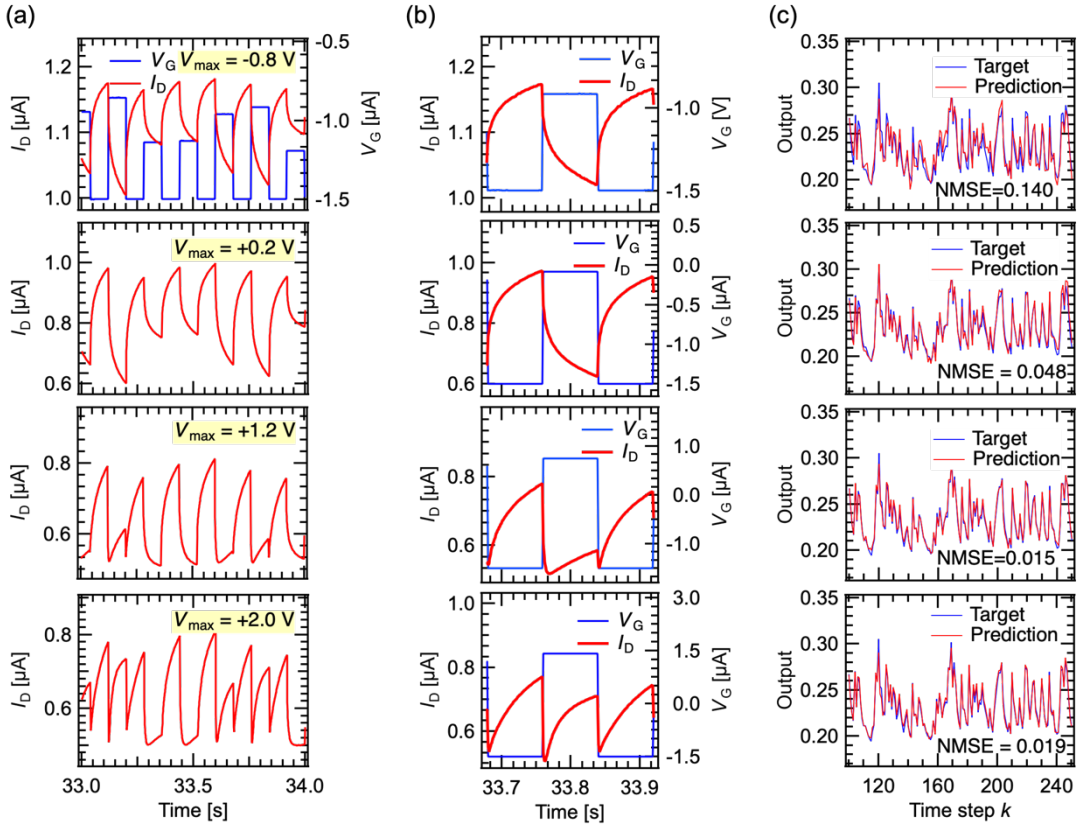

Fig. S1. (a)I_D response in V_G pulse measurement. (b)Enlarged view of I_D response in V_G pulse measurement. (c)Target waveform and predict waveform in NARMA2 task.

The results of four representative points (V_{max} = -0.8 V, V_{max} = +0.2 V, V_{max} = +1.2 V, and V_{max} = +2.0 V) are shown in Fig. S1. As shown in Fig.S1(a), the response current I_D to the applied V_G pulses. The I_D response becomes more complex as V_{max} increases. Figure S1(b) is an enlarged view of Fig. S1(a), where V_{max} = +1.2 V and V_{max} = +2.0 V include the Dirac point in the V_G range, and a quasi-second harmonic was generated. Figure S1(c) shows the calculation results of the NARMA2 task for each condition, among which V_{max}

= +1.2 V was the best score.

Observation of quasi-second harmonic by the I_D - V_G cycle measurement

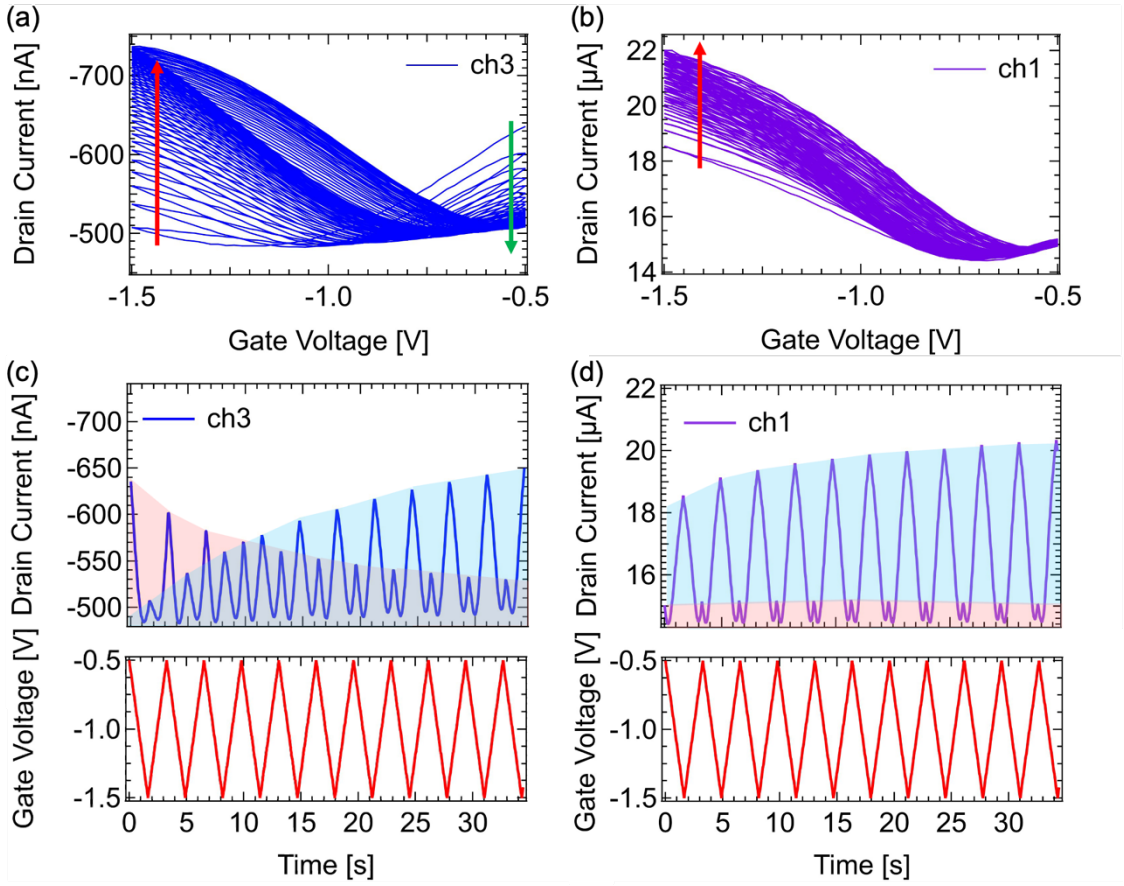

Fig. S2. (a)The I_D-V_G response to the triangular wave input (ch3). (b)The I_D-V_G response to the triangular wave input (ch1). (c)The I_D response vs time (ch3). (d)The I_D response vs time (ch1).

Figure S2(a) and (b) show the I_D - V_G response for ch1 (length was100 µm and width was 30 µm) and ch3 (length was5 µm and width was 30 µm) when the gate voltage (V_G) of a transistor is swept continuously for 40 cycles within the range of -1.5 V to -0.5 V. With each cycle, the drain current increases in the negative voltage side of the Dirac point. Figure S3(c) and (d) show the same measurement results as in Fig. S3(a) and (b) but shown with time on the horizontal axis and I_D on the vertical axis. In both Fig. S3(c) and Fig. S3(d), the quasi-second harmonic wave is observed. While it increases in ch3, it remains almost constant in ch1. As seen in the contrast behavior, the electrical response differs depending on the channel.

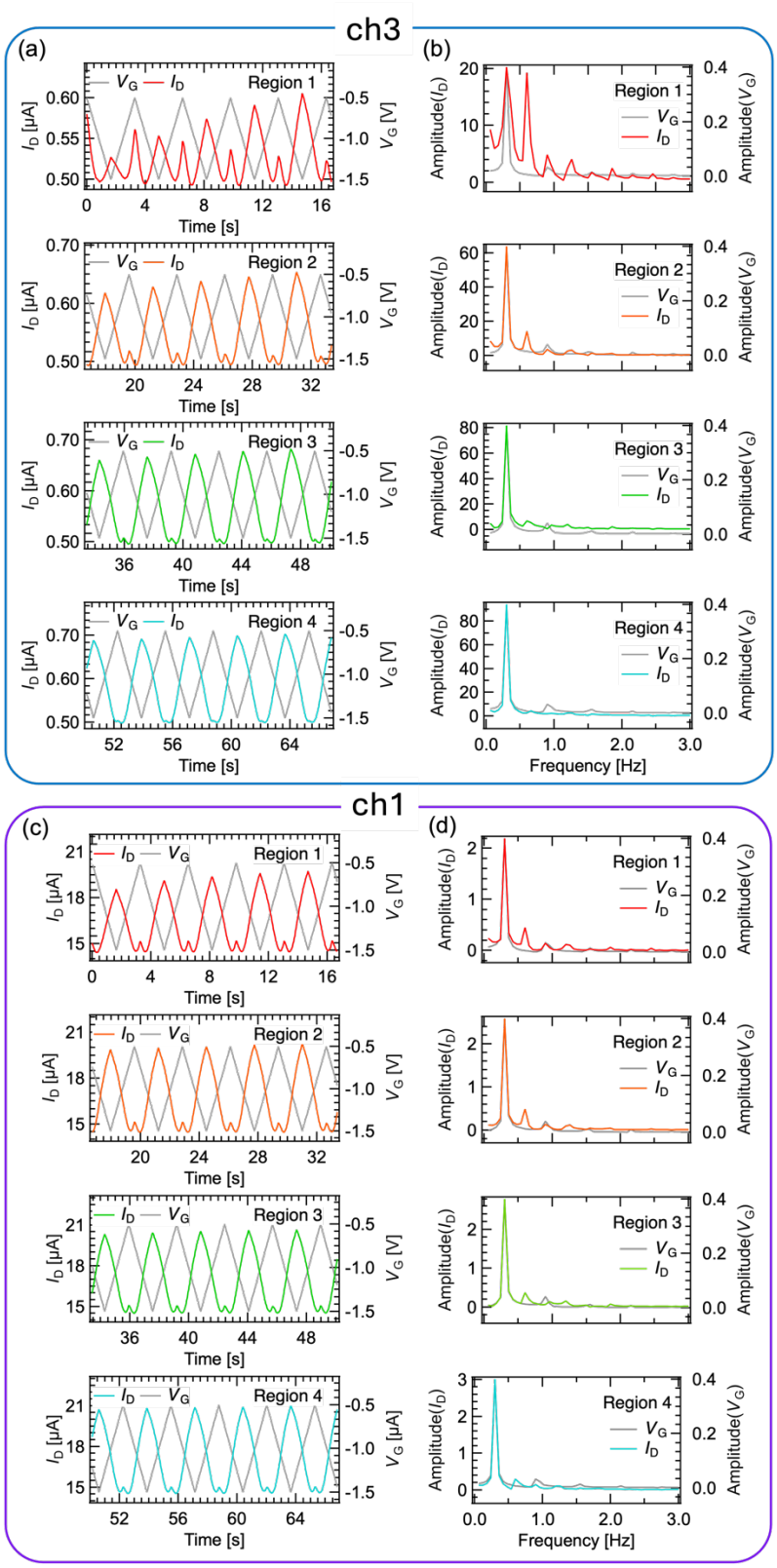

Fig. S3. (a)The I_D - V_G response for ch3. (b)The fast Fourier transform (FFT) spectrum of ch3. (c)The I_D - V_G response for ch1. (d)The FFT spectrum of ch1

The I_D response to the triangular wave input shown in Fig. S2(c,d) was divided into four regions, and the fast Fourier transform (FFT) spectra were calculated as shown in Fig. S3. Figure S3(a) shows the divided I_D response of ch3. In region 1, the quasi-second harmonic due to including the Dirac point in the V_G range is observed. Corresponding to this response, overtones were clearly observed in the FFT spectrum of region 1, as shown in Fig. S3(b). As the quasi-second harmonic due to the Dirac point weakened from region 1 to 4, the FFT spectrum also showed a decrease in overtones. The overtones were also observed in the FFT spectrum corresponding to the I_D response of ch1, as shown in Fig. S3(d). A similar decrease in overtones was observed in Fig. S3(d), although the decrement was not as pronounced as in ch3. The contrast difference in the two FFT spectra agrees well with the corresponding two I_D responses in Fig. S3(a,c).

References

[S1] J. Dambre, D. Verstraeten, B. Schrauwen, and S. Massar, Information processing capacity of dynamical systems. *Scientific reports*, *2*(1), 514. (2012).

[S2] S. Tsunegi, T. Kubota, A. Kamimaki, J. Grollier, V. Cros, K. Yakushiji, A. Fukushima, S. Yuasa, H. Kubota, K. Nakajima and T. Taniguchi, Information processing capacity of spintronic oscillator. *Advanced Intelligent Systems*, *5*(9), 2300175 (2023).