Boron-doped diamond MOSFETs operating at temperatures up to 400 °C

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Abstract

The boron-doped diamond (B-diamond) metal-oxide-semiconductor field-effect transistors (MOSFETs) are fabricated and characterized at operating temperatures up to 400 ℃. The SiO_2 serves as the gate oxide insulator, while the Ti/Pt bilayer is employed as the gate contact metal. As the operating temperature rises from room temperature (RT) to 400 ℃, the absolute drain current for the B-diamond MOSFET increases from 3.9 μA mm^{-1} to 177.4 μA mm^{-1}. Conversely, the on-resistance decreases significantly from 1469.8 kΩ mm to 16.5 kΩ mm. The on/off ratio for the MOSFET at RT is 1.9 × 10^5, which increases to over 5.0 × 10^6 at temperatures exceeding 100 ℃. The threshold voltage exhibits a decreasing trend, though it deviates from this trend at 300 ℃. The subthreshold voltage and extrinsic transconductance maximum show increasing trends from 113 mV dec^{-1} to 299 mV dec^{-1} and from 0.9 μS mm^{-1} to 23.1 μS mm^{-1}, respectively. The interfacial trapped charge density is found to be stable in the range of 8.0 × 10^{11} ~ 2.3 × 10^{12} eV^{-1} cm^{-2}.

1. Introduction

Due to its exceptional intrinsic properties such as a wide bandgap energy, high breakdown field, high carrier mobility, and excellent thermal conductivity, diamond has been extensively studied for applications in high-power, high-frequency, and high-temperature electronic devices [1, 2]. Hydrogen-terminated surface channels and bulk-doped diamond channels are utilized in the production of electronic devices such as metal-oxide-semiconductor field-effect transistors (MOSFETs) [3-12].

Surface carbon-hydrogen bonds and negatively charged acceptors are two essential requirements for hole accumulation in the *p*-type hydrogen-terminated diamond (H-diamond) channel layer. The H-diamond-based MOSFETs exhibited outstanding electrical characteristics, including a drain current maximum ($I_{D,max}$) of 1.35 A mm^{-1} [3], an extrinsic transconductance maximum ($g_{m,max}$) of 206 mS mm^{-1} [3], a cut-off frequency of 70 GHz [7], and a robust breakdown voltage of 3326 V [13]. However, the limited thermal stability led to unsatisfied high-temperature performance [14] due to the degradation of negatively charged acceptors on the H-diamond [15].

In the case of bulk-doped diamond channels like the *p*-type boron-doped diamond (B-diamond) and *n*-type phosphorus-doped diamond (P-diamond) channel layers, the activation energies of boron (370 meV) and phosphorus (570 meV) dopants significantly exceed the thermal energy (26 meV) available at room temperature (RT) [1]. Consequently, their carrier densities are relatively low. The MOSFETs on the B-diamond and P-diamond exhibited low $I_{D,max}$ and $g_{m,max}$ values [9, 10, 16]. Nevertheless, as there is no surface thermal sensitivity issue with bulk-doped diamond channels, it is anticipated that the B-diamond and P-diamond MOSFETs can perform effectively at high temperatures.

Previously, we have fabricated the B-diamond MOSFETs and examined their electrical properties [11, 12, 17]. At RT, the B-diamond MOSFET displayed an $I_{D,max}$ of -1.2 mA mm^{-1} and a $g_{m,max}$ of 29.0 μS mm^{-1}. Impressively, even at an operating temperature of 300 ℃, the B-diamond MOSFET continued to perform well, showing an $I_{D,max}$ of -10.9 mA mm^{-1} and a $g_{m,max}$ of 215.7 μS mm^{-1} [17]. However, while operating temperature up to 400 ℃, significant degradation in the performance of the B-diamond MOSFETs was observed. This degradation is likely attributed to that the in-situ high-temperature annealing deteriorates the qualities of the Al_2O_3 gate oxide insulator and the Ti/Au bilayer gate contact metal.

To further improve the performance of B-diamond MOSFETs at high operating temperatures, we have employed SiO_2 gate insulator and Ti/Pt bilayer gate contact metal in the fabrication process. We have conducted a thorough examination and discussion of their electrical characteristics at operating temperatures of RT, 100 ℃, 200 ℃, 300 ℃, and 400 ℃.

2. Experimental

The fabrication process for the B-diamond MOSFETs has been reported previously [17]. Initially, the Ib-type (100) diamond substrate underwent cleaning by immersion in a solution of H_2SO4 + HNO_3 at 300 ℃ for 3 hours. Subsequently, the B-diamond epitaxial layer was grown using a microwave plasma-assisted chemical vapor deposition system with source gases of H_2 and CH_4 [18]. Boron was sourced from the residual boron in the chamber of the prior B-diamond growth. Secondary ion mass spectrometry measurement indicated that the B-diamond epitaxial layer had a thickness of 825 nm with a boron atom concentration of approximately 4×10^{15} cm^{-3}.

The B-diamond epitaxial layer underwent treatment in the acid solution (H_2SO_4 +

HNO_3) once more, converting its hydrogen surface to oxygen. Source and drain electrodes, comprised of a Ti/Au bilayer (10/150 nm), were evaporated onto the B-diamond using an electron-gun evaporation system. The chamber pressure for evaporating the Ti/Au bilayer was around 10^{-6} Pa, with evaporation rates for Ti and Au of 1.0 and 2.0 Å s^{-1}, respectively. Annealing at 550 ℃ for 20 minutes in an Ar atmosphere facilitated the formation of Ohmic contacts using a rapid thermal annealing system.

A SiO_2 gate oxide, approximately 11 nm thick, was deposited through an atomic layer deposition system at 300 ℃ using bis(diethylamino)silane and ozone precursors. The pulse times for these precursors were 200 msec and 150 msec, with purge times of 4 s and 6 s, respectively. The carrier gas of N_2 flowed at a rate of 100 sccm. A Ti/Pt (10/100 nm) bilayer served as the gate electrode formed using the electron-gun evaporation system. Evaporation rates for Ti and Pt were set at 1.0 and 0.5 Å/s, respectively. Following this, a 7.6 nm-thick SiO_2 film was redeposited to cover the entire sample surface. This additional SiO_2 layer served to protect the B-diamond MOSFETs from environmental effects and the edge leakage of the electrodes, thereby enhancing their reliability and performance. Electrode access windows were created by etching the SiO_2 film in the HF acid solution. The electrical characteristics for the B-diamond MOSFETs were obtained using a Grail 10-5-LV-HTV prober system across temperatures ranging from RT to 400 ℃.

3. Results and discussion

Figures 1(a) and 1(b) show microscope image and schematic diagram of the B-diamond MOSFET, respectively. The diameter for the drain electrode is 301.6 μm. The gate width (W_G) can be computed as 947.0 μm. The gate length is 4.8 μm. The

interspatial distances for the gate-to-source and gate-to-drain electrodes are both 5.0 μm.

Figure 2(a) shows the I_D as a function of drain voltage (V_D) for the B-diamond MOSFET operating at RT. The V_{GS} varies from -2.0 to 33.0 V in steps of +1.0 V. The B-diamond MOSFET shows obvious saturation regions and operates with a *p*-type characteristic. The absolute $I_{D,max}$ for the B-diamond MOSFET operating at RT is 3.9 μA mm^{-1}, which is lower than that of the previous reported value of 1.2 mA mm^{-1} [17]. It was confirmed that the low doping level and thin channel layer thickness for the B-diamond epitaxial layer would lead to the decrease of $I_{D,max}$ [19]. These are the reasons for the lower $I_{D,max}$ here. Based on the linear region for the I_D-V_D characteristic at the V_{GS} of -2.0 V, on-resistance (R_{ON}) normalized by the W_G can be deduced to be 1469.8 kΩ mm.

The I_D as a function of gate-to-source voltage (V_{GS}) for the B-diamond MOSFET operating at RT is shown in Fig. 2(b). The V_D is kept at -10.0 V. The on/off ratio is determined at the V_{GS} of -2.0/15.0 V to be 1.9×10^5. Through linear extrapolation, threshold voltage (V_{TH}) is found to be 8.3 V. Subthreshold voltage (*SS*) value for the MOSFET operating at RT is determined to be 113 mV/dec. Then, interfacial trapped charge density (D_{it}) of the SiO_2/B-diamond at RT can be calculated using the following equation (1) [20].

$$SS = \frac{kT}{q}\ln(10)\left(1+\frac{qD_{it}}{C_{OX}}\right), \quad (1)$$

where *k*, *T*, *q*, and C_{OX} are Boltzmann's constant (8.62×10^{-5} eV K^{-1}), operating temperature, elementary charge (1.6×10^{-19} C), and SiO_2 oxide capacitance (0.314 μF/cm^2) which is calculated based on its thickness (11 nm) and dielectric constant (3.9),

respectively. The D_{it} for the B-diamond MOSFET operating at RT is computed as 1.8 × 10^{12} eV^{-1} cm^{-2}, which is better than that of the Al_2O_3/B-diamond interface of 7.2 × 10^{12} eV^{-1} cm^{-2} [17]. Since the oxygen vacancies on the surface of the B-diamond and the interfacial quality of the oxide/B-diamond can be modified by the oxygen precursors during the atomic layer deposition [12], opting for a higher deposition temperature of 300 ℃ for SiO_2 compared to the 200 ℃ for Al_2O_3 would possibly enhance these modifications, leading to the better interfacial quality for SiO_2/B-diamond and the low D_{it}.

Figure 3(a) displays the I_D-V_D characteristics for the B-diamond MOSFETs operating from 100 ℃ to 400 ℃ with the V_{GS} maintained at -2.0 V. Even at an elevated operating temperature of 400 ℃, the B-diamond MOSFET continues to operate well. Therefore, the transition of gate oxide insulator from Al_2O_3 to SiO_2 and gate cover metal from Ti/Au to Ti/Pt have enhanced the high-temperature properties for the B-diamond MOSFETs. The $I_{D,max}$ values for the B-diamond operating at 100, 200, 300, and 400 ℃ are -33.3, -57.8, -78.1, and -177.4 μA mm^{-1}, respectively. Correspondingly, their R_{ON} values are determined to be 191.8, 106.6, 75.5, and 16.5 kΩ mm, respectively. Fig. 3(b) illustrates the I_D-V_{GS} characteristics for the B-diamond MOSFETs operating from 100 ℃ to 400 ℃. The on/off ratios of them exceed 5 × 10^6, surpassing the MOSFET operating at RT. With the fluctuation in operating temperature, the V_{TH} value undergoes significant shifts, indicating the variations of charges and hole densities for the B-diamond MOSFETs. Further details regarding the on/off ratio, V_{TH} value, *SS* value, and D_{it} value will be elaborated in subsequent discussions.

Figures 4(a) and 4(b) present summaries of the I_D and R_{ON} as functions of operating temperature for the B-diamond MOSFETs, respectively. As the operating

temperature increases, the absolute $I_{D,max}$ increases from 3.9 to 177.4 μA mm^{-1}. The $I_{D,max}$ operating at 400 ℃ is approximately 45 times greater than that operating at RT. Conversely, the R_{ON} experiences a significant decrease from 1469.8 kΩ mm at RT to 16.5 kΩ mm at 400 ℃. The activation of boron dopants at higher operating temperatures enhances the carrier density and augments the properties of the B-diamond MOSFETs.

Figures 5(a), 5(b), 5(c), and 5(d) summarize the on/off ratio, V_{TH}, *SS* value, and D_{it} as functions of operating temperature for the B-diamond MOSFETs, respectively. The on/off ratios for the B-diamond MOSFET exceeding 100 ℃ are more than one order higher than that at RT, indicating efficient control over the flow of current at higher operating temperatures. The V_{TH} exhibits a decreasing trend, though it deviated from this trend at 300 ℃, possibly due to the variations of charges in the SiO_2 or at the Pt/Ti/SiO_2 interfaces. With the increase in operating temperature, the *SS* value rises from 113 mV/dec at RT to 299 mV/dec at 400 ℃. Based on the equation (1), the D_{it} can be computed to be stable in the range of $8.0 \times 10^{11} \sim 2.3 \times 10^{12}$ eV^{-1} cm^{-2}. Consequently, the elevated operating temperature does not degrade the interfacial quality for the SiO_2/B-diamond.

Figures 6(a) and 6(b) depict the g_m -V_{GS} characteristics and $g_{m,max}$ as a function of operating temperature for the B-diamond MOSFETs, respectively. At RT, the $g_{m,max}$ is 0.9 μS mm^{-1}, which significantly increases to be more than 25 times, reaching 23.1 μS mm^{-1} at 400 ℃. Table 1 summarizes the electrical properties of the B-diamond MOSFETs operating across the temperatures ranging from RT to 400 ℃. With the increase of operating temperature, the $I_{D,max}$, on/off ratio, and $g_{m,max}$ demonstrate improvements, showcasing enhanced performance characteristics of the B-diamond

MOSFETs as the temperature rises.

4. Conclusions

To enhance the performance of the B-diamond MOSFETs operating at temperatures up to 400 ℃, the utilization of SiO_2 gate insulator and Ti/Pt bilayer gate contact metal was adopted in their fabrication. A comprehensive investigation and discussion of their electrical properties at operating temperatures ranging from RT, 100 ℃, 200 ℃, 300 ℃, to 400 ℃ were conducted. As the operating temperature increased, the absolute $I_{D,max}$ surged from 3.9 μA mm^{-1} to approximately 45 times the value, reaching 177.4 μA mm^{-1}. The on/off ratios for the B-diamond MOSFETs at temperatures surpassing 100 ℃ exceeded one order higher than that at RT. Furthermore, the $g_{m,max}$, initially at 0.9 μS mm^{-1} at RT, increased significantly to more than 25 times of 23.1 μS mm^{-1} at 400 ℃. This study is of importance for understanding the behavior and performance of B-diamond MOSFETs operating at high temperatures such as 400 ℃.

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Disclosure Statement

No potential conflict of interest was reported by the authors.

Table 1. Summary of electrical properties of the B-diamond MOSFETs operating across the temperatures range from RT to 400 ℃.

	RT	100 ℃	200 ℃	300 ℃	400 ℃
$I_{D,max}$ (μA mm^{-1})	-3.9	-33.3	-57.8	-78.1	-177.4
R_{ON} (kΩ mm)	1469.8	191.8	106.6	75.5	16.5
On/off	1.9×10^5	6.4×10^6	2.2×10^7	5.3×10^6	5.5×10^6
V_{TH} (V)	8.3	7.3	6.8	11.5	4.1
SS (mV dec^{-1})	113	153	139	170	299
D_{it} (eV^{-1} cm^{-2})	1.8×10^{12}	1.8×10^{12}	8.0×10^{11}	8.5×10^{11}	2.3×10^{12}
$g_{m,max}$ (μS mm^{-1})	0.9	6.9	11.5	21.0	23.1

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Figure captions

Figure 1. (a) Microscope image and (b) schematic diagram of the B-diamond MOSFET, respectively.

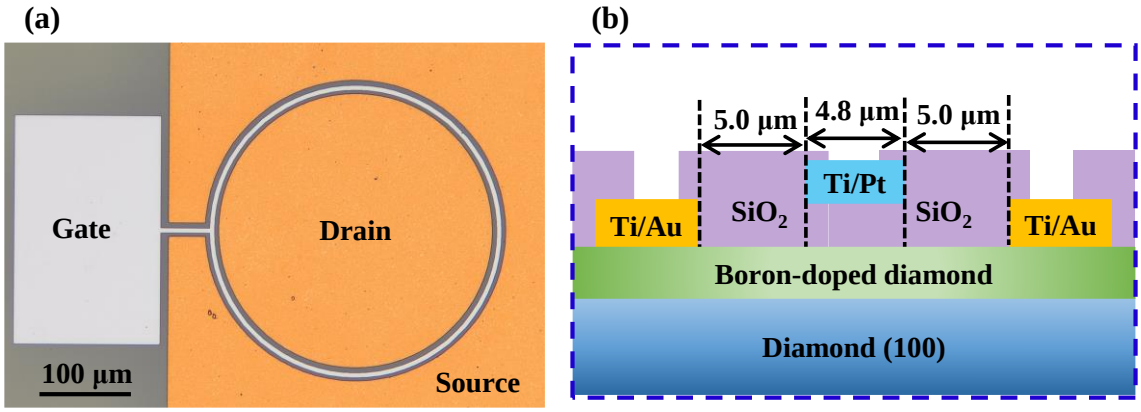
Figure 2. (a) I_D-V_D and (b) I_D-V_{GS} characteristics for the B-diamond MOSFET operating at RT, respectively. The V_{GS} in Fig. 2 (a) is changed from -2.0 V to 33.0 V in steps of +1.0 V. The V_D in Fig. 2(b) is kept at -10.0 V.

Figure 3. (a) I_D-V_D and (b) I_D-V_{GS} characteristics for the B-diamond MOSFETs operating from 100 ℃ to 400 ℃. The V_{GS} in Fig. 3(a) is kept at -2.0 V. The V_D in Fig. 3(b) is kept at -10.0 V.

Figure 4. (a) I_D and (b) R_{ON} as functions of operating temperature for the B-diamond MOSFETs, respectively.

Figure 5. (a) On/off ratio, (b) V_{TH}, (c) *SS* value, and (d) D_{it} as functions of operating temperature for the B-diamond MOSFETs, respectively.

Figure 6. (a) g_m -V_{GS} characteristics and (b) $g_{m,max}$ as a function of operating temperature for the B-diamond MOSFETs, respectively.



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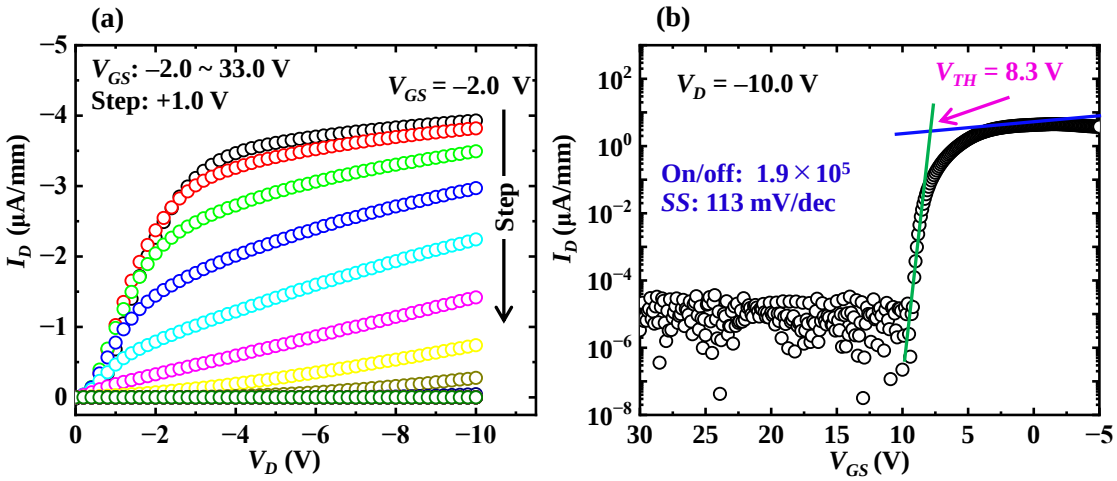

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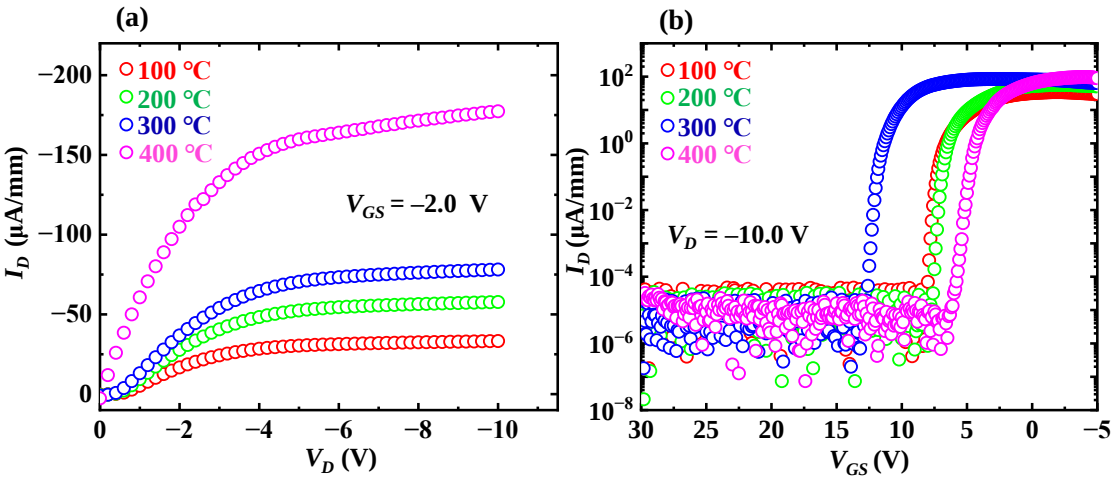

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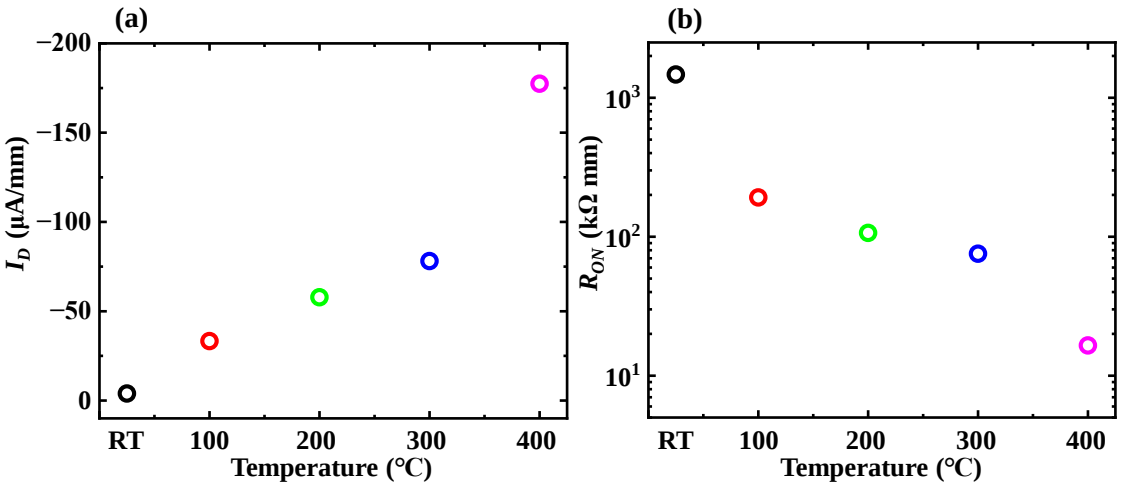

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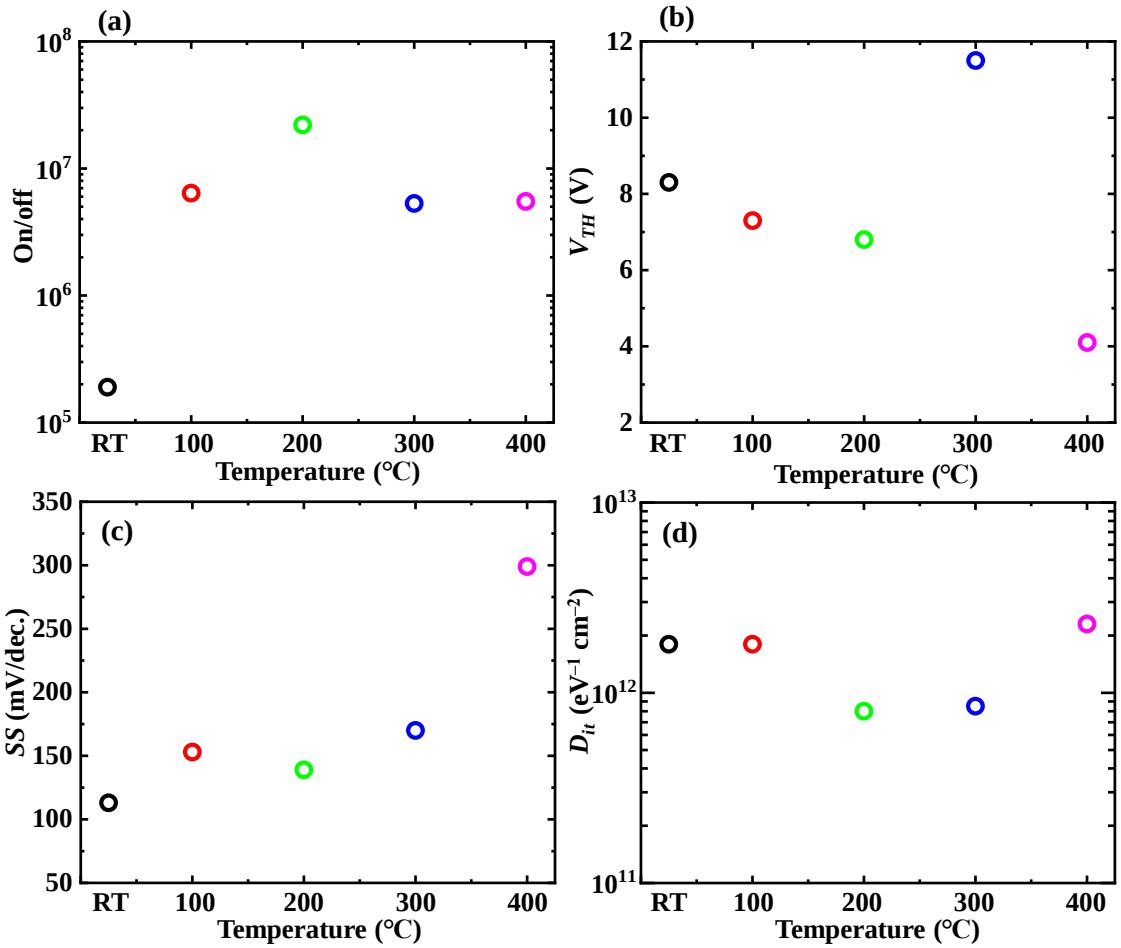

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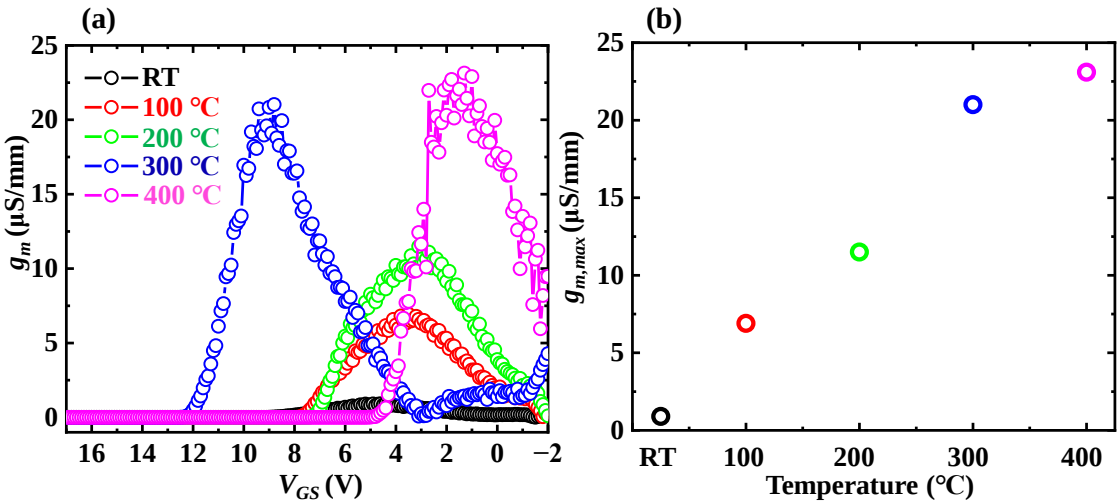

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