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A back-to-back diode model applied to van der Waals Schottky diodes

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Abstract

The use of metal and semimetal van der Waals contacts for 2D semiconducting devices has led to remarkable device optimizations. In comparison with conventional thin-film metal deposition, a reduction in Fermi level pinning at the contact interface for van der Waals contacts results in, generally, lower contact resistances and higher mobilities. Van der Waals contacts also lead to Schottky barriers that follow the Schottky–Mott rule, allowing barrier estimates on material properties alone. In this study, we present a double Schottky barrier model and apply it to a barrier tunable all van der Waals transistor. In a molybdenum disulfide (MoS_2) transistor with graphene and few-layer graphene contacts, we find that the model can be applied to extract Schottky barrier heights that agree with the Schottky–Mott rule from simple two-terminal current–voltage measurements at room temperature. Furthermore, we show tunability of the Schottky barrier *in-situ* using a regional contact gate. Our results highlight the utility of a basic back-to-back diode model in extracting device characteristics in all van der Waals transistors.

Keywords: diodes, back-to-back, model, applied, MoS_2, van der Waals

1. Introduction

In metal-semiconductor-metal devices, diode models have been used to calculate and extract device characteristics, such as the Schottky barriers and diode ideality factors, from simple electrical measurements [1–4]. Due to strong Fermi level pinning (FLP) though, these characteristics typically do not agree with the Schottky–Mott theory, and it is challenging to separate model inadequacies and intrinsic device characteristics. For instance, no change in the extracted Schottky barriers from a back-to-back model for tin oxide nanobelt junctions has been reported, even for different contact metals [4].

FLP at the interface between a metal and a semiconductor can be detrimental to device performance, ultimately increasing contact resistance and reducing device mobility. In two-dimensional (2D) material devices with evaporated metal contacts, FLP has been identified as a significant contribution to inhibiting device performance [5, 6]. They also lead to Schottky barriers that deviate greatly from the Schottky–Mott rule and typically, a pinning factor is incorporated in Schottky–Mott theory to account for FLP [6, 7]. FLP in these devices results from both intrinsic and extrinsic effects, complicating estimates of Schottky barriers based on contact metals alone. Intrinsic effects leading to FLP include the formation of metal-induced gap states (MIGS) from

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metal d-orbital and chalcogen p-orbital overlap [8], metalized interfaces for some contact metals [9, 10], and interfacial charge redistribution [11]. Extrinsic effects further promoting FLP in these devices include defect induced gap states (DIGS) from intrinsic vacancies and surface vacancies introduced during metal deposition [12].

Several strategies have been implemented to reduce FLP in 2D material devices [13]. Some successful achievements have been using metallic 2D materials as contacts [14–16], inserting a buffer layer between the metal and the channel material [17], phase engineering of the 2D material itself [18, 19], mechanical transfer of metals on top of 2D materials [20], and edge contacts [21]. Generally, these methods act to strongly reduce MIGS and further contributions from DIGS to de-pin the Fermi level at the interface. Using 2D materials as metal contacts is particularly attractive because, in the case of graphene, this allows tunability of the Schottky barrier through electrostatic modulation of the Fermi energy in the contact metal. The graphene barristor showed that the Schottky barrier can be directly tuned at the interface between graphene and silicon [22]. Using van der Waals metals as a contact is also theoretically expected to reduce MIGS and thereby lower FLP [14]. This can then lead to devices that approach the Schottky–Mott limit and Schottky barriers that can be estimated based on material characteristics alone. For example, accurate Schottky barriers can be extracted for van der Waals materials connected to tungsten disulfide (WS2) [23], tungsten diselenide (WSe2) [24] and indium selenide (InSe) [25]. This allows for optimized devices for next generation computing, sensing, and digital-analog chips [26, 27].

A diode model that shows consistency with Schottky–Mott theory for van der Waals contacted 2D semiconductors is desirable to efficiently extract device characteristics from simple electrical measurements without the need of model additions such as pinning factors. Here, we show that a straightforward back-to-back diode model can be applied to metal van der Waals contacted MoS_2 junctions. The model extracts barriers that are in general agreement with the Schottky–Mott rule. In few-layer graphene contacted MoS_2 devices, we extract barriers of 0.46 eV−0.58 eV, varying according to the gating conditions. For a graphene contact we extract barriers of 0.37 eV−0.74 eV for different contact gate voltages. Our results here show that the simple model is capable of capturing reasonable barrier values for both graphene and few-layer graphene contacts to few-layer MoS_2 flakes.

2. Results

A back-to-back diode model is implemented to extract device characteristics from simple two-terminal electrical measurements [1–4]. Our open source python script of the model is available for others to use [28]. The current through each contact of the device can be written from thermionic theory as:

$$I_1 = I_{s1}\left(e^{\frac{qV_1}{kT}} - 1\right), I_2 = -I_{s2}\left(e^{\frac{-qV_2}{kT}} - 1\right), \tag{1}$$

where

$$I_{s1,s2} = S_{1,2}A^*T^2\left(e^{-\frac{\phi_{B01,B02}}{kT}}\right), \tag{2}$$

are the reverse saturation currents, $V_{1,2}$ are the voltage drops across each contact, k is the Boltzmann constant, T is the temperature, $S_{1,2}$ are the contact areas, A^* is the Richardson constant, and $\phi_{B01,B02}$ are the Schottky barriers. For simplicity, we make the assumption that the voltage drops are equal across each contact, $V_1 = V_2 = V/2$. The total current through the device must be equal to the currents through each junction ($I_{tot} = I_1 = I_2$) and the total voltage drop is equal to the sum of the voltage drops across each junction ($V = V_1 + V_2$). Through a little algebra, the total current can be expressed as:

$$I_{tot} = \frac{2I_{s1}I_{s2}\sinh\left(\frac{qV}{2kT}\right)}{\left(I_{s1}e^{\frac{qV}{2kT}} + I_{s2}e^{-\frac{qV}{2kT}}\right)}. \tag{3}$$

Figures 1(a) and (c) shows the calculated current for two ideal cases ($n_1, n_2 = 1$) with equal and unequal junction barriers. The exponential increase in current around zero bias is present. The current saturates at higher biases set by the reverse saturation current of the reversed-biased junction. For non-ideal cases in nanoscale junctions, the intrinsic Schottky barriers ($\phi_{B01,B02}$) can be replaced by effected barriers that include the voltage dependence (image charge lowering) and an ideality constant, n, to account for defects and interface oxides. The effective barriers can be written as:

$$\phi_{B1,B2} = \phi_{B01,B02} \pm eV_{1,2}\left(1 - \frac{1}{n_{1,2}}\right). \tag{4}$$

Two examples of non-ideal diode curves are shown in figures 1(b) and (d) for equal and unequal barrier strengths. A more gradual nonlinearity is observed that is reminiscent of experimental current–voltage curves for nanoscale devices.

This model is used to extract ideality constants (n_1, n_2) and Schottky barriers from simple two terminal current–voltage measurements in an all van der Waals transistor composed of MoS_2 with graphene and few-layer graphene contacts. We note that the model could also be applied to metal contacted devices but the extracted Schottky barriers typically will not agree with the Schottky–Mott rule due to strong Fermi level pinning. Figure 2(a) shows an optical image of the device. To fabricate the device, prepatterned gold electrodes, accompanied by a chromium layer for adhesion, are deposited onto a heavily doped silicon wafer with 285 nm of SiO_2. The doped substrate is used as a global back gate to gate the MoS_2 channel. A van der Waals heterostructure is stacked and transferred on top of electrodes using dry stacking and heated transfer techniques [29, 30]. The heterostructure is composed of, in stack order, an encapsulating top boron nitride (BN), two few-layer graphene flakes, an MoS_2 flake, a graphene flake, and a bottom BN flake used as a gate dielectric for the contact gate. On the left side (figure 2(a)), the MoS_2 flake (labeled 2) is connected to a gold electrode by a graphene flake (labeled 1, contact area 15×10^{-8} cm^{-2}). At the junction of the MoS_2 flake and the graphene, there is a gold finger gate. On the right side,

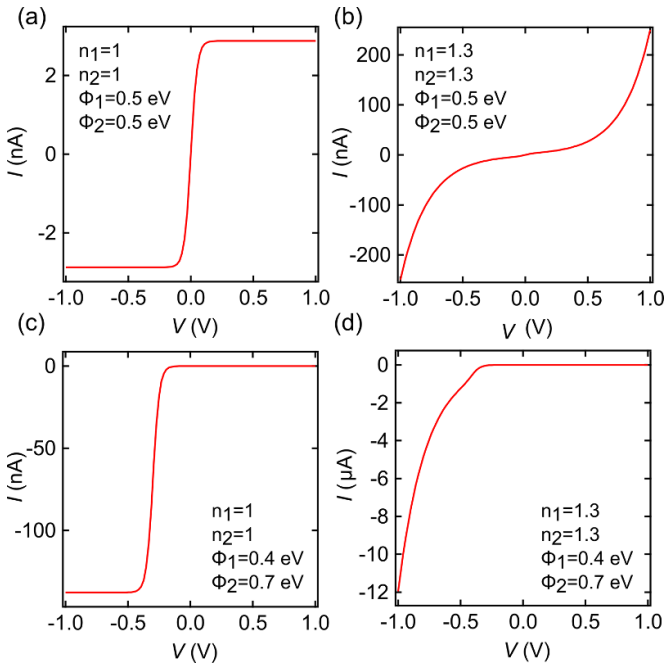

Figure 1. Calculated current–voltage curves for a back-to-back diode model. (a) An ideal case in which the ideality constants are 1 and the Schottky barriers are equal. (b) A non-ideal case in which the ideality constants are 1.3 and the barriers are equal. (c) An ideal case in which the ideality constants are 1 and the barriers are not equal. (d) A non-ideal case in which the ideality constants are 1.3 and the barriers are unequal.

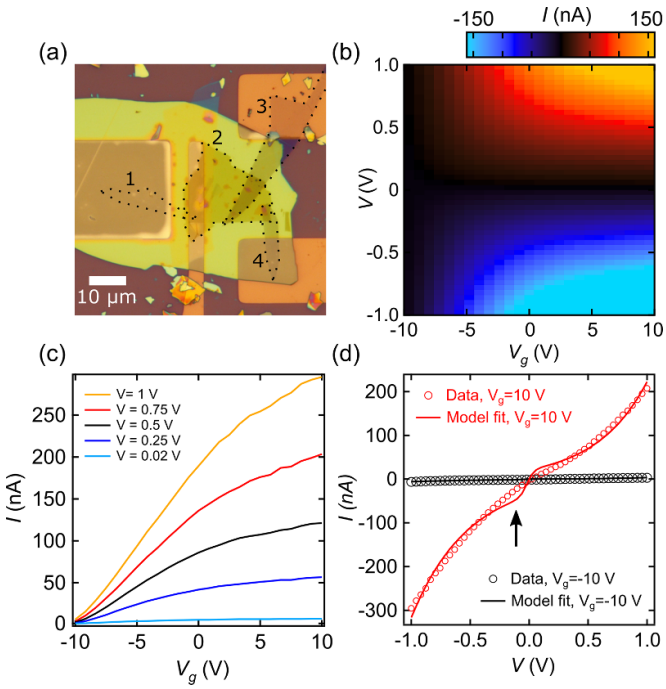

Figure 2. An MoS_2 transistor with graphene and few-layer graphene contacts. (a) An optical image of the device. The dotted lines outline the various flakes in the van der Waals heterostructure. 1 is the graphene flake on the left side of the image, 2 is the MoS_2 flake, and 3 and 4 are both few-layer graphene (8 layers, 2.7 nm thick) flakes on the right side. (b) Color plot of the current through the few-layer graphene contacts (3 source and 4 drain) as a function of bias voltage (V) and gate voltage (V_g). (c) $I-V_g$ curves for increasing positive bias voltage. (d) $I-V$ curves for gate voltages of -10 V (black) and 10 V (red). The solid lines indicate fits to the $I-V$ curves using the two diode model in the main text.

the same MoS_2 flake is connected to two few-layer graphene flakes (labeled 3, contact area 100×10^{-8} cm^{-2} and 4, contact area 15×10^{-8} cm^{-2}). From contrast analysis [31], the few layer graphene electrodes are both determined to be 8 layers or 2.7 nm thick. For all model calculations, we have used a Richardson constant of 80.3 A cm^{-2} K^{-2} for MoS_2 [32].

We first investigate the right side of the device, using the two few-layer graphene contacts as source and drain electrodes and the highly doped silicon substrate as a back gate. Figure 2(b) shows a 2D color plot of the drain current as a function of bias and gate voltage. The typical transistor response is observed, with the left side of the plot indicating the OFF state and the right side of the plot the ON state. The 1D gate sweeps for increasing bias voltage are shown in figure 2(c). Figure 2(d) shows $I-V$ curves in the OFF (black) and ON (red) states. Using the two diode model, we extract ideality constants close to 1 ($n_1 = 1.09, n_2 = 1.17$ in the OFF state and $n_1 = 1.12, n_2 = 1.14$ in the ON state) and Schottky barriers of $\phi_1 = 0.58$ eV, $\phi_2 = 0.58$ eV in the OFF state and $\phi_1 = 0.49$ eV, $\phi_2 = 0.46$ eV in the ON state. The most significant difference between the model and data is a low bias nonlinearity, highlighted by the black arrow in figure 2(d). This can be attributed to the absence of the series resistance of the MoS_2 flake itself from the model [2]. This series resistance leads to softening of the low bias nonlinearity in devices with similar barriers for source and drain.

The observed barrier lowering for increasingly positive gate voltage for both the source and drain due to the image charge effect is consistent with previous results showing similar behavior [33–35]. As a result of van der Waals contact, there is minimal Fermi level pinning and the Schottky–Mott relationship, $\phi_{1,2} = \phi_m - \chi_S$ where ϕ_m is the work function of the metal and χ_S is the electron affinity of the semiconductor, can be directly applied. Given that the electron affinity of MoS_2 is 4.0 eV [36] and the work function of few-layer graphene (graphite) is 4.5 eV [37], we would expect a Schottky barrier of 0.5 eV. This is consistent with our results and highlights the ease of extracting barrier information from simple two-terminal measurements. From the Schottky–Mott rule, any change in the work function of the contact material, including thickness dependent changes, would reflect in a change in the Schottky barrier height.

Using the contact gate, the Schottky barrier for the graphene to MoS_2 contact can be tuned independently. Figure 3(a) shows the current–voltage sweeps at $V_g = 10$ V for different contact gate voltages. For negative contact gate voltages, the $I-V$ curves show a clear diode-like response, with the forward current completely suppressed. For positive contact gate voltages, this suppression is lifted and finite forward currents are observed. By employing the double diode model once again, we can extract the Schottky barriers and ideality factors for different contact gate voltages. Figure 3(b) plots the curve in figure 3(a) for contact gate of -0.5 V (red circles). The diode model fit (black) produces Schottky

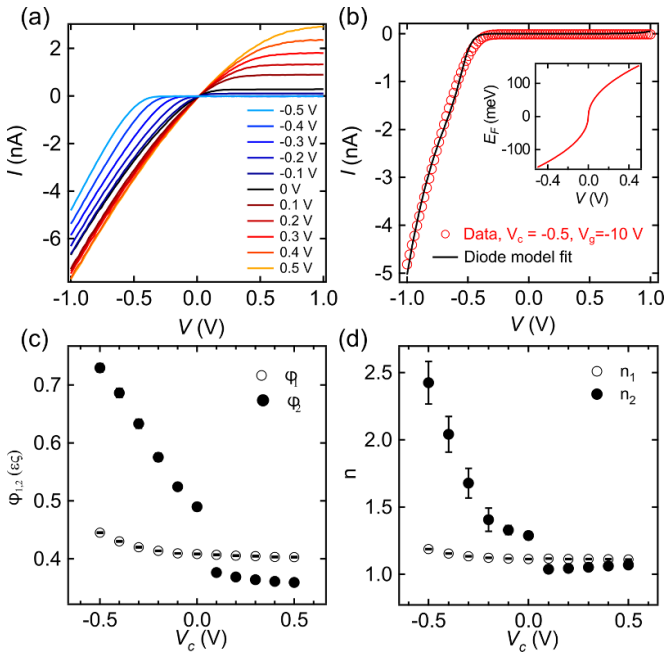

Figure 3. Tunable Schottky barriers in graphene contacted MoS_2. (a) Current as a function of bias voltage for different contact gate voltages. (b) Current as a function of bias voltage for a contact voltage of −0.5 V (red circles). The black curve shows the fit from the diode model. The inset shows a calculation of the Fermi energy in graphene as a function of contact gate voltage. (c) Extracted Schottky barriers for the graphene (ϕ_1) and few-layer graphene contact (ϕ_2) for the data shown in panel (a). The error bars show one-sigma uncertainty in the fitting parameters. (d) Extracted ideality factors for the graphene (n_1) and few-layer graphene (n_2) contact. The error bars show one-sigma uncertainty in the fitting parameters. All measurements made with source contact 1 (graphene) and drain contact 3 (few-layer graphene)..

barriers of $\phi_1 = 0.44$ eV (few-layer graphene) and $\phi_2 = 0.73$ eV (graphene), and ideality factors of $n_1 = 1.19$ and $n_2 = 2.42$ (respectively). The negative contact voltage pulls the Fermi energy of graphene into the valence band and increases the Schottky barrier for the corresponding contact. The contact gate completely shields the graphene-MoS_2 contact from the global back-gate.

The Schottky barriers and ideality factors from fits for all the data curves in figure 3 are shown in panels (c) and (d). Error bars in these figures indicate the standard deviations for each parameter from the fit. While the Schottky barrier for the few-layer graphene contact stays relatively constant over the change in contact gate voltage, the barrier at the graphene contact changes considerably, spanning more than 300 meV in energy. This behavior is also reflected in the ideality constants.

3. Discussion

Part of the barrier modulation can be understood from the electric field-induced change to the work function of graphene. The work function of graphene is marginally lower than graphite. Both experimental and theoretical studies report the work function to be approximately 4.3 eV [38–40]. This would correspond to Schottky barrier of 0.3 eV from the Schottky–Mott rule. Self-consistent density functional calculations of an explicit graphene-MoS_2 heterostructure estimate the Schottky barrier to be 0.37 eV [41]. This roughly aligns with our extracted barrier at zero contact gate voltage of 0.48 eV although residual doping of the graphene layer in contact with MoS_2 may be responsible for the discrepancy. The gate-induced change in the work function of graphene has been reported using surface Kelvin probe microscopy [42]. The Fermi energy in single-layer graphene can be calculated from:

$$E_{\mathrm{F}} = \mathrm{sign}\,(\Delta V_{\mathrm{g}})\,\hbar v_{\mathrm{F}}\,(\alpha\pi|\Delta V_{\mathrm{g}}|)^{1/2} \tag{5}$$

where α is the capacitance and v_{F} is the Fermi velocity. A calculation of the change in the Fermi energy with gate voltage for this device is shown in the inset of figure 3(b). For this calculation, the dielectric constant of BN is taken to be 3.76 [43]. The BN thickness for the graphene contact insulating layer is 6 nm, estimated by optical contrast analysis [44]. Over the 1-volt range of the contact gate, an isolated graphene layer typically exhibits a modulation of $E_{\mathrm{F}} \approx 300$ meV. In the case of a graphene in contact with MoS_2, there is an enhanced tunability of the barrier due to the influence of the gate on both materials. Calculations for this heterostructure show a significant change of 0.75 eV−0.03 eV when subjected to slightly larger electric field strengths (0.01 V/Ang vs. 0.008 V/Ang) [41]. This agrees with the magnitude of the Schottky barriers for negative contact gate in our measurements.

The lack of modulation of the Schottky barrier beyond 100 mV contact gate could be due to pinning from impurity levels in the MoS_2 itself [45]. While the influence of MIGS has been largely mitigated using 2D material contacts, there still may be some influence from DIGS. Rhenium impurities are known to be present in MoS_2 samples and lead to impurity states near the conduction band (0.29 eV below the conduction band)[45]. A similar trend in the change in Schottky barrier heights has been reported in graphene and few-layer graphene contacted MoS_2 devices [46, 47]. The barrier height modulation flattens for increasingly positive gate voltages.

4. Conclusions

We have shown that a straightforward back-to-back diode model can be used to extract Schottky barrier heights and ideality factors in MoS_2 transistors with graphene and few-layer graphene contacts. The lack of strong FLP leads to barrier heights that reasonably agree with the Schottky–Mott rule with consideration of defect doping. In an MoS_2 transistor with two few-layer graphene contacts, we extract barrier heights of 0.46 eV−0.58 eV depending on gating conditions. In an MoS_2 transistor with a graphene contact on one side, we extract a barrier height of 0.48 eV. Using a contact gate on the graphene contacted side of the device, we showed how the barrier heights could be directly tuned. Our results support the use of a simple back-to-back diode model in extracting characteristics in van der Waals contacted 2D semiconductors.

Data availability statement

The data that support the findings of this study are openly available at the following URL/DOI: https://github.com/islandlab-unlv/Back-to-back-diode-model.

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