Supporting Information: Correlating Carrier Localization to Optoelectronic Behavior of Monolayer MoS_2

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&- Equal Contribution $- Equal Contribution

AFM measurements

Thickness profile:

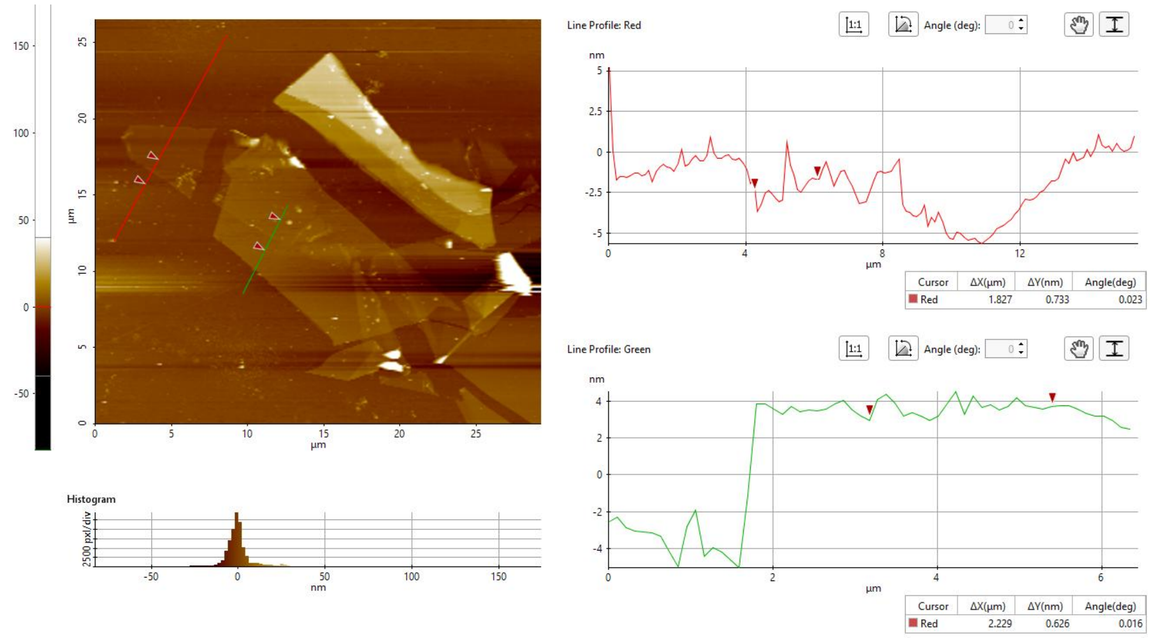

Fig. S1. The surface profile of MoS_2 in two different regions, MoS_2 and another region in MoS_2 on hBN, respectively. Red and green coloured lines show the height profile of MoS_2 in two separate regions. The thickness extracted from the measurement is 0.733nm, suggesting monolayer MoS_2.

Surface roughness.

(a) (b)

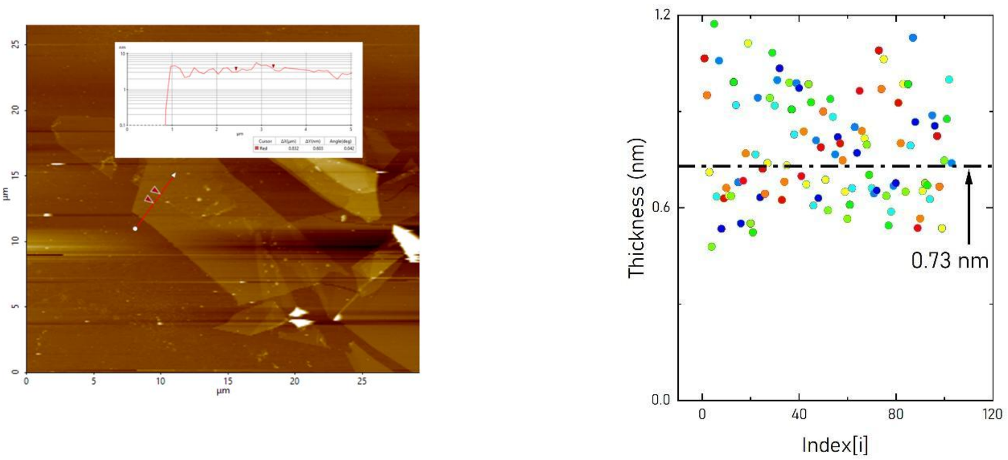

Fig. S2 (a) Atomic Force Microscopy (AFM) image of one of the fabricated devices to estimate the surface morphology and quality. (b) Thickness of MoS_2 channel at various places to estimate the surface roughness. The thickness came around 0.73 nm; the monolayer MoS_2 thickness with fluctuations.

Surface roughness calculation:

We calculated the surface roughness (R_a) of monolayer MoS_2 by using the formula mentioned in (Ruzova *et al, Results in Surfaces and Interfaces* (2025): 100441), with reference to Fig. S2 (a). In our case, n=100, m=0.733nm (from Fig. S1(b)). The roughness of monolayer MoS_2 is 0.14 nm.

Raman Spectroscopy

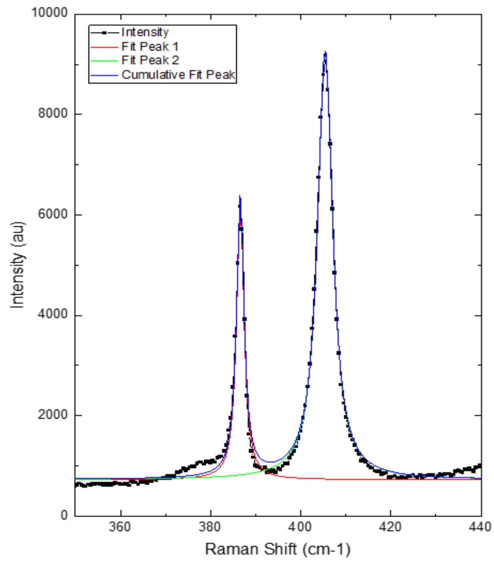

Fig S3: Raman spectroscopic measurement on Monolayer MoS_2

Fig. S3 shows the Raman spectra of monolayer MoS_2 (apart from that which is outside the hBN and is on SiO_2/Si). We observed E_{2g} and A_{1g} peaks at 386.59 cm^{-1} and 405.41 cm^{-1}, respectively. The difference between the peak positions is around 18 $cm^{-1,}$ implying its monolayer nature.

Estimation of intrinsic n-type doping in the MoS_2 channel:

The intrinsic doping of the MoS_2 channel is calculated using the gate voltage shift as shown in Fig. 1f of the main paper.

$$n = C\Delta V_g / e \qquad \text{(S1)}$$

$$C = \frac{k\varepsilon_0}{d} \qquad \text{(S2)}$$

$$n = \frac{k\varepsilon_0 \Delta V_g}{300e} \qquad \text{(S3)}$$

Here, C is the capacitance, e is the electronic charge, ΔV_g is the shift in gate voltage, K is the dielectric constant, and ε_0 is the electric permittivity of the hBN layer, including SiO_2.

In our case, the model assumes a parallel-plate geometry and uniform dielectric, applicable to monolayer MoS_2 placed on atomically flat hBN on SiO_2. The dielectric permittivity of both components (hBN on SiO_2) is nearly equal (4) for this estimation.

Hence, the total thickness of the parallel capacitor is calculated by adding the individual thickness of the hBN layer (15 nm) and SiO_2 (285 nm)/Si.

Considering the Value, K=4, $\varepsilon_0 = 8.854 \times 10^{-12}\ \mathrm{Fm^{-1}}$, d=300 nm & $\Delta V_g = 12$ V.

at T=222 K

$$n = 1.45\times10^{16}\ /\mathrm{m}^2$$

$$= 1.45\times10^{12}\ /\mathrm{cm}^2$$

at T=143 K

$$n = 0.72 \times 10^{16}\ /\mathrm{m}^2$$

$$= 0.72 \times 10^{12}\ /\mathrm{cm}^2$$