

Accumulation-mode p-channel MOSFETs on phosphorous-doped n-type diamond

Wen Zhao, Satoshi Koizumi*, and Meiyong Liao*

Abstract—P-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) are demonstrated on phosphorus-doped n-type diamond epilayers. The p-channel nature is due to the surface conductivity based on hydrogenated termination on the n-type diamond surface. The MOSFET exhibit normally-off properties with accumulation mode and show a threshold of -1.1 V and an on/off ratio of 10^9 . The maximum drain current is around 1.8 mA/mm and the transconductance is 0.4 mS/mm, which decreases as the phosphorus concentration increases in the n-type diamond epilayer. The demonstration of p-channel MOSFETs on the n-type diamond epilayer facilitates the development of complementary MOS (CMOS) circuits on a single diamond wafer.

Index Terms—N-type diamond, p-channel MOSFET, Surface Conductivity

I. INTRODUCTION

Diamond, with its exceptional material properties such as ultra-wide bandgap, high breakdown voltage, and high thermal conductivity, presents a promising platform for next-generation electronic devices [1-4]. The development of diamond electronics has been directing toward two main topics, high-power, high-voltage, and high-frequency electronic devices [5, 6] and integrated circuits [7, 8] consuming less energy and reliable under extreme conditions. Diamond metal-oxide-semiconductor field-effect transistors (MOSFETs) based on surface conductivity have been mostly concentrated and exciting progress has been achieved, such as in power handling and blocking voltage boosting [6, 9], frequency escalating [10, 11], and thermal stability improvement [12, 13].

To enable diamond-based integrated circuits, complementary metal-oxide-semiconductors (CMOS) are desirable for efficient power management, which requires both p-type and n-type channel conductivities as those for silicon microelectronics. P-channel diamond MOSFETs have been extensively investigated either on hydrogenated diamond surface or boron-doped diamond [11, 14, 15]. By combining surface conductivity p-channel diamond MOSFET with n-channel GaN FET, complementary power amplifiers were proposed and developed [16]. Such a hybrid technique represents a promising method for certain applications

considering the difficulty in obtaining n-type diamond. Recently, we demonstrated n-channel MOSFETs on phosphorus-doped n-type diamond epilayer [17]. From the viewpoint of integrated circuits with numerous FETs, CMOS on the same diamond wafer is the extreme pursuit. A sophisticated p-channel diamond MOSFET was reported on an n-type diamond epilayer with a heavily boron-doped p⁺ layer as the source (S) and drain (D) contacts and an OH surface termination under the gate (G) dielectric oxide. This p-channel MOSFET was claimed to be inversion type [18].

In this work, we realize the p-channel MOSFETs on hydrogen (H)-terminated surface fabricated on phosphorus-doped n-type diamond epilayers. Both the S and D contacts and gate dielectric oxide are fabricated on the H-terminated diamond surface. The MOSFETs exhibit a normally-off nature operated in accumulation mode.

II. EXPERIMENTAL

A. N-type Diamond Epilayers Growth

The p-channel MOSFETs were fabricated on lightly phosphorus-doped n-type diamond epilayers grown on type-Ib (111) oriented high-pressure high-temperature (HPHT) diamond substrates by using a microwave plasma assisted chemical vapor deposition (MPCVD) [19]. The surface of the as-grown n-type diamond epilayers were hydrogenated. Two n-type diamond epilayers with different phosphorus concentrations of $[P] \sim 10^{16} \text{ cm}^{-3}$ and $[P] \sim 10^{17} \text{ cm}^{-3}$ were utilized in this study. The thickness of the n-type layer was about 2.2 μm . The n-type diamond epilayers were exposed to air for a couple of days, as those done for intrinsic diamond epilayers for the formation of 2-dimensional hole gas (2DHG) [20].

B. Device Fabrication and Measurements

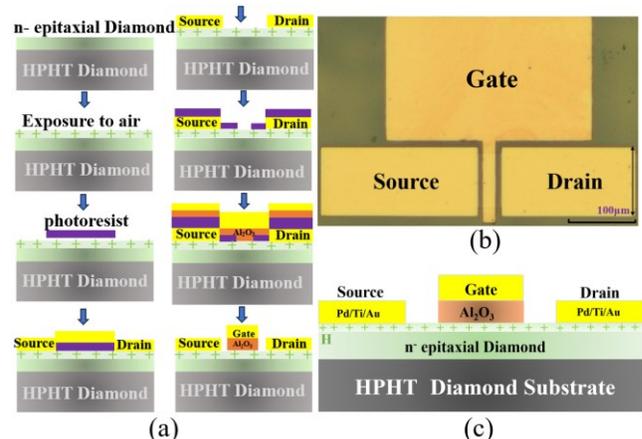


Fig.1 (a) Fabrication procedure for the diamond MOSFETs; (b) Optical image of the fabricated transistor with 100 μm gate length; (c) Schematic cross-section of the p-channel MOSFET.

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The fabrication process of the MOSFETs on the n-type diamond epilayers with H-termination is similar to those on the hydrogenated diamond surface with 2DHG [20, 21], as shown in Fig. 1(a). A laser photolithographic technique was used for the MOSFETs fabrication. A 10 nm-thick Pd layer is directly contacted to the H-terminated diamond surface, followed by 10 nm-thick Ti and 80 nm-thick Au, to form the Ohmic contact as the source and drain electrodes. Consequently, oxygen plasma was used to isolate the devices by forming mesa structure. Then, an Al₂O₃ layer with a thickness of 27 nm was grown by an atomic layer deposition (ALD) at 400 K on the gate area defined by the laser lithography. Finally, a 10 nm-thick Ti layer covered by a 60 nm thick Au layer was deposited on the Al₂O₃ layer. The gate length is 16 μm and the width is 80 μm. The source-gate and drain-gate gaps are both 10 μm. Fig.1(b) illustrates the optical image of a typical MOSFET and Fig.1 (c) is the cross-section structure of the MOSFET.

The current-voltage (I-V) characteristics were measured by a semiconductor analyzer in the air at room temperature by using a probe station with a current noise level less than 10⁻¹³ pA.

III. RESULTS AND DISCUSSION

It was confirmed that there was an electrical current flow on the H-terminated n-type diamond epilayer between the source and drain electrodes before the gate formation. The current level from the epilayer with [P]~10¹⁶cm⁻³ is higher than that of the epilayer with [P]~10¹⁷cm⁻³, implying the depletion of 2DHG hole by electrons from the n-type diamond epilayers. But the current level (10⁻⁵ A) of the H-terminated n-type

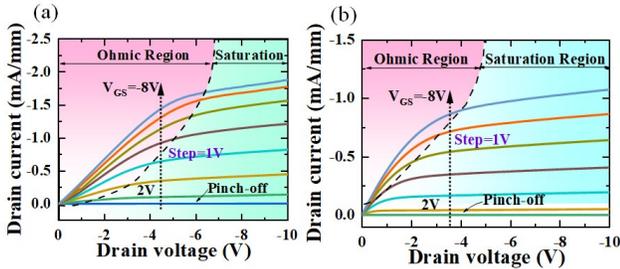


Fig.2 I_{DS}-V_{DS} output characteristic curve of MOSFETs fabricated on the n-type epilayer with (a) [P]~ 10¹⁶cm⁻³ and (b) 10¹⁷cm⁻³. The gate length is 16 μm, width 80 μm, and the source-gate and drain-gate gaps are both 10 μm.

diamond is ~two orders of magnitude lower than that (10⁻³A) on the intrinsic diamond layer with H-termination. We investigate the drain current (I_{DS}) vs drain voltage (V_{DS}) characteristics of the MOSFETs fabricated on the diamond epilayers with different phosphorous concentrations by varying the gate voltage (V_{GS}) from -8 V to 2 V with a step of 1 V, as shown in Fig.2. The obtained results indicate that the drain currents are well modulated by the gate voltage. All the MOSFETs have obvious p-type conductivity and pinch-off characteristics. The I_{DS} at V_{DS}=-10 V and V_{GS}= -8V is around 1.8 mA/mm for [P]~10¹⁶cm⁻³ (Fig.2a), which is reduced to 1.1 mA/mm for [P]~10¹⁷cm⁻³ (Fig.2b). The on-resistance is around 301Ω·mm and 360 Ω·mm, for [P]~10¹⁶cm⁻³ and 10¹⁷cm⁻³, respectively. Therefore, the higher [P] in the n-type diamond epilayer leads to partial depletion of holes on the surface channel. Considering that the Ohmic contacts were formed on the H-terminated

diamond surface, the MOSFETs fabricated on the n-type diamond epilayers show an accumulation behavior.

The fabricated MOSFETs on the n-type diamond epilayer for [P]~ 10¹⁶cm⁻³ show a normally-off behavior, as disclosed in the transfer properties of I_{DS} vs V_{GS} at V_{DS}= -8 V in Fig. 3(a). The threshold voltage V_{th} is around -1.1 V. The V_{th} varies with the measurement history due to the trap states at the interface of Al₂O₃/diamond or in the Al₂O₃ layer[22]. Taking into account

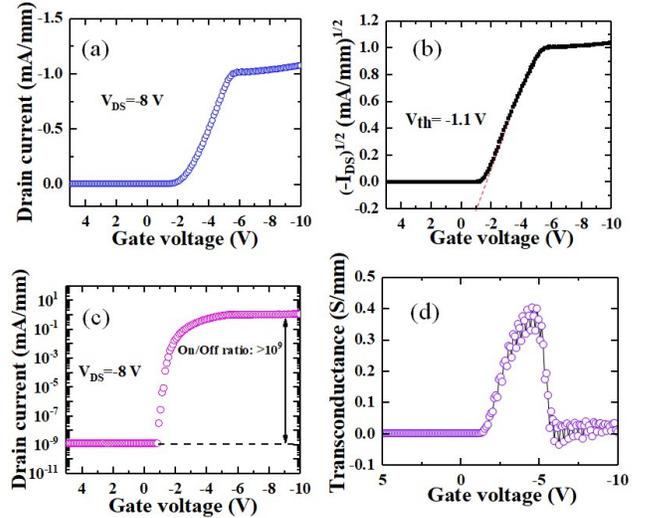


Fig.3 The transfer characteristics of diamond MOSFET at gate drain voltage of -8 V on the n-type layer with [P]~ 10¹⁶cm⁻³ (a) Drain current vs gate voltage; (b) (-I_{DS})^{1/2} vs gate voltage; (c) log scale of drain current vs gate voltage, and (d) transconductance.

the facts: (1) the appearance of electrical conductivity of the H-terminated surface that is over three orders of magnitude higher than that of the lightly phosphorous-doped n-type diamond epilayer itself with an oxidized surface [23], and (2) the Ohmic contact properties of the Pd/Ti/Au electrode on the H-terminated surface, the present MOSFETs on the H-terminated n-type diamond layer exhibit the similar electrical behavior as those on H-terminated intrinsic diamond [21, 22]. The fabricated MOSFETs show an on/off ratio over 10⁹, as shown in Fig. 3 (c). The subthreshold swing is around 120 mV/dec. The maximum transconductance g_{max} value is around 0.4 mS/mm, as disclosed in Fig.3(d). The field-effect

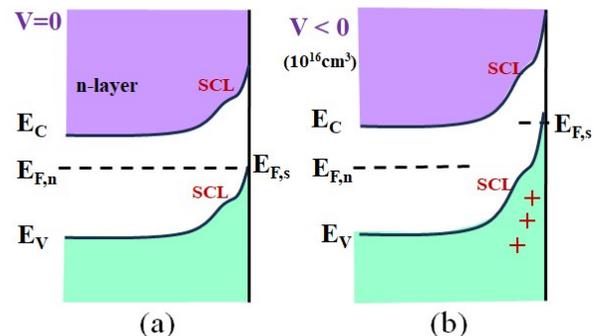


Fig.4 Energy band diagrams when applying (a) V=0V; (b) V<0V, at the density of 10¹⁶cm⁻³.

hole mobility μ_{eff} calculated by the quadratic model [20] is around $20 \text{ cm}^2/\text{V}\cdot\text{s}$.

The formation mechanism of p-channel conductivity on the hydrogenated n-type diamond surface is still under investigation. Based on the above experimental data, we speculate that the H-termination forms a p-type surface conductive layer (SCL) after the exposure to air, which forms a pn junction near the n-type diamond surface. At zero gate bias, the surface holes are partially depleted with a surface upward band bending. The deposition of ALD- Al_2O_3 further depletes the holes on the diamond surface, which eventually leads to the normally-off operation of the MOSFETs here[22]. As the negative gate biases are large enough, the surface Fermi level bends upward more strongly and holes accumulate near the surface, as illustrated in Fig.4. The increase in the phosphorous concentration in the diamond epilayer just depletes more holes on the surface and changes the surface band upward strength. The drain current level of the p-channel MOSFETs is five orders of magnitude higher than those of n-channel ones fabricated on the n-type diamond epilayer at room temperature. Nevertheless, the conductivity difference becomes only 10 times at 573 K. The demonstration of high-temperature thermal stability for the p-channel MOSFETs based on surface conductivity up to 673 K provides a promising potential for high-temperature diamond CMOS on the same n-type diamond epilayer by using the planar fabrication process.

IV. CONCLUSIONS

We demonstrated p-channel MOSFETs on phosphorous-doped n-type diamond epilayers with hydrogen termination on the surface. The resulting MOSFETs exhibited normally-off behavior and were operated in accumulation mode. The drain current was around 1.8 mA/mm at $V_{\text{GS}}=-8 \text{ V}$ and $V_{\text{DS}}=-10 \text{ V}$ and the maximum transconductance was around 0.4 mS/mm . The fabrication of p-channel MOSFETs on the n-type diamond epilayer provides a facile route for the development of high-temperature CMOS working at high temperatures.

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