***A review paper celebrating the distingushed career of Prof. Yasuo Koide***

# Hydrogen-terminated and oxygen-terminated diamond metal-oxide-semiconductor field-effect transistors

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**Abstract**

Extensive research has been conducted on wide-bandgap semiconductor diamond for the advancement of high-power, high-frequency, and high-temperature electronic devices. The author has established long-term collaboration with Prof. Koide, focusing on producing *p*-type hydrogen-terminated diamond (H-diamond) and boron-doped oxygen-terminated diamond (O-diamond) based metal-oxide-semiconductor field-effect transistors (MOSFETs). This paper presents our primary research findings on the fabrication of enhancement-mode H-diamond MOSFETs and MOSFET logic circuits, as well as the high-temperature operation of the boron-doped O-diamond MOSFETs.

## 1. Introduction

To further develop high-power, high-frequency, and high-temperature complementary metal-oxide-semiconductor (CMOS) devices, it is necessary to develop a semiconductor with a large band gap energy, high breakdown field, high carrier mobility, high saturation velocity, and high thermal conductivity. Diamond emerges as a promising candidate for fabricating high-performance CMOS devices [1, 2].

Recently, significant advancements have been made in *p*-type hydrogen-terminated diamond (H-diamond) and boron-doped oxygen-terminated diamond (O-diamond) channel layer-based MOS field-effect transistors (MOSFETs) [3-12]. Fig. 1(a) depicts a schematic diagram illustrating the accumulation of holes in the H-diamond channel layer. Two-dimensional hole gases (2DHGs) present on the surface of the H-diamond channel layer with a sheet hole density of $10^{12}$~$10^{14}$ $cm^{-2}$ [14]. The accumulation of 2DHGs relies on the existence of surface carbon-hydrogen bonds and negatively charged acceptors. The H-diamond-based MOSFETs have demonstrated remarkable electrical characteristics, including a maximum drain current ($I_{D,max}$) of 1.35 A/mm [3], a maximum extrinsic transconductance ($g_{m,max}$) of 206 mS/mm [3], a cut-off frequency of 70 GHz [7], and a robust breakdown voltage of 4266 V [13].

For the *p*-type boron-doped O-diamond channel layer, the activation energy of boron-doping (0.37 eV) notably surpasses the thermal energy (0.026 eV) at room temperature (RT) [Fig. 1(b)]. Consequently, the hole density is relatively low, resulting in the MOSFETs on the boron-doped O-diamond demonstrating low current outputs [9, 10]. Nevertheless, due to no surface thermal sensitivity issue, it is expected that the O-diamond MOSFETs can operate effectively even under high-temperature conditions.

Previously, the authors have engaged in long-term collaborations with Prof. Koide,

focusing on fabricating *p*-type H-diamond and boron-doped O-diamond based MOSFETs. This paper will provide our primary research findings concerning the fabrication of enhancement-mode (E-mode) H-diamond MOSFETs and MOSFET logic circuits, as well as the high-temperature operation of the boron-doped O-diamond MOSFETs.

## 2. H-diamond MOSFETs

### 2.1 E-mode H-diamond MOSFETs

The conditions governing the operation of depletion-mode (D-mode) and E-mode H-diamond MOSFETs have been clarified [15]. Two essential conditions have been identified for the fabrication of E-mode H-diamond MOSFETs: the utilization of a bilayer gate oxide prepared through atomic layer deposition (ALD) and sputtering deposition (SD) techniques, coupled with annealing in the temperature range of 150-350 ℃ [16-18]. Meanwhile, the ALD-oxide/ALD-oxide bilayer and single evaporated oxide insulator on the H-diamond can also lead to the E-mode characteristics for the MOSFETs [19, 20]. On the other hand, despite the existence of an annealing step in the fabrication process of H-diamond MOSFETs with a single ALD-$Al_2O_3$ layer as a gate oxide, these MOSFETs continue to exhibit D-mode characteristics [5].

The transition to E-mode behavior in the H-diamond MOSFETs induced by annealing and SD-oxide/ALD-oxide bilayer conditions is attributed to a modification in the transfer doping of the channel layer [15]. Initially, the presence of negative charges at the ALD-oxide/H-diamond interface leads to hole accumulation in the H-diamond channel layer, resulting in the D-mode characteristics in the MOSFETs before annealing. Subsequent annealing leads to the elimination of the negative acceptors or the introduction of compensatory positive charges within the oxide insulator [15]. This

process significantly reduces the hole density in the H-diamond channel layer, thereby causing the MOSFETs to exhibit E-mode characteristics.

Figures 2(a) and 2(c) depict scanning electron microscope (SEM) images of the D-mode ALD-$Al_2O_3$/H-diamond and E-mode SD-$LaAlO_3$/ALD-$Al_2O_3$/H-diamond MOSFETs, respectively [5]. Schematic cross-sectional structures of these devices are presented in Figs. 2(b) and 2(d), respectively. The distance between the source and drain electrodes for both the $Al_2O_3$/H-diamond and $LaAlO_3$/$Al_2O_3$/H-diamond MOSFETs is kept at 5.5 μm. However, their gate length ($L_G$) values differ, with the former at 3.0 μm and the latter at 2.0 μm. The interspace lengths between source and gate electrodes ($L_{S\text{-}G}$) and between drain and gate electrodes ($L_{D\text{-}G}$) for the $Al_2O_3$/H-diamond MOSFET are 1.2 and 1.3 μm, respectively, while those for the $LaAlO_3$/$Al_2O_3$/H-diamond MOSFET are 1.5 and 2.0 μm, respectively. Despite both MOSFETs being designed with the same device structures, variations in the $L_G$, $L_{S\text{-}G}$, and $L_{D\text{-}G}$ are observed. These differences are potentially attributed to the positioning accuracy of the laser lithography system, estimated to be around ±1.0 μm.

Figures 3(a) and 3(b) display the drain-source current ($I_D$) versus drain-source voltage ($V_D$) characteristics for the $Al_2O_3$/H-diamond and $LaAlO_3$/$Al_2O_3$/H-diamond MOSFETs, respectively. The gate-to-source voltage ($V_{GS}$) for both MOSFETs was varied from -10.0 to 6.0 V in increments of +1.0 V, revealing distinct pinch-off and *p*-channel characteristics in each case. The $I_{D,max}$ values for the $Al_2O_3$/H-diamond and $LaAlO_3$/$Al_2O_3$/H-diamond MOSFETs are recorded as -112.4 and -69.3 mA/mm, respectively. Normalized on-resistance ($R_{ON}$) values by the gate width ($W_G$) at $V_{GS}$= -10.0 V are calculated as 56.0 and 63.5 Ω mm for the two devices, respectively. Threshold voltage ($V_{TH}$) values [Fig. 3(c)] are determined to be 5.3 ±0.1 and -5.0 ±0.1 V

for the $Al_2O_3$/H-diamond and $LaAlO_3/Al_2O_3$/H-diamond MOSFETs, respectively. Consequently, the $Al_2O_3$/H-diamond and $LaAlO_3/Al_2O_3$/H-diamond MOSFETs operate with D-mode and E-mode characteristics, respectively. Despite the smaller $I_{D,max}$ of the E-mode MOSFET compared to the D-mode MOSFET, their $g_{m,max}$ values are nearly identical at 17 mS/mm [Fig. 3(d)]. This suggests that the current D/E-mode control technique does not compromise the performance of the H-diamond MOSFETs.

**2.2 E-mode H-diamond MOSFET NOT logic circuits [5]**

Figures 4(a) and 4(b) depict the top view and schematic diagram of the H-diamond MOSFET NOT logic circuit, respectively. In this setup, $V_{in}$, $V_{out}$, and $V_{DD}$ represent the input voltage, output voltage, and supply voltage, respectively. The NOT logic circuit comprises a D-mode ALD-$Al_2O_3$/H-diamond MOSFET serving as the load device and an E-mode SD-$LaAlO_3$/ALD-$Al_2O_3$/H-diamond MOSFET as the driver device. Fig. 4(c) illustrates the voltage transfer characteristics (VTCs) of the H-diamond NOT logic circuit as $V_{DD}$ varies from -5.0 V to -25.0 V, revealing distinctive inversion properties inherent to the NOT logic circuit. In operation, when $V_{in}$ is at 0 V, the E-mode $LaAlO_3/Al_2O_3$/H-diamond MOSFET remains in the off-state, leading to $V_{out}$ closely tracking $V_{DD}$. Conversely, with $V_{in}$ set at -10.0 V, the E-mode MOSFET switches on, resulting in $V_{out}$ near ground level. Consequently, when $V_{in}$ carries a low logical 0 signal, $V_{out}$ responds with a high logical 1 signal. The gain curve, defined by $-dV_{out}/dV_{in}$, is presented in Figure 4(d). The maximum gain value increases from 1.2 to 26.1 as $V_{DD}$ transitions from -5.0 to -25.0 V, showcasing the amplification capabilities of the circuit under varying supply voltage conditions.

**2.3 E-mode H-diamond MOSFET NOR logic circuits [21]**

Figures 5(a) and 5(b) display the top view and schematic diagram of the

H-diamond MOSFET NOR logic circuit, respectively. This NOR logic circuit configuration consists of two E-mode SD-$LaAlO_3$/ALD-$Al_2O_3$/H-diamond MOSFETs and a load resistor ($R_L$). $V_{in1}$ and $V_{in2}$ are representative of the two input voltages, while $V_{out}$ and $V_{DD}$ denote the output voltage and supply voltage, respectively. The $W_G$ and $L_G$ for the E-mode MOSFET are maintained at 100.0 and 2.0 μm, respectively. The interspaces between different electrodes for $V_{in}$-to-ground, $V_{in}$-to-$V_{out}$, and $V_{in}$-to-$V_{DD}$ are specified as 1.5, 2.0, and 26.0 μm, respectively.

Figure 5(c) illustrates $V_{out}$ as functions of $V_{in1}$ and $V_{in2}$ for the as-fabricated E-mode H-diamond MOSFET NOR logic circuit. The logic circuit exhibits four distinct states corresponding to logical (1, 1), logical (1, 0), logical (0, 1), and logical (0, 0) input voltage combinations. Each input voltage state is measured over a duration of 60 seconds. When both $V_{in1}$ and $V_{in2}$ are set to -10.0 V, representing the logical (1, 1) state, both E-mode MOSFETs are activated. This results in a substantial current flow through the load resistor, causing a significant drop in $V_{DD}$. Consequently, $V_{out}$ converges near 0 V, indicating a logical 0 state. When one $V_{in}$ is set to -10.0 V and the other to 0 V, corresponding to logical (1, 0) or (0, 1) states, only one E-mode MOSFET enters the on-state. $V_{out}$ again approaches 0 V, reflecting a logical 0 state. When both $V_{in1}$ and $V_{in2}$ are set to 0 V, representing the logical (0, 0) state, both E-mode MOSFETs remain off-state, resulting in no current flow through the load resistor. Consequently, $V_{out}$ aligns closely with $V_{DD}$ at -10.0 V, indicating a logical 1 state. In summary, when one or both input voltages are “high” signals, the output voltages respond with “low” signals, while both input voltages being “low” signals prompt $V_{out}$ to exhibit a “high” signal. These observations confirm that the logic circuits are operating with NOR characteristics.

Figures 6(a) and 6(b) present the electrical properties of the H-diamond NOR logic

circuit following annealing at 300 °C and 400 °C, respectively. Following the 300 °C annealing process, the logic circuit continues to exhibit good operation and maintains its NOR characteristics. However, after annealing at 400 °C, the logical characteristics are damaged. When both input voltages are set to 0 V, resulting in the logical (1, 1) state, both E-mode MOSFETs remain in the off-state, causing $V_{out}$ to approach the $V_{DD}$ of -10.0 V. Conversely, when one or both input voltages are at -10.0 V, representing the logical (1, 0) or (0, 1) states, at least one E-mode MOSFET enters the on-state. This leads to $V_{out}$ ranging between -4.1 to -7.7 V. Therefore, after annealing at 400°C, there is an increase in the absolute $V_{out}$. This is possibly attributed to the degradation of the H-diamond MOSFETs at high annealing temperature [22].

## 3. Boron-doped O-diamond MOSFETs

Due to the exceptional thermal stability of the boron-doped O-diamond electronic devices, our attention was directed towards producing high-performance O-diamond MOSFETs. We focused on investigating their performance through ex-situ and in-situ annealing processes.

### 3.1 O-diamond MOSFETs after ex-situ annealing [23]

Figures 7(a) and 7(b) display an SEM image and a schematic diagram of the boron-doped O-diamond MOSFET, respectively. The inset figure in Fig. 7(a) offers a magnified view of the blue square area. The $L_G$, $L_{S\text{-}G}$, and $L_{D\text{-}G}$ are measured at 7.0, 9.9, and 17.4 μm, respectively. Additionally, the diameter of the circular-shaped drain electrode is determined to be 597.8 μm.

Figures 7(c) and 7(d) depict the $I_D$–$V_D$ characteristics for the as-fabricated and ex-situ 500 °C-annealed boron-doped O-diamond MOSFETs, respectively. The annealing time was 30 min. The $V_{GS}$ values for both devices range from -16.0 V to 33.0 V in

increments of +1.0 V. Both MOSFETs exhibit *p*-type channel characteristics and showcase clear saturation and pinch-off properties. The $I_{D,max}$ values are recorded as -0.49 and -0.6 mA/mm for the B-diamond MOSFETs before and after ex-situ annealing, respectively. Their $R_{ON}$ values are measured at 26.9 and 12.8 kΩ mm, respectively, which are much higher than those of the H-diamond MOSFETs [5]. The $V_{TH}$ and $g_m$ for the O-diamond MOSFETs are illustrated in Figs. 8(a) and 8(b) respectively. The $V_{TH}$ values for the as-fabricated and ex-situ 500 °C-annealed O-diamond MOSFETs are determined to be 63.2 V and 56.1 V, respectively. For both the as-fabricated and ex-situ 500 °C-annealed B-diamond MOSFETs, the $g_{m,max}$ values are determined to be 18.7 and 21.4 μS/mm, respectively.

### 3.2 O-diamond MOSFETs at in-situ annealing [24]

Figures 9(a) and 9(b) display a SEM image and a schematic diagram of the O-diamond MOSFET, respectively. The drain electrode has a diameter of 299.6 μm, allowing the calculation of the $W_G$ as 940.7 μm. The $L_G$ is specified as 2.6 μm, with interspatial lengths for the $L_{S\text{-}G}$ and $L_{D\text{-}G}$ electrodes noted as 5.8 μm and 4.6 μm, respectively. In contrast to the O-diamond MOSFETs in session 3.1, a 20 nm-thick layer of $Al_2O_3$ film was applied to cover the sample surface. This $Al_2O_3$ cover layer serves to eliminate surrounding environmental effects and edge leakage of electrodes for the O-diamond MOSFETs, thereby enhancing their reliability and device performance.

Figures 10(a) and 10(b) illustrate the $I_D$-$V_D$ characteristics for the O-diamond MOSFETs operating at RT and 300 °C, respectively. The $V_{GS}$ ranges from -20.0 to 78.0 V in increments of +2.0 V. These figures demonstrate efficient operations with *p*-type characteristics. The $I_{D,max}$ for the O-diamond MOSFET operating at RT is recorded as -1.2 mA/mm. Despite the lower boron doping levels and acceptor concentrations

(approximately $10^{16}$ $cm^{-3}$ and 6.0 × $10^{14}$ $cm^{-3}$) [24] in this O-diamond channel layer compared to the previous one (approximately $10^{17}$ $cm^{-3}$ and 2.9 × $10^{16}$ $cm^{-3}$) [23], the $I_{D,max}$ exceeds two times the reported value of -0.49 mA/mm. This improvement is likely due to the reduction in $L_G$, $L_{S-G}$, and $L_{D-G}$, leading to a decrease in $R_{ON}$ from 26.9 kΩ mm to 9.6 kΩ mm. At an operating temperature of 300°C, the $I_{D,max}$ experiences a substantial increase to -10.9 mA/mm, while the $R_{ON}$ decreases to 1.1 kΩ mm due to the enhanced activation of boron dopants at higher temperatures. Figures 10(c) and 10(d) depict the $I_D$–$V_{GS}$ characteristics for the O-diamond MOSFETs operating at RT and 300°C, respectively. Through linear extrapolation, the $V_{TH}$ values for the MOSFETs at RT and 300°C are determined to be 63.8 ± 0.1 V and 31.2 ± 0.1 V, respectively. The on/off ratios for both MOSFETs exceed $10^9$, marking the highest values reported to date.

## 4. Conclusions

This paper provides a summary of key research outcomes concerning the fabrication of E-mode H-diamond MOSFETs and logic circuits, along with insights into the high-temperature performance of boron-doped O-diamond MOSFETs. The operational parameters for D-/E-mode H-diamond MOSFETs have been clarified, leading to the successful fabrication of D-/E-mode H-diamond MOSFET logic circuits. Notably, the E-mode H-diamond MOSFET NOT and NOR logic circuits exhibit robust logical properties. Furthermore, the boron-doped O-diamond MOSFETs demonstrate favorable characteristics following ex-situ annealing at 500 ℃ and in-situ annealing at 300 ℃.

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**Disclosure Statement**

No potential conflict of interest was reported by the author.

**Notes on contributor**

Dr. *Jiangwei Liu* is currently a Principal Researcher at Semiconductor Defect Design Group of the National Institute for Materials Science (NIMS), Japan. He received his Ph. D. degree from the University of Tokyo in 2012. He worked as a postdoctoral researcher from 2012 to 2013 and as an ICYS Fellow from 2014 to 2016 at NIMS. He became a tenured Independent Scientist from Oct. 2016 and changed to the current position from April 2023. He is presently interested in wide bandgap semiconductors (mainly diamond) based electronic devices and semiconductor physics.

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**Figure captions**

**Figure 1.** (a) Schematic diagram for 2DHGs accumulation of the H-diamond channel layer and (b) activation energies for diamond with the boron-doping, phosphorus-doping, and nitrogen-doping.

**Figure 2.** (a) SEM images of the D-mode $Al_2O_3$/H-diamond and E-mode $LaAlO_3/Al_2O_3$/H-diamond MOSFETs, respectively. (b) and (d) Schematic cross-sectional structures of them, respectively.

**Figure 3.** (a) and (b) $I_D$-$V_D$ characteristics for the $Al_2O_3$/H-diamond and $LaAlO_3/Al_2O_3$/H-diamond MOSFETs, respectively. (c) and (d) $I_D$-$V_{GS}$ and $g_m$-$V_{GS}$ characteristics for both MOSFETs, respectively.

**Figure 4.** (a) Surface morphology for E-mode H-diamond MOSFET NOT logic circuit, (b) VTCs of the NOT logic circuit with the $V_{DD}$ changing from -5.0 to -25.0 V, and (c) the gain curve ($-dV_{out}/V_{in}$) derived from the VTCs.

**Figure 5.** (a) and (b) Top view and schematic diagram of the E-mode H-diamond MOSFET NOR logic circuit, respectively. (c) $V_{out}$ as functions of four $V_{in}$ states of logical (1, 1), logical (1, 0), logical (0, 1), and logical (0, 0) for the as-fabricated E-mode H-diamond MOSFET NOR logic circuit.

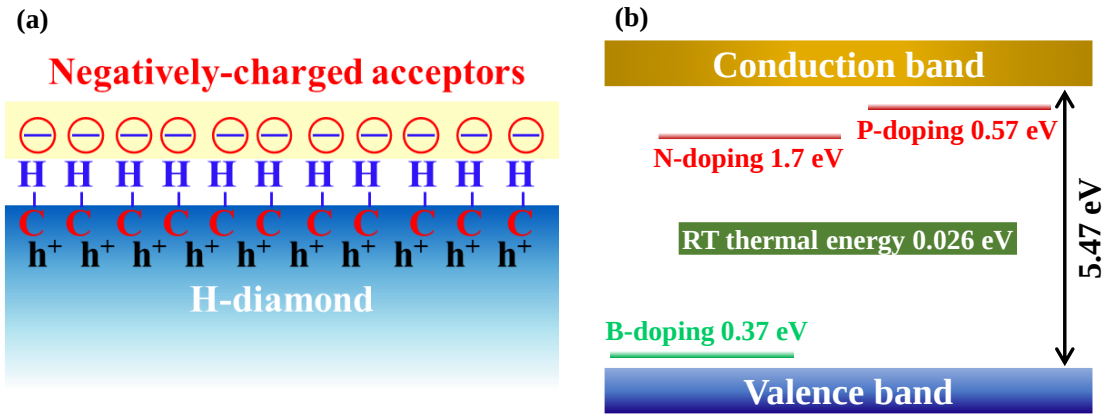
**Figure 6.** (a) and (b) $V_{out}$ as functions of input voltages for the E-mode H-diamond MOSFET NOR logic circuit after annealing at 300 and 400 ºC, respectively.

**Figure 7.** (a) SEM image and (b) schematic diagram of the boron-doped O-diamond MOSFET, respectively. (c) and (d) $I_D$–$V_D$ characteristics for as-fabricated and ex-situ 500 ºC-annealed O-diamond MOSFETs, respectively.

**Figure 8.** (a) $-\sqrt{|I_D|}$ and (b) $g_m$ as functions of $V_{GS}$ for the B-diamond MOSFETs, respectively.

**Figure 9.** (a) SEM image and (b) schematic diagram of the boron-doped O-diamond MOSFET, respectively. (c) and (d) $I_D$–$V_D$ characteristics for the O-diamond MOSFETs working at RT and in-situ 300 ºC annealing, respectively.

**Figure 10.** (a) and (b) $I_D$–$V_{GS}$ characteristics for the O-diamond MOSFETs working at RT and in-situ 300 ºC annealing, respectively. (c) and (d) $g_m$-$V_{GS}$ characteristics for the O-diamond MOSFETs working at RT and in-situ 300 ºC annealing, respectively.

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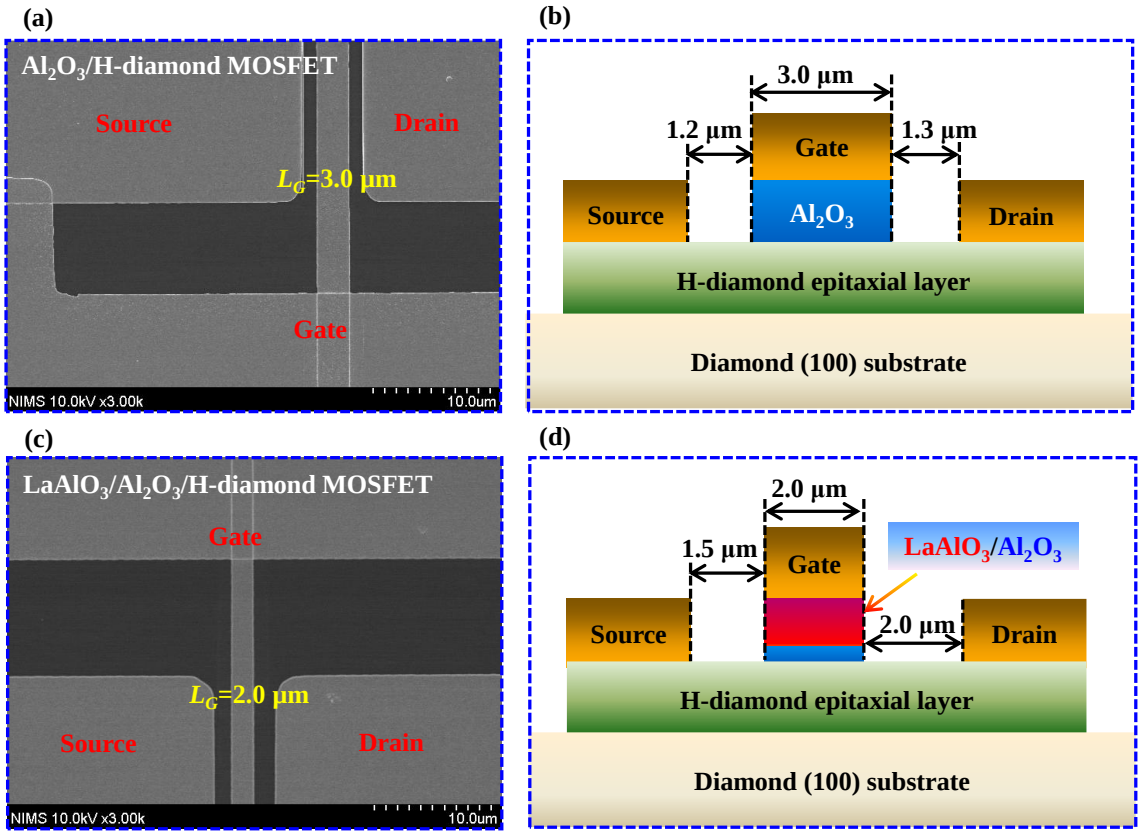


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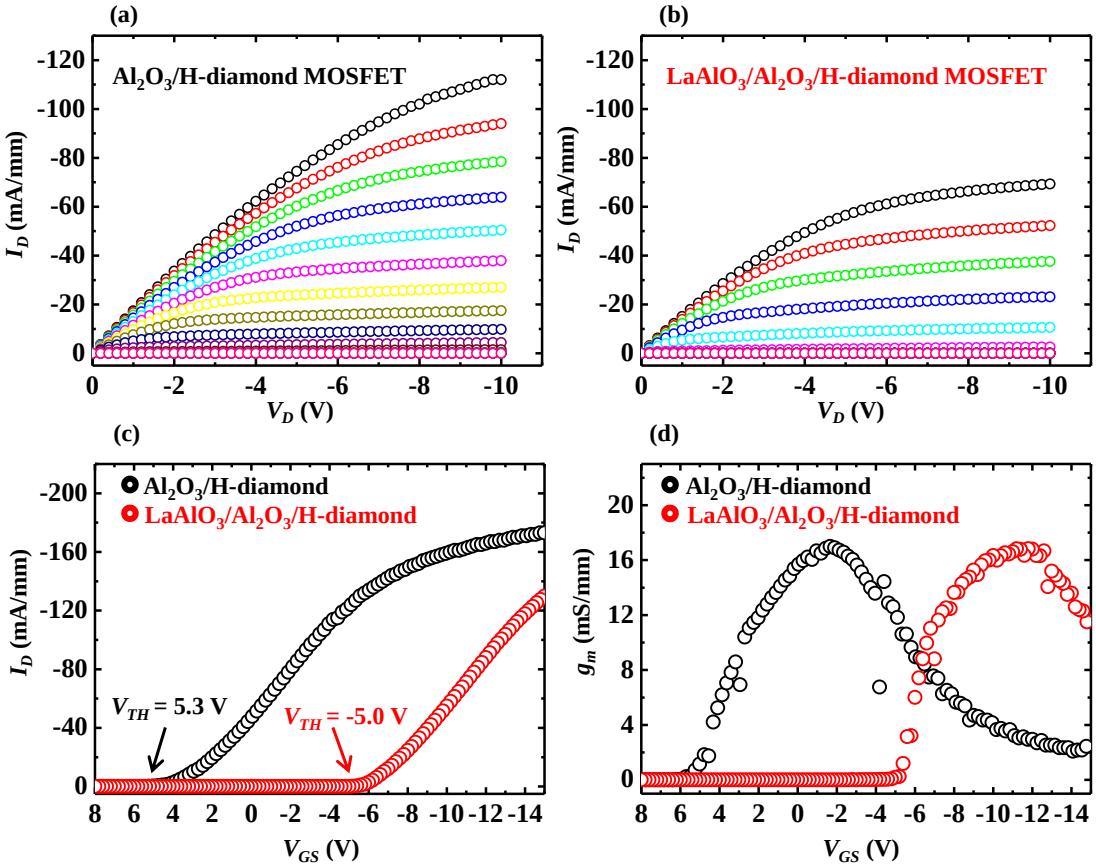


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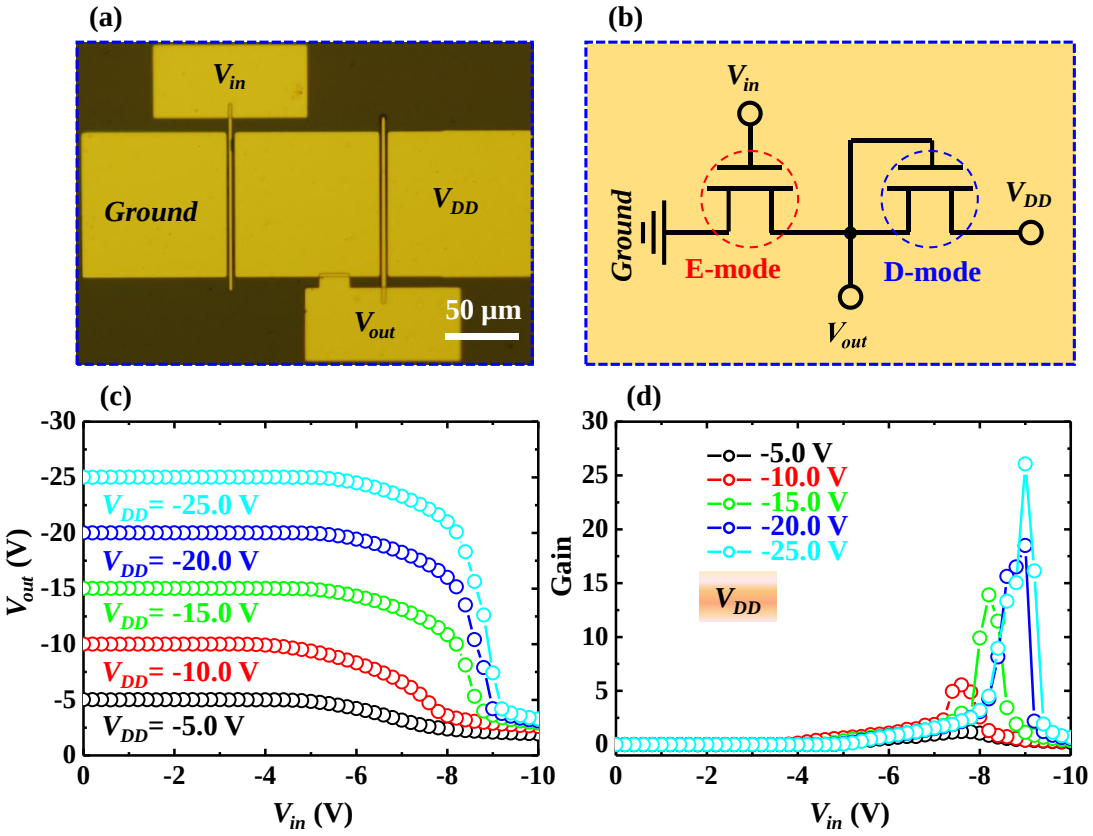


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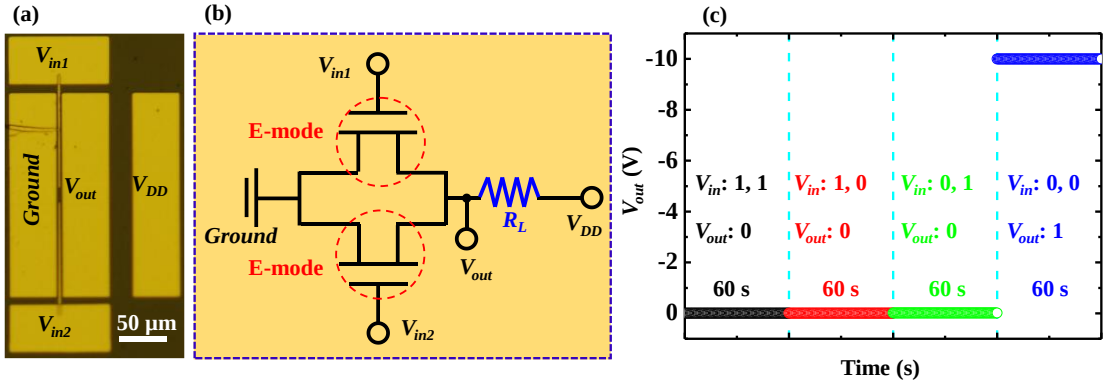


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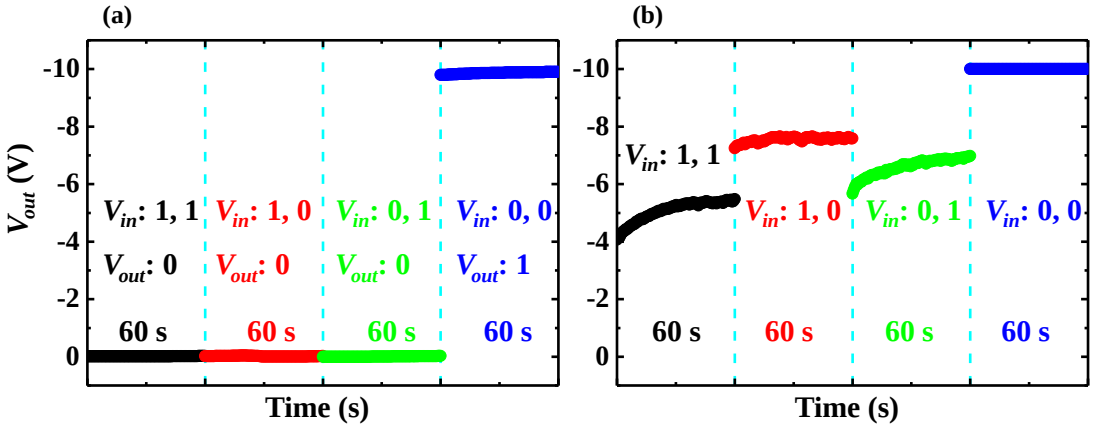


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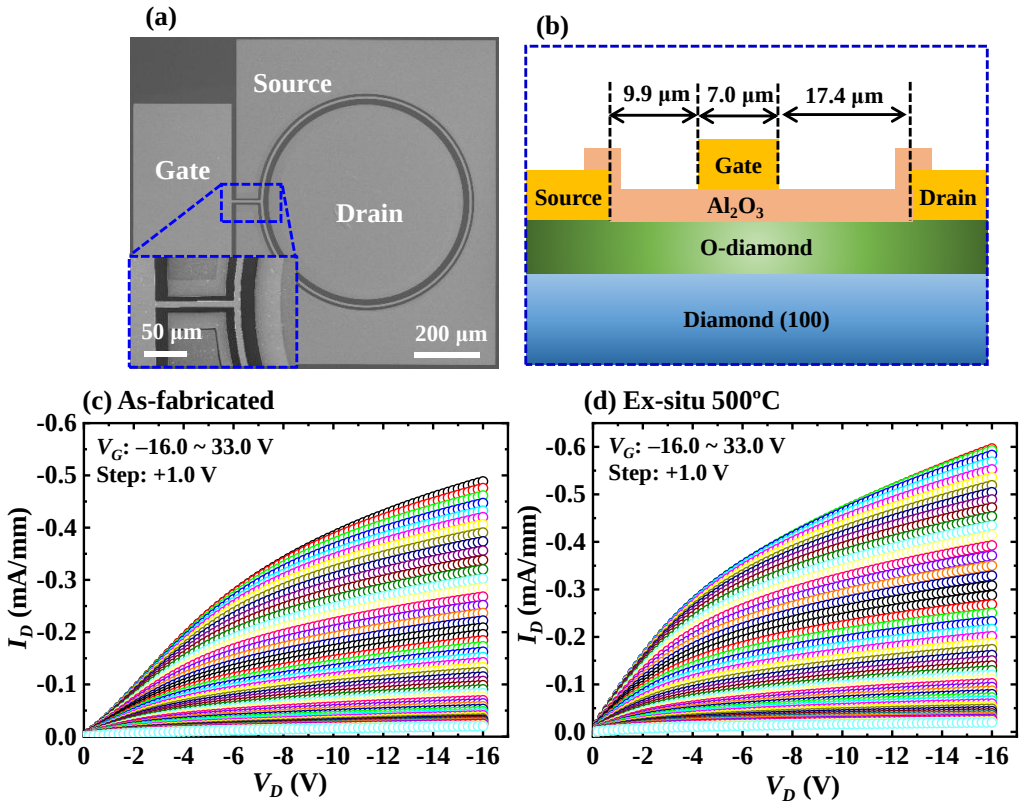


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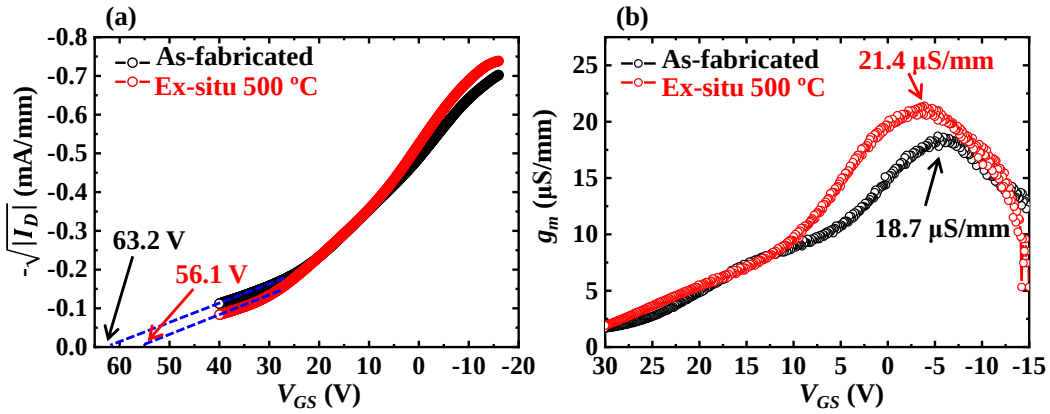
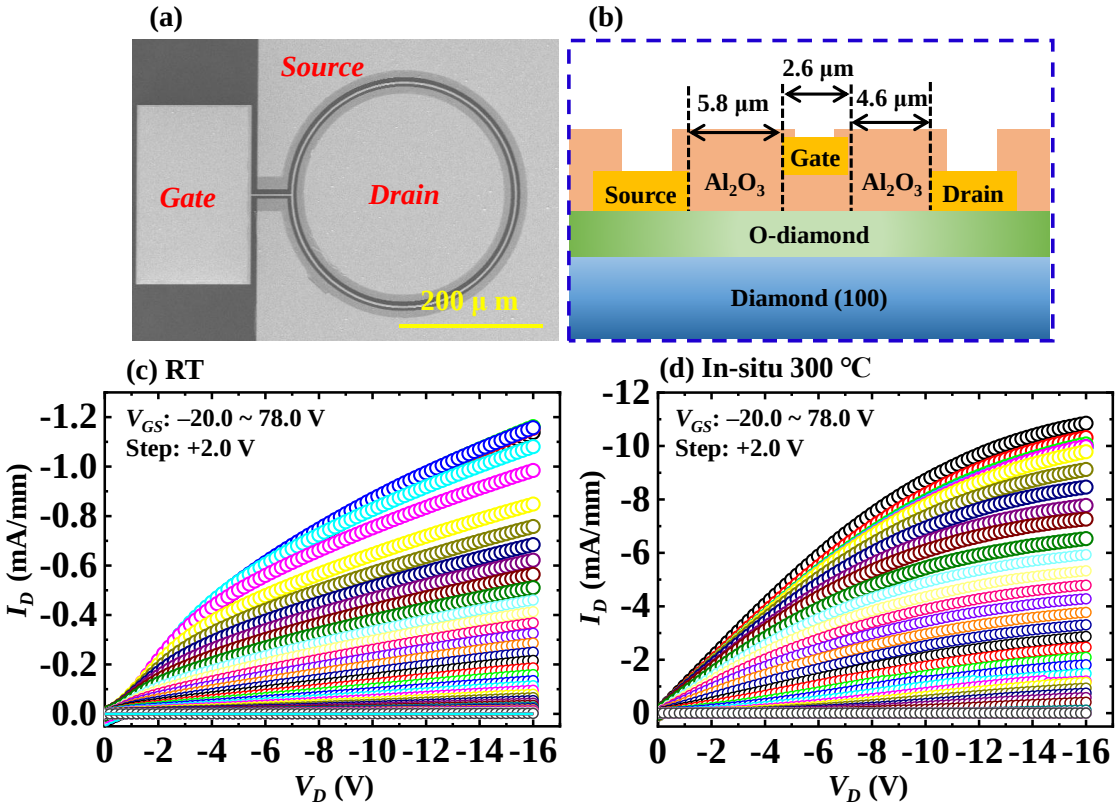
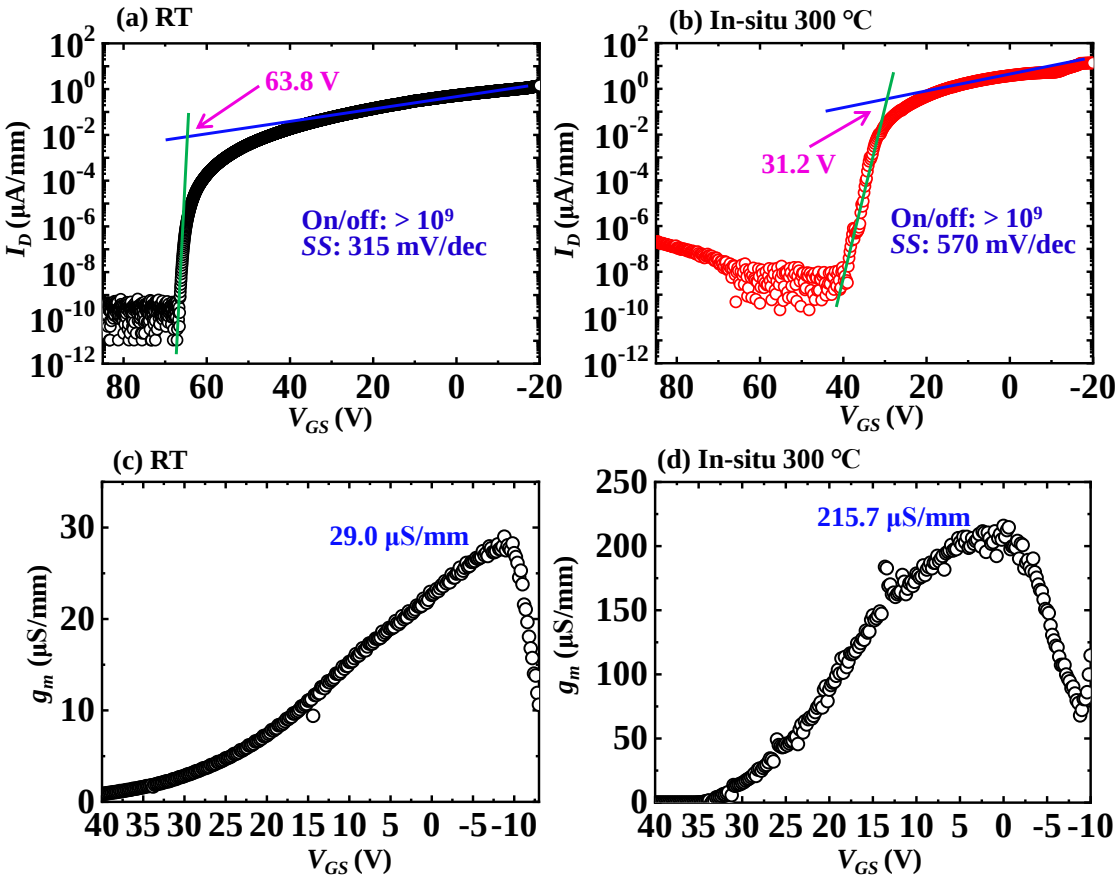



Liu *et al.*, Figure 8




Liu *et al.*, Figure 9




Liu *et al.*, Figure 10