

## Supplementary Materials

# Selective Manipulation and Tunneling Spectroscopy of Broken-Symmetry Quantum Hall States in a Hybrid-edge Quantum Point Contact

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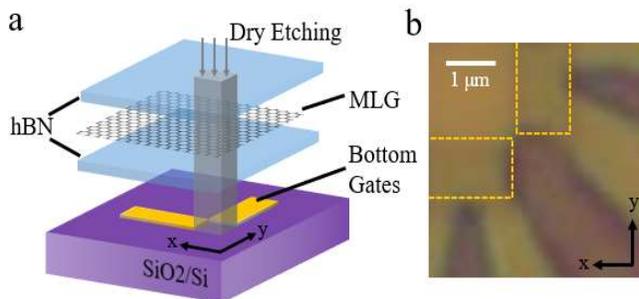
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## S1. Sample Preparation, Device Fabrication and Measurement Method.



**Figure S1. Device Architecture.** (a) Schematic of the hBN-encapsulated monolayer graphene stack. The stack is transferred onto pre-deposited bottom gates and etched into the designed shape. (b) Optical microscope image of a similar device. The boundary of the bottom gates is delineated by the yellow dashed lines. The scale bar on the top left corner corresponds to 1  $\mu\text{m}$ .

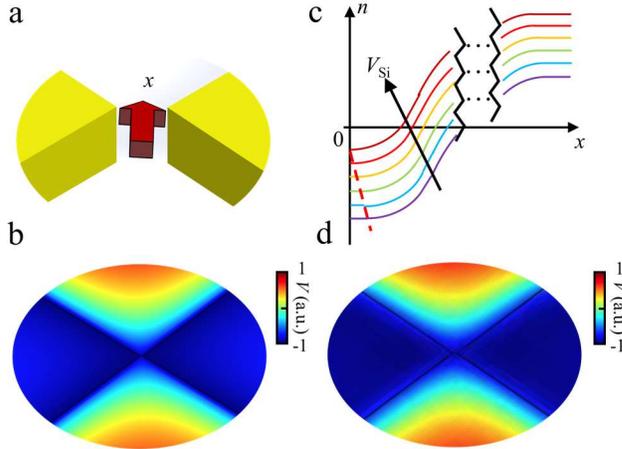
A pair of metal gates (serving as the local bottom gates  $V_{LM}/V_{RM}$ , whose long axis are perpendicular to each other) consisting of Cr/Pd-Au alloy (1 nm / 7 nm) is deposited on a SiO<sub>2</sub> (285 nm) /Si (doped) chip (serving as the silicon backgate,  $V_{Si}$ ). The Pd-Au alloy (40% Pd / 60% Au) is chosen to reduce the surface roughness when it is compared to conventional Au deposition. The gates are annealed in a high-vacuum environment at 350°C for 5 minutes to remove surface residue.

Top hBN, graphene [1], and bottom hBN flakes are picked up consecutively, using polypropylene carbonate and polydimethylsiloxane stamps via the standard dry transfer technique [2], before dry-transferred [3,4] on top of the pre-deposited bottom gates. The sample is rinsed in acetone

and isopropyl alcohol to remove residue, and then annealed in a high-vacuum environment at 350°C for 5 minutes. Electrical contacts to metal gates and ohmic contacts to 1D graphene boundaries are fabricated using electron-beam lithography and metal deposition (Cr/Pd/Au, 1 nm / 5 nm / 140 nm). Lastly, the stack is etched into a “ $\Lambda$ ” shape, with sample edges aligned with the boundary of local metal gates, as shown in the schematic image (fig. S1a). The atomic force microscope scans of the device are taken to ensure that the device is free from air bubbles and local atomic strain.

Experiments are performed in a Bluefors dilution fridge at a base temperature of  $\sim 10$  mK. All data are collected by a standard lock-in amplifier with an alternating current excitation of 100 nA at 17.777 Hz applied through the device unless otherwise specified. DC bias measurements are performed by applying a direct current through the sample from a Keysight waveform generator.

## S2. Partially Screened Electrostatics at the Quantum Point Contact.



**Figure S2. COMSOL Simulation of Partially screened electrostatics at the quantum point contact.** (a) Schematic image of the device. (b) COMSOL simulation of the electrostatics at  $\Delta V_M = -1$  V and  $\Delta V_{Si} = 1$  V. (c) Schematic of the carrier density along the sample edge to the center ( $x$ -direction) when local metal gate regions are n-doped and the silicon backgate region is p-doped. The red dashed line represents the edge of the local metal gate fringing electrostatics. (d) As a comparison, COMSOL simulation of the electrostatics at  $\Delta V_M = -1$  V and  $\Delta V_{Si} = 1$  V if the metal gates are configured as top gates. The Si back gate is not screened by the metal gates in this case.

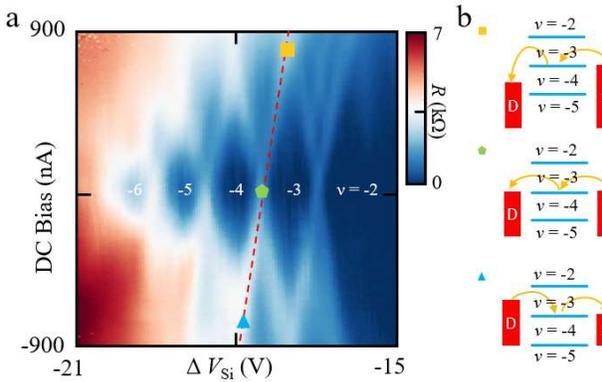
In previous studies of conventional QPC devices, a global gate is used to define the carrier density in the 1D QPC channel while a depleted region can be obtained through both local gates and the global gate. In contrast to conventional QPC devices, the bottom gate is designed to provide screening of backgate electrostatic fields instead of defining the constriction. The separation between the corners of the bottom gates is designed to be  $\sim 100$  nm, corresponding to the estimated length of the quasi-1D channel (not its width). The width of the channel is tuned by electrostatic fringing fields (controlled by  $\Delta V_{Si}$ ) at the side of the channel. The carrier density in the channel is first offset by the fringing field from the bottom gates, then being fine-tuned by  $\Delta V_{Si}$  via the separation of the bottom gates. This results in an “L” shaped carrier density distribution in the channel. The uniform doping of the channel is tuned by partially screened electrostatic fields applied directly from below the channel (flat part of the “L”) while the width is adiabatically tuned by the fringing field from the side of the channel (steep side of the “L”). The carrier density distribution along the width of the channel, now taken to be the

$x$ -direction (shown in fig. S2a), is plotted for different values of  $\Delta V_{Si}$  (fig. S2c) for the QPC configured in the coupling regime, and the channel and backgate region having opposite carrier types. The width of the channel is defined by the spatial span between two boundaries: the physical edge of the channel defined at  $x = 0$  (that has no  $\Delta V_{Si}$  dependence), and the electrostatically defined boundary (dashed line in fig. S2c) determined by the fringing field from  $\Delta V_{Si}$ . Qualitatively, the channel width is the width of the “flat” region where the carrier density can be approximated as constant in the context of Quantum Hall physics. In this flat region, the change in the carrier density is, at least, an order of magnitude smaller than the degeneracy of a Landau level (i.e., the maximum number of particles per Landau level). As  $\Delta V_{Si}$  increases, the n-type doping in the channel decreases, and the top ( $x > 0$ ) electrostatically defined boundary (red dashed line) approaches the bottom ( $x = 0$ ) etch-defined physical edge, thereby reducing the QPC confinement width. Both the width and the doping level of the channel are more finely tuned by partially-screened fringing fields from  $\Delta V_{Si}$  than in conventional QPC devices, allowing precise control over Quantum Hall edge states (QHES) in the channel with excellent energy and spatial resolution.

For a quantitative determination of the channel width discussed above, a COMSOL simulation of backgate electrostatic fields along the width of the channel ( $x$  direction in fig. S2a) was performed with  $\Delta V_M = -1$  V and  $\Delta V_{Si} = 1$  V (fig. S2b), a typical QPC device configuration. The red dashed line (fig.

S2c) indicates the boundary of the channel where the variation of carrier density along the  $x$  direction (due to smoothly varying yet nearly flat electrostatics in the channel) is less than  $1/5$  of  $\Delta n = eB/h$ .  $\Delta n$  corresponds to the increase in the carrier density when a degeneracy-lifted Landau level (LL) is filled. At  $\Delta V_{Si} = 1$  V, the width of the channel is estimated to be 50 nm based on the simulation results and the capacitive coupling of the device, thereby allowing multiple compressible strips to be distributed across the channel. The minimum size of the compressible strips is estimated by the broadening of the strips, where the broadening is of the same order of magnitude as the magnetic length  $l_B = \sqrt{\hbar/eB} \sim 10$  nm at  $B = 6$  T.

The simulation provides a quantitative estimation of electrostatic fields in the channel that agrees with our experimental observations. However, sample-to-sample variations unavoidably exist for nano-devices that require precise overlay alignment between subsequent lithography steps, such as the one presented in this work. For example, the distance from the etch-defined physical edge of the graphene to the bottom gates is controlled within  $\sim 10$  nm standard variation but can nevertheless affect the specifics of local electrostatic fields. Despite microscopic variations between devices, a gate-defined channel can always be established and precisely tuned by local electrostatic fields in this device architecture, with the caveat that the precise voltages applied may differ. Despite sample variations, core physics observations and device functionality have been reproduced in multiple samples.



**Figure S3. Measured resistance as a function of  $\Delta V_{Si}$  and DC bias.** Obvious Coulomb diamonds are obtained when sweeping the silicon backgate voltage and the DC bias current. The red dashed line is a boundary of one Coulomb diamond.

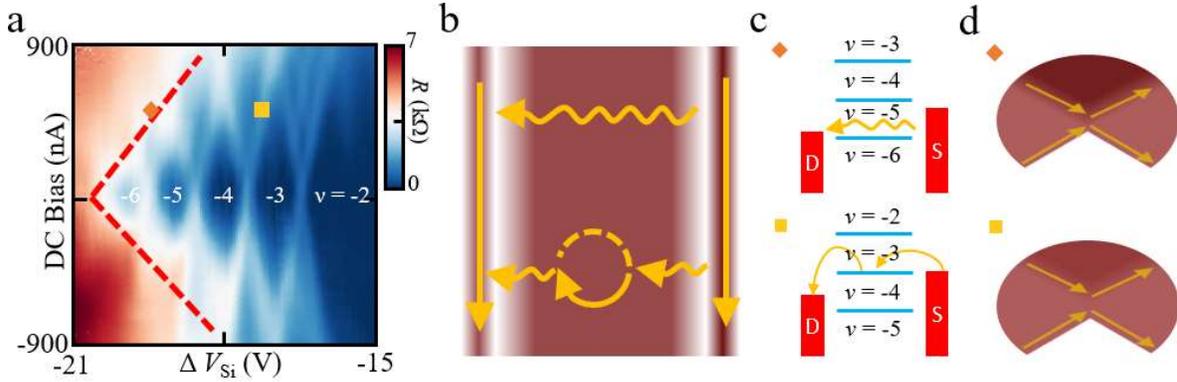
### S3. Characterization of Gate Capacitive Coupling via Tunneling Spectroscopy of Quantum Hall Edge States.

We directly characterize the capacitive coupling of  $\Delta V_{Si}$  to the degeneracy-lifted LLs in the channel via tunneling spectroscopy between two QHES demonstrated in the manuscript (replotted in fig. S3a). As discussed in the manuscript, resistance peaks arise when one of the degeneracy-lifted LLs is in resonance with either the source or drain chemical potential. As a specific example, we highlight (by a dashed red line) the resistance peak in which the LL between  $\nu = -3$  and  $\nu = -4$  is in resonance with the source chemical potential. The source chemical potential is accurately tuned by applying a bias voltage to the device. The slope of the peak position (in  $I_{DC}$  vs  $\Delta V_{Si}$ ) is measured to be 890 nA/V. Therefore, the capacity of  $\Delta V_{Si}$  in

shifting the energies of the degeneracy-lifted LLs in the channel is measured to be 0.403 meV/V.

### S4. Funnel-shaped Background in Finite Bias Transport Measurement.

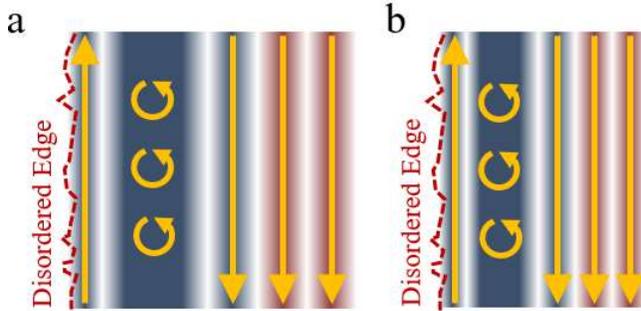
In contrast to the cascade nature (source chemical potential  $>$  degeneracy-lifted LL in the center of channel  $>$  drain chemical potential) of resonant tunneling (responsible for diamond-shaped resistance peaks), the funnel-shaped background (fig. S4a, red dashed lines) is due to direct tunneling between QHES (fig. S4b,c) on opposite boundaries of the channel as the two boundaries merge together (fig. S4d). In other words, the funnel-shaped background corresponds to the breakdown of QH transport [5–12]. While a more positive  $\Delta V_{Si}$  corresponds to a wider channel (and therefore larger separation between QHES), the tunneling current increases with DC bias, eventually leading to onset of significant back-scattering due to QH breakdown (red-dashed lines) that are tuned by both  $\Delta V_{Si}$  and DC bias.



**Figure S4. Funnel-shaped Background in Finite DC Bias Transport Measurement.** (a) Red dotted lines outline the boundary of the funnel-shaped background. (b) Schematic of direct quantum tunneling (upper path) and tunneling through the extended bulk state (lower path) in real space. (c) Schematic of direct quantum tunneling (upper) and tunneling through the extended bulk state (lower). (d) Closer proximity between QHES on the opposite boundaries of the QPC can help enhance quantum tunneling.

### S5. Tuning the $\nu = 1$ Gap Via Proximity to the Disordered Physical Device Edge.

The origin of the  $\nu = 1$  gap can be traced to electron-electron interactions [13–24]. As  $\Delta V_M$  becomes more positive and  $\Delta V_{Si}$  becomes more negative, the n-type compressible strips are pushed closer towards the disordered physical edge (fig. S5). A higher level of disorder along the physical edge suppresses the interaction-driven  $\nu = 1$  energy gap. This is corroborated by our data shown in fig. 3c, e and can be served as a new experimental knob for tuning the degeneracy-lifted LL gap via spatial proximity to disordered physical edges.



**Figure S5. Tunable Proximity to Disordered Physical Edge.** From (a) to (b): as  $\Delta V_M$  becomes more positive and  $\Delta V_{Si}$  becomes more negative, the n-type compressible strips are pushed closer towards the disordered physical edge.

### S6. Measurement of Additional Devices.

Fig. S6 shows magneto-transport for a second dual-bottom-gated graphene QPC, Device 2 (D2). D2 yields a similar QPC phase diagram as Device 1 (D1) from the manuscript (fig. S6a). As previously explained, the separate tunneling and merged regimes can be achieved by tuning the bottom gates. In D2, the transition from the separated to the merged regime is smoother than in D1. The sharpness of the transition can be attributed to differences in device details. For example, the distance the bottom corner of the stack (where the QPC is located) is etched into the backgate region affects the QPC's electrostatic response to applied bottom gate voltages.

Signatures of degeneracy-lifted LLs are also observed in D2 in fig. S6b, c, though with comparably lower quality compared to D1. In D1, four individual resistance peaks are observed in a PPP configuration. In D2, the resistance peaks overlap with each other and are mixed into the merged regime. The  $\nu = 1$  gap in D2 is found to be almost constant with changing  $B$  (fig. S6d) when D2 is tuned into a PNP configuration, suggesting that spin-valley degeneracy cannot be lifted by the Zeeman effect as effectively as in D1. For constant  $B$ , QHES in D2 respond similarly to applied bottom gate voltages as D1 (fig. S6c, e). A Coulomb

Diamond can be found in a finite-bias transport measurement of Device 2, though affected by comparably lower device quality (fig. S6f).

### S7. Characterization of Degeneracy-Lifted Landau Gap.

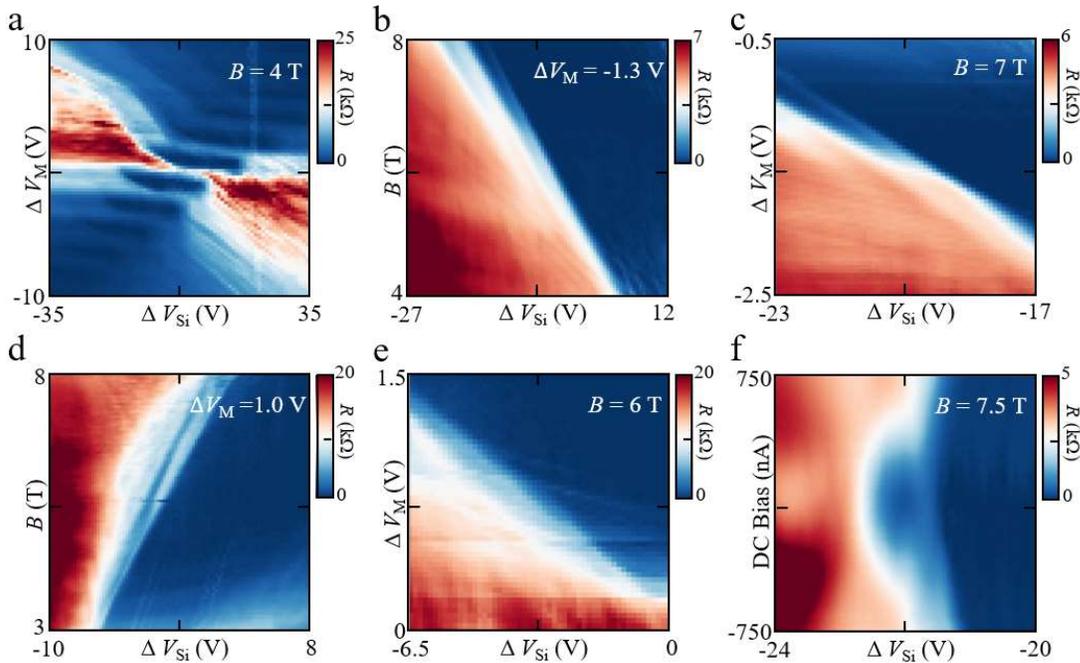
As mentioned in section S3, the capacity of  $\Delta V_{Si}$  in shifting the energies of the degeneracy-lifted LLs in the channel is measured to be 0.403 meV/V. Therefore, the energy gap can be calculated by multiple the voltage difference of the adjacent resistance peaks (where degeneracy-lifted Landau levels are observed) with the capacity value 0.403 meV/V. The corresponding resistance peaks  $G$  can be described by the following equation [25]:

$$G = G_0 \cosh\left(\frac{e(V - V_0)}{\Delta}\right)^{-2}$$

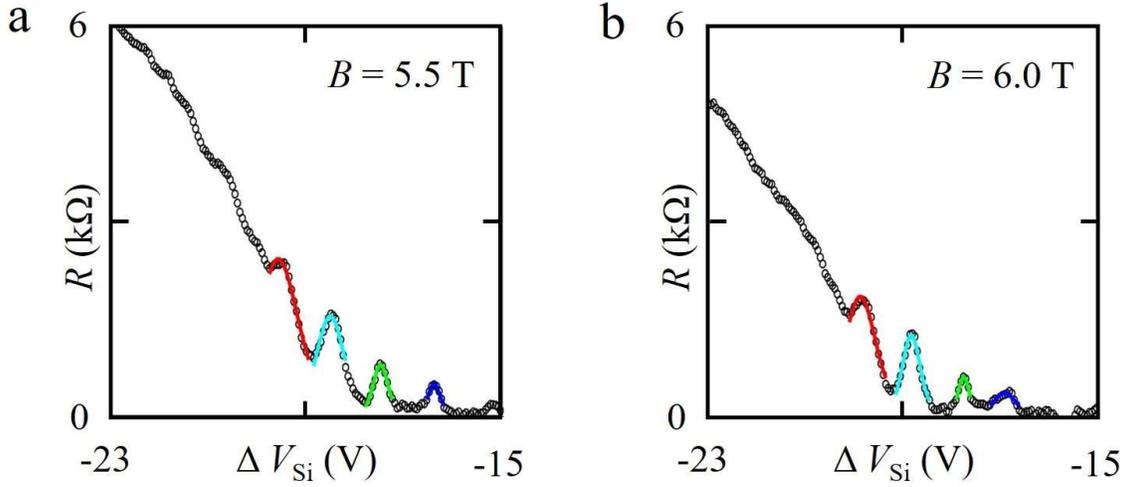
where  $G_0$  is the normalization index of the peak,  $V_0$  is the voltage at the center of the peak,  $e$  is the elementary charge and  $\Delta$  is the energy that proportional to  $kT$ .

Using this equation to fit the measured data points near the peaks, the center of the peak  $V_0$  as well as the corresponding error can be obtained. Figure S7 (a) and (b) show the original data points and the 99.7 % confidence fitting results when  $\Delta V_M = -1.75$  V at  $B = 5.5$  T and  $B = 6.0$  T, respectively. The red, cyan, green, and blue curves indicate the fitting results of the resistance peak 1, peak 2, peak 3 and peak 4. The gaps can be calculated as:

$$\begin{aligned} \text{gap 1} &= (\text{peak 2} - \text{peak 1}) \times 0.403 \text{ meV/V} \\ \text{gap 2} &= (\text{peak 3} - \text{peak 2}) \times 0.403 \text{ meV/V} \\ \text{gap 3} &= (\text{peak 4} - \text{peak 3}) \times 0.403 \text{ meV/V} \end{aligned}$$



**Figure S6. Additional Magneto-Transport Data for Device 2.** (a) Measured four-probe resistance of D2. (b)(c) Tunable broken-symmetry QHES in a PPP Configuration. Because of the compromised quality of the control device, the resistance peaks can be observed, but not as clearly as in D1. (d)(e) Tunable broken-symmetry QHES in a PNP Configuration. (f) Measured four-probe resistance as a function of  $\Delta V_{Si}$  and DC bias in a PPP Configuration at  $B = 7.5$  T.



**Figure S7. Resistance Peaks Fitting.** (a) Fitting results at  $\Delta V_M = -1.75$  V and  $B = 5.5$  T. (b) Fitting results at  $\Delta V_M = -1.75$  V and  $B = 6.0$  T. The red, cyan, green and blue curves indicate the fitting results of the resistance peak 1, peak 2, peak 3 and peak 4, respectively.

Subsequently, the voltage difference between the adjacent peak positions as well as the errors can be also calculated through a simple error propagation formula. The fitting results of the gap (in terms of gate voltage) as well as the errors in the represent of [gap 1, gap 2, gap 3] are  $[(0.427 \pm 0.021)$  meV,  $(0.412 \pm 0.014)$  meV,  $(0.439 \pm 0.016)$  meV] and  $[(0.423 \pm 0.015)$  meV,  $(0.436 \pm 0.008)$  meV,  $(0.340 \pm 0.026)$  meV] for  $B = 5.5$  T and  $B = 6.0$  T cases. Similarly, the gap sizes and the error bars at other magnetic fields and  $\Delta V_M$  can be extracted by the same method, as they presented in the fig. 4c~f. Noting that the data points in fig. 4c were extracted from the data of DC-bias measurement at the corresponding magnetic field when the bias is at zero.

### S8. Device Characterization at Zero Magnetic Fields and in Quantum Hall Regime.

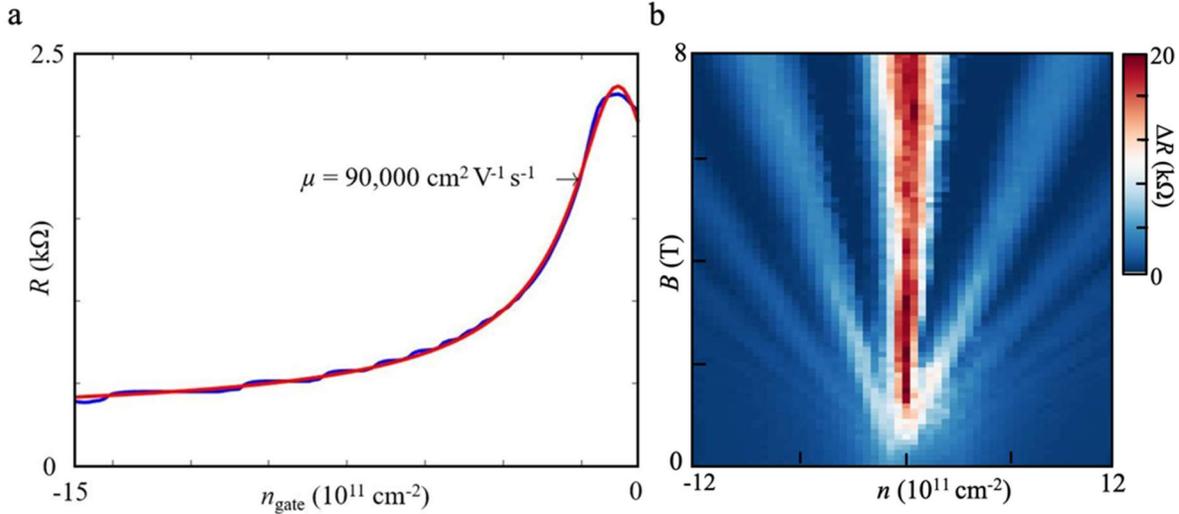
Here we perform characterization on a different device region (standard Hall bar shaped) fabricated with exactly the same graphene stack as the QPC device studied in this work. An estimation on the carrier mobility is provided using 4-probe resistance at zero magnetic field (fig. S8a) and the Shubnikov–de Haas (SdH) oscillation or quantum Hall effect (fig. S8b). At zero magnetic field, we fit the Dirac peak by the following formula [26]:

$$R = R_c + \frac{L}{W} \frac{1}{\mu e \sqrt{n_0^2 + (C_g |V_g - V_{Dirac}|)^2}}$$

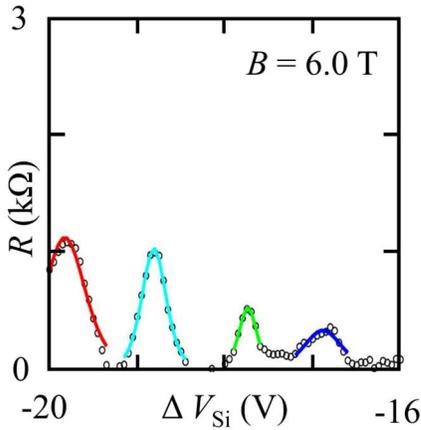
where  $L$  and  $W$  are the length and width of the sample,  $e$  is the elementary charge,  $R_c$  is the contact resistance from graphene 1D contact,  $\mu$  is the mobility,  $n_0$  is the residual carrier density,  $C_g$  is the capacitance of the hBN per unit area,  $V_g$  is the gate voltage, and  $V_{Dirac}$  is the Dirac peak shift voltage. The mobility is estimated as  $\sim 90,000$   $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ , corresponding to a mean-free path of  $\sim 0.9$   $\mu\text{m}$ .

The SdH oscillations start to be observable at around 1T as shown in fig. S8b. This provides an estimation of carrier mobility of  $\sim 90,000$   $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ , or a mean-free path [27] of  $\sim 0.9$   $\mu\text{m}$  at the carrier density of  $1.5 \times 10^{12}$   $\text{cm}^{-2}$ . This is consistent with the extracted mobility at zero magnetic fields. It is worth mentioning that even though the symmetry broken QH states are not visible from the quantum Hall measurements (which are measured over a region on the order of a few  $\mu\text{m}$  long), they can be clearly resolved in our QPC structure fine-tuned by the electrostatic fringing field.

This thanks to the novel device architecture of hybrid-edge and dual-bottom-gated QPC, which allows more versatile and precise electrostatic control over the location, transmission and tunneling of selected QHES.



**Figure S8. Device Characterization at Zero Magnetic Fields and in the Quantum Hall Regime.** (a) Fitting of Resistance Versus Carrier Density. Blue curve is the original data of resistance as a function of carrier density, while the red curve is the fitting result. The mobility is characterized about  $90,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . (b) SdH oscillation can be observed starting at  $B = 1 \text{ T}$  in a different device region from the same stack. Even though the symmetry-broken QH states are not visible in the quantum Hall measurements, they can be captured by the hybrid-edge and dual-bottom-gated QPC.



**Figure S9. Resistance Peaks After Subtracting Background Resistance.** The resistance dips are close to zero after the background subtraction at  $B = 6.0 \text{ T}$ . The red, cyan, green and blue curves are the peak fitting result based on the data after the background subtraction.

### S9. Background Subtraction of Energy Gaps of $\nu = -5, -4$ and $-3$

Due to the existence of the background resistance, the dips between  $\nu = -5, -4$  and  $-3$  gaps are not exactly hitting the zero. However, this background resistance can be subtracted. Similar to section S7, the background resistance can also be described as the equation:

$$G = G_0 \cosh\left(\frac{e(V - V_0)}{\Delta}\right)^{-2}$$

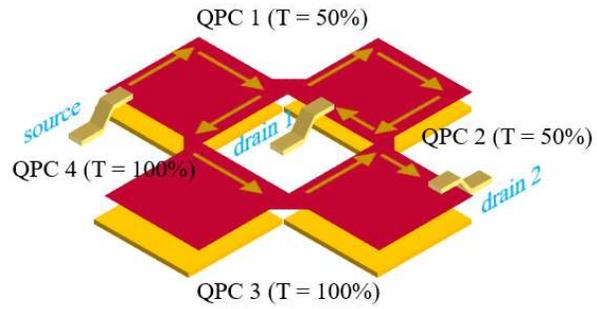
After fitting with the resistance values from the more negative silicon backgate voltages, it can be subtracted from the total resistance. Taking the peaks at  $B = 6.0 \text{ T}$  as an example (fig. S7(b)), after the background resistance subtraction, the resistance dips are close to zero, as shown by fig. S9.

### S10. Towards Potential Applications in Quantum Interferometers

Here we propose an interferometer scheme with our newly designed QPC, where we can have more delicate and selective control over the emergence, evolution, location, transmission, and width of broken-symmetry

edge state. Fig. S10 shows the schematic image of a device with 4 hybrid QPCs, two of which are tuned to allow 50% transmission for selected QH states, while the other two allow full transmission. In this configuration, the size of the interference path can be fine-tuned by the Si back gate, and the lower two metal gates. Depending on the choice of which two QPCs serve as effective 50/50 beam splitter, the interference paths could be formed in different device regions. Setting 3 or more QPCs at 50% transmission can also allow more advanced interferometry network.

It is worth noting that while our QPC operation relies on pp' or pn interface at the vicinity of the QPC, after the two paths has diverges away from the QPC, the part of graphene on top of the Si back gate can be etched, so the path along pp' or pn interface can be transformed to conventional physical edge, eliminating the complication due to QH states hybridization at the pp' or pn interface.



**Figure S10. Proposed Interferometer Scheme.** Source and drains are indicated by metal contacts. The direction of QHES is labeled by yellow arrows. QHES split at QPC 1 with 50% transmission rate, then meet again at QPC 2 and finally flow into drain 1 and drain 2.

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