Electrical properties improvement for boron-doped diamond metal-oxide-semiconductor field-effect transistors

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Abstract

High-performance boron-doped diamond (B-diamond) metal-oxide-semiconductor field-effect transistors (MOSFETs) are fabricated by improving fabrication process and device structures. Drain current maximum values for the B-diamond MOSFETs working at room temperature (RT) and 300 °C are −1.2 and −10.9 mA/mm, respectively. Both of them show on/off ratios higher than 10^9 and their extrinsic transconductance maximum values are 29.0 and 215.7 μS/mm, respectively. These properties are better than those of the previous reported values.

Diamond has been widely studied as a wide bandgap semiconductor for applications in high-power, high-frequency, and high-temperature electronic devices because it exhibits a high breakdown field, high carrier mobility, and high thermal conductivity.[1] *p*-type channel layers of hydrogen-terminated diamond (H-diamond),[2-7] silicon-terminated diamond (Si-diamond),[8,9] and boron-doped diamond (B-diamond),[10-14] are employed for the fabrication of high-performance diamond-based metal-oxide-semiconductor field-effect transistors (MOSFETs).

For the H-diamond channel layer, two-dimensional hole gases are accumulated on its surface with a sheet hole density of ~10^{14} cm^{-2}.[15] The hole accumulation is explained by the transfer doping mechanism,[16] where electrons are transferred from the diamond to the surface negatively charged adsorbates. The H-diamond-based MOSFETs have been fabricated with high drain current maximum ($I_{D,max}$, –1.35 A/mm), extrinsic transconductance maximum ($g_{m,max}$, 206 mS/mm), cut-off frequency (70 GHz), and on/off ratio (>10^9).[2-7] However, their high-temperature performance has not been satisfactory owing to the poor thermal stability of surface adsorbates.[17]

For the Si-diamond-based channel layer,[8,9] the surface bonds of C-Si are similar with those of the C-H on the H-diamond to generate the hole accumulation. In order to enhance the properties of the Si-diamond-based MOSFETs, heavily B-doped selectively layers (concentration: 10^{21} cm^{-3}) on the Si-diamond would be necessary. The Si-diamond-based MOSFETs could work well at 300 and 400 ºC with excellent $I_{D,\,max}$ and $g_{m,\,max}$ of –124 mA/mm and 4100 μS/mm, respectively.[9] However, high-temperature operation also degraded the electrical properties, such as on/off ratio decreased from 10^8 to 10^6.

For the B-diamond channel layer,[10-14] the activation energy (370 meV) of boron

dopants is higher than the thermal energy (26 meV) provided at room temperature (RT). Its hole density is relatively low, and B-diamond-based MOSFETs exhibit low $I_{D,max}$ and $g_{m,max}$ of –0.49 mA/mm and 18.7 μS/mm, respectively.[13] The B-diamond MOSFET has good thermal stability after annealing at 500 ºC with $I_{D,max}$ and $g_{m,max}$ of –0.6 mA/mm and 21.4 μS/mm, respectively.[13] By employing the ozone precursor for the Al_2O_3 gate oxide deposition, the Al_2O_3/B-diamond interfacial quality has been improved and the B-diamond MOSFET operate with on/off ratio higher than 10^8.[14]

In order to further enhance the performance of the B-diamond MOSFETs, we are currently putting more effort into improving the fabrication process and the device structure. For demonstrating the performance of them at high-temperature, we have investigated their electrical properties at 300 ºC.

Figure 1 illustrates the fabrication process for the B-diamond MOSFETs. First, Ib-type (100) diamond substrates were boiled in a solution of H_2SO_4 + HNO_3 at 300 ℃ for 3 hours to clean the diamond surface [Fig. 1(a)]. The B-diamond epitaxial layer was grown by microwave plasma-assisted chemical vapor deposition [Fig. 1(b)]. The microwave power, temperature, and chamber pressure were kept at 1.4 kW, ~1000 ℃, and 18.6 kPa, respectively.[18] The boron source was the residual boron in chamber from the previous B-diamond growth. Flow rates for the source gases of H_2 and CH_4 were 49 and 1 sccm, respectively. Thickness and concentration of boron atoms for the B-diamond epitaxial layer were measured by secondary ion mass spectroscopy to be 2650 nm and ~10^{16} cm^{-3}, respectively. Acceptor concentration was deduced based on the capacitance-voltage measurement to be 6.0×10^{14} cm^{-3}.

The B-diamond epitaxial layer was treated in the acid solution (H_2SO_4 + HNO_3) at 300 ℃ for 3 hours, changing its hydrogen surface to oxygen [Fig. 1(c)]. After

sequentially coating the B-diamond with a positive photoresist (LOR5A) followed by an image reversal photoresist (AZ5214E) using a spin-coater, it was exposed and developed using a DL-1000 scanning maskless lithography system and tetramethylammonium hydroxide (TMAH) solution (concentration: 2.38%), respectively. The spin speed and time for coating both photoresists were 7000 rpm and 1 second, respectively. The baking temperature and time for LOR5A were 180 °C and 5 minutes, and those for AZ5214E were 110 °C and 2 minutes, respectively. The developing time in the TMAH solution was 2.0–2.5 minutes.

The source/drain electrodes consisting of a Ti/Au bilayer (10/150 nm) were evaporated on the B-diamond by electron-gun evaporation system [Fig. 1(d)]. The chamber pressure used for evaporating the Ti/Au bilayer was ~10^{-6} Pa, and the evaporation rates for the Ti and Au were 1 and 2 Å/s, respectively. They were annealed at 550 °C for 20 minutes in an Ar atmosphere to form Ohmic contacts using a rapid thermal annealing system [Fig. 1(e)]. An Al_2O_3 gate oxide was deposited by atomic layer deposition at 200 °C using $Al(CH_3)_3$ and ozone precursors [Fig. 1(f)]. The gate oxide thickness was approximately 26 nm. A Ti/Au (10/200 nm) bilayer was employed as the gate electrode [Fig. 1(g)]. Then, the Al_2O_3 film was deposited again with thickness of 20 nm to cover the surface of the sample [Fig. 1(h)], unlike our previous reports.[13,14] This Al_2O_3 cover layer is helpful to eliminate the surrounding environmental effect and the edge leakage of electrodes for the B-diamond MOSFETs, which would enhance their reliability and device performance.

Windows for accessing the electrodes were opened by etching the Al_2O_3 film using a capacitively coupled plasma reactive-ion etching system in a CHF_3 + Ar atmosphere [Fig. 1(i)]. The plasma power, chamber pressure, CHF_3 flow rate, and Ar flow rate were

100 W, 3.0 Pa, 10 sccm, and 40 sccm, respectively. The electrical properties were measured using a Grail 10-5-LV-HTV prober system at RT and 300 ºC.

Figures 2(a) and 2(b) shows a scanning electron microscopy image and schematic diagram of the B-diamond MOSFET, respectively. The diameter for the drain electrode is 299.6 μm. The gate width (W_G) can be calculated as 940.7 μm. The L_G is 2.6 μm. The interspatial lengths for the gate-to-source and gate-to-drain electrodes are 5.8 and 4.6 μm, respectively. Comparing to our previous report (5.6/9.8/15.3 μm),[13] all of them have been shortened. This is benefit to decrease total on-resistance (R_{ON}) and to increase $I_{D,max}$ for the B-diamond MOSFETs.

Figures 3(a) and 3(b) show the I_D as functions of drain voltage (V_D) for the B-diamond MOSFETs working at RT and 300 °C, respectively. The gate-to-source voltage (V_{GS}) varies from –20.0 to 78.0 V in steps of +2.0 V. They show good operations with *p*-type characteristics. The $I_{D,max}$ for the B-diamond MOSFET working at RT is –1.2 mA/mm. Although the boron doping and acceptor concentrations (~10^{16} cm^{-3} and 6.0×10^{14} cm^{-3}) for this B-diamond channel layer is lower than those (~10^{17} cm^{-3} and 2.9×10^{16} cm^{-3}) of the previous one,[13] the $I_{D,\,max}$ is more than two times higher than that of the reported value of –0.49 mA/mm. This is possibly attributed to the decrease of the L_G and the interspatial lengths for the gate-to-source and gate-to-drain electrodes, resulting in the reduction of the R_{ON} from 26.9 kΩ mm to 9.6 kΩ mm. At the working temperature of 300 °C, the $I_{D,max}$ significantly increases to –10.9 mA/mm and the R_{ON} decreases to 1.1 kΩ mm because of the activation of boron dopants at higher temperature. The $I_{D,max}$ working at 300 °C is higher than that (~8 mA/mm) of the B-diamond MOSFET working at 250 °C.[12]

Figures 4(a) and 4(b) show the I_D–V_{GS} characteristics for the B-diamond MOSFETs

working at RT and 300 °C, respectively. By linear extrapolation, threshold voltage (V_{TH}) values for the MOSFETs at RT and 300 °C are determined to be 63.8 ± 0.1 and 31.2 ± 0.1 V, respectively. The on/off ratios for both MOSFETs are higher than 10^9. They are the highest comparing to the previous reports by now.[10-14] The choosing of ozone precursors for the deposition of Al_2O_3 gate film[13] and the covering of metal electrodes with Al_2O_3 layer lead to the improvement of Al_2O_3/B-diamond interfacial quality and the suppression of electrode edge leakage. This is the possible reason for the better on/off ratios of the B-diamond MOSFETs.

Subthreshold voltage (*SS*) values for the MOSFETs working at RT and 300 °C are determined to be 315 and 570 mV/dec, respectively. Then, interfacial trapped charge density (D_{it}) of the Al_2O_3/B-diamond can be calculated using Eq. (1).[19]

$$SS = \frac{kT}{q}\ln(10)\left(1+\frac{qD_{it}}{C_{OX}}\right) , \quad (1)$$

where k, T, q, and C_{OX} are Boltzmann's constant (8.62×10^{-5} eV/K), working temperature, elementary charge (1.6×10^{-19} C), and oxide capacitance (0.266 μF/cm^2),[14] respectively. The D_{it} for the B-diamond MOSFET working at RT was calculated as 7.2×10^{12} eV^{-1} cm^{-2}, which is better than that of the previous report value (1.1×10^{13} eV^{-1} cm^{-2}) that for the MOSFET without the electrode cover layer.[14] At working temperature of 300 °C, the D_{it} increases to be 1.4×10^{13} eV^{-1} cm^{-2}. Figures 4 (c) and 4(d) show the g_m-V_{GS} characteristics for the B-diamond MOSFETs working at RT and 300 °C, and their $g_{m,max}$ values were 29.0 and 215.7 μS/mm, respectively.

Table 1 summarized electrical properties of the B-diamond MOSFETs working at RT, 250 °C, and 300 °C. The $I_{D,max}$, R_{ON}, on/off ratio, D_{it}, and $g_{m,max}$ in this work are improved comparing to the previous B-diamond MOSFETs.[10-14] Although the on/off ratio

(>10^9) of the B-diamond-based MOSFET is better than that (10^6) of the Si-diamond-based MOSFET at 300 °C, the $I_{D,max}$ (–10.9 mA/mm) and $g_{m,max}$ (215.7 μS/mm) are much lower than those of the latter of ~120 mA/mm and ~4000 μS/mm, respectively.

There are several methods to further improve performance of the B-diamond MOSFETs. One is to decrease the Ohmic contact resistance by choosing heavily B-doping or ion implantation in the source/drain contact area. We can also try to improve the structures of the B-diamond MOSFETs such as to further decrease the L_G and the interspatial lengths between source/drain and gate electrodes for reducing the R_{ON} of the MOSFETs or to fabricate the triple-gate fin-type MOSFETs to enhance the carriers travelling at the same device area.[20]

In this study, B-diamond MOSFETs have been fabricated and their operating performance at RT and 300 °C has been investigated. The $I_{D,max}$, on/off ratio, and $g_{m,max}$ for the B-diamond MOSFET working at RT are −1.2 mA/mm, >10^9, and 29.0 μS/mm, respectively. The B-diamond MOSFET still operates well at 300 °C with the above properties of −10.9 mA/mm, >10^9, and 215.7 μS/mm, respectively. This study would promote the development of diamond-based MOSFETs for high-temperature applications.

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Data Availability Statements

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Table 1. Summary of electrical properties of the B-diamond MOSFETs working at RT, 250 ℃, and 300 ℃.

Ref.	Tem.	$I_{D,max}$ (mA/mm)	R_{ON} (kΩ mm)	V_{TH} (V)	On/off ratio	D_{it} (eV^{-1} cm^{-2})	$g_{m,max}$ (μS/mm)
[10]	RT	–0.0019	>1000	7	~10^4	-	~2
[11]	RT	–0.12	~200	>20	-	-	-
[12]	RT	–0.12	~80	35	>10^5	-	-
	250 ℃	–8	~1.7	-	5×10^5	-	-
[13]	RT	–0.49	26.9	63.2	-	-	18.7
[14]	RT	–0.11	220	58.8	>10^8	1.1 × 10^{13}	4.1
This work	RT	–1.2	9.6	63.8	>10^9	7.2 × 10^{12}	29.0
	300 ℃	–10.9	1.1	31.2	>10^9	1.4 × 10^{13}	215.7

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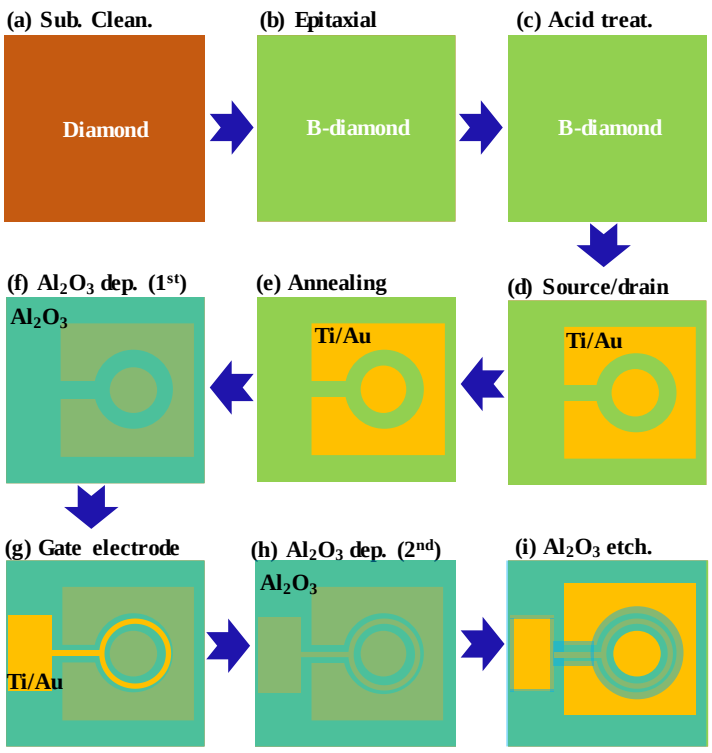
Figure captions

FIG. 1. Fabrication process for B-diamond MOSFET: (a) Diamond cleaning, (b) B-diamond growth, (c) acid treatment, (d) Ti/Au source/drain electrode formation, (e) annealing to form Ohmic contact, (f) first time Al_2O_3 deposition for gate oxide, (g) Ti/Au gate electrode formation, (h) second time Al_2O_3 deposition to cover the electrodes, and (i) opening windows for the electrodes.

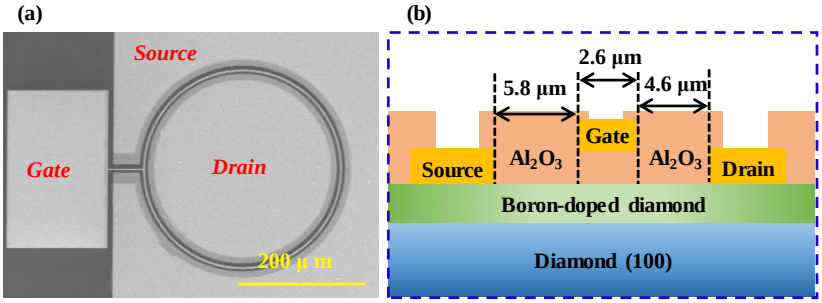
FIG. 2. (a) Scanning electron microscopy image and (b) schematic diagram of the B-diamond MOSFET, respectively.

FIG. 3. (a) and (b) I_D–V_D characteristics for the B-diamond MOSFETs working at RT and 300 ºC, respectively.

FIG. 4. (a) and (b) I_D–V_{GS} characteristics for the B-diamond MOSFETs working at RT and 300 ºC, respectively . (c) and (d) g_m-V_{GS} characteristics for the B-diamond MOSFETs working at RT and 300 ºC, respectively .



Liu *et al.*, Figure 1



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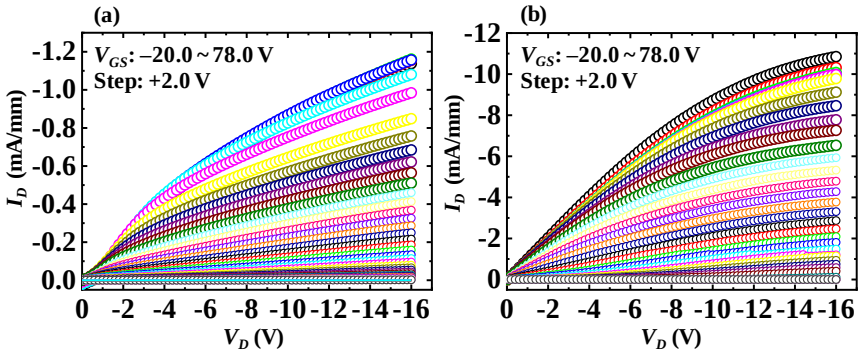
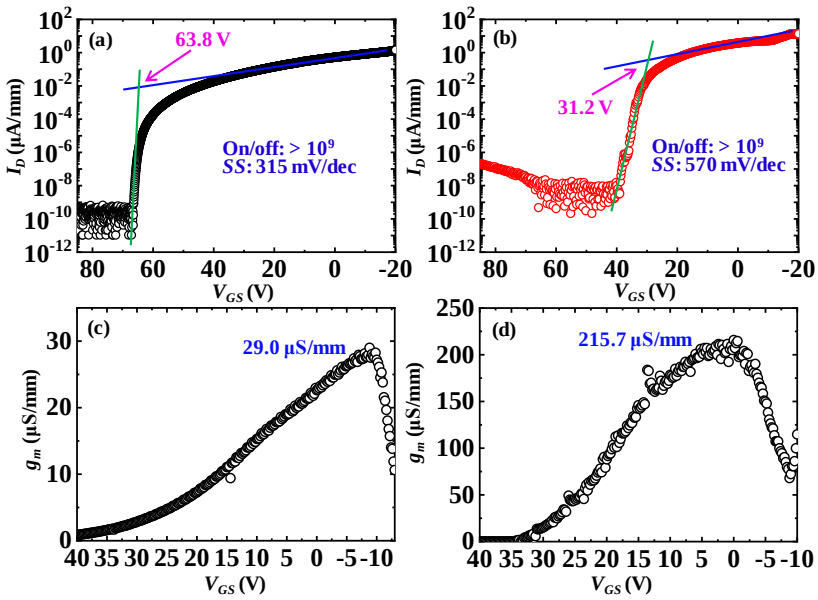


Liu *et al.*, Figure 3



Liu *et al.*, Figure 4