Development of p-type ion implantation technique for realization of GaN vertical MOSFETs

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1. Introduction

GaN has attracted attention as a semiconductor material for next-generation power switching devices. Vertical-type GaN devices with MOS gate driving are preferable for high-power switching applications. Due to recent advances in bulk GaN crystal growth [1], more studies are reporting vertical-type GaN devices with a breakdown voltage exceeding 1 kV on GaN substrates [2, 3]. However, these reports use an epitaxially grown p-type layer or fin-structure.

For practicality and reliability viewpoints, it is essential to form a p-type layer by ion-implantation (I/I). I/I requires a high-temperature activation heat treatment, however, heat treatment at 800 °C or higher decomposes GaN due to the very strong triple bond of N molecule that reduces the negative Gibbs free energy of the nitride component [4]. Consequently, p-type formation by I/I into GaN is extremely difficult. To address this issue, an ultra-high-pressure annealing (UHPA) process, in which GaN does not thermally decompose in a thermal equilibrium state, has been investigated. The p-type hole conduction in the Mg-implanted GaN layer annealed at 1400 °C under a nitrogen pressure of 1 GPa was demonstrated using the temperature dependence of the Hall effect measurement [5]. Recently, further investigation has been carried out, and p-type activation by UHPA process at 300 MPa and 1300 °C has also been reported [6]. However, challenges still exist in processing large diameter wafers and improving throughput.

Therefore, we are investigating activation of the p-type I/I layer by atmospheric pressure annealing using a encapsulation cap. By using AlN for the encapsulation cap, annealing at 1300°C for 5 minutes can be performed stably without surface roughening.

To realize GaN vertical MOSFETs fabricated by I/I, it is necessary to secure a high breakdown voltage of pn junction by improving the characteristics of the p-type I/I layer and control the MOS channel characteristics on the p-type I/I layer. In this talk, we will introduce recent development and issues of the p-type activation by atmospheric pressure annealing using AlN encapsulation cap.

2. Improvement of characteristics of p-type ion implantation layer

It has been reported that large complex defects formed by clustering of Ga vacancies and N vacancies introduced by Mg I/I remain after the activation heat treatment [7]. In addition, the emission peaks from deep levels due to N vacancy-related defects was confirmed from the PL spectrum [8]. These defects have been found to adversely affect the electrical properties of p-type I/I layers. Therefore, sequential N I/I into the Mg I/I layer has been investigated to reduce N vacancies [9].

To evaluate the breakdown voltage of the pn-junction, we fabricated a pn-diode by I/I [10]. A 10-µm-thick n-GaN layer was epitaxially grown by MOCVD on the n-type GaN (0001) substrate. The net donor concentration of the n-GaN epitaxial layer was around 1.5×10^{16} cm^{-3}. Mg ions were selectively implanted on the n-GaN layer. The Mg ions were implanted with 10 to 240 keV and a total dose of 8.4×10^{13} cm^{-2} to obtain a 0.3-µm-thick box-profile of 1×10^{18} cm^{-3} with a p+ contact region of 2×10^{19} cm^{-3} near the surface. After Mg I/I, N I/I was carried out sequentially. N ions were implanted with 10 to 180 keV and a total dose of 9.9×10^{13} cm^{-2}. In addition, samples without N sequential I/I were fabricated. After Mg and N I/I, the wafers were annealed at 1300 °C for 5 minutes in a N_2 atmosphere at atmospheric pressure with an AlN encapsulation cap to prevent GaN dissociation. After annealing, the AlN cap was chemically removed. AFM measurements in a 1-µm square area indicated that the typical RMS surface roughness of GaN after activation annealing was 0.25 nm. The anode electrode was composed of nickel and gold, while the cathode electrode was

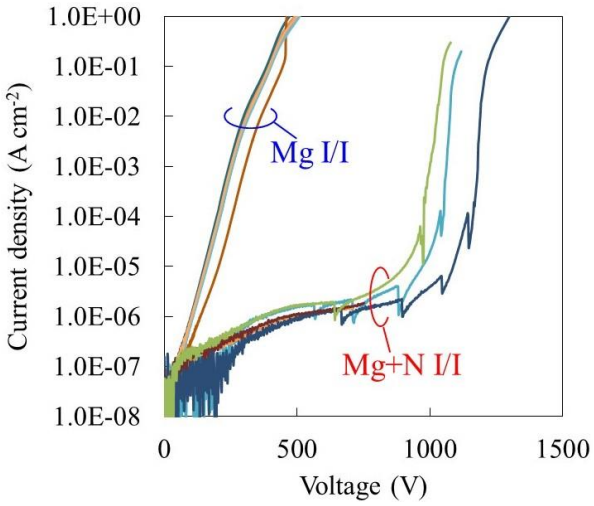

Fig. 1. Reverse I-V characteristics of the fabricated GaN pn-diode [10]. Copyright (2019) The Japan Society of Applied Physics.

composed of titanium and aluminum.

In Fig.1, it is shown the reverse I-V characteristics of the pn-diodes fabricated by Mg I/I. Subsequent N I/I drastically suppresses the leakage current and increases the breakdown voltage. Using PL and positron annihilation spectroscopy, we reported that N sequential I/I into the Mg implanted layer enhances the activation of Mg through Mg diffusion and suppression of vacancy clustering (We call this technique the vacancy-guided Mg redistribution) [11, 12]. Therefore, the breakdown voltage improved due to the enhanced pn junction characteristics.

Unfortunately, it is still difficult to form a good ohmic contact on a p-type I/I layer. Therefore, we used an epitaxially grown p+ layer as a contact layer to form a stable ohmic contact for Hall-effect measurement [13]. The schematic cross sectional image of the Hall-effect measurement devices are shown in Fig.2. A 4-µm-thick n-GaN layer and a 500-nm-thick p-GaN layer were epitaxially grown by MOCVD on the n-GaN substrate sequentially. The net donor concentration of n-GaN epi-layer was around 1.0×10^{16} cm^{-3} and the Mg concentration of p-GaN epi-layer was around 3.0×10^{19} cm^{-3}. A part of p-GaN epi-layer was removed by ICP dry-etching to the depth of 1µm and the n-GaN epi-layer was exposed to the surface. The Mg ions and N ions were implanted into the exposed n-GaN region. Here, the implanted region was partly overlapped onto p-GaN epi-layer in order to achieve electrical conduction. After Mg and N I/I, the wafers were annealed at 1300 °C for 5 minutes in a N_2 atmosphere at atmospheric pressure with an AlN encapsulation cap. The Mg profile of implanted region after annealing was a 0.3-µm-thick box-like-feature with Mg concentration around 2.8×10^{18} cm^{-3} as shown in Fig.3. After

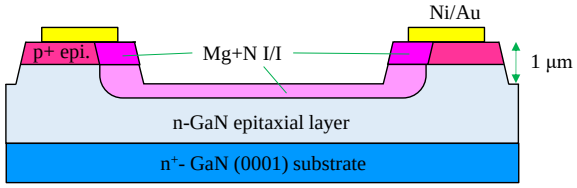

Fig. 2. Schematic cross sectional image of the Hall-effect measurement structure

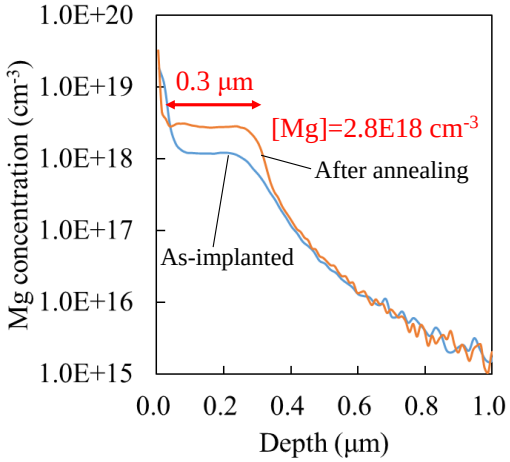

Fig. 3. Mg profiles of Mg and N implanted region

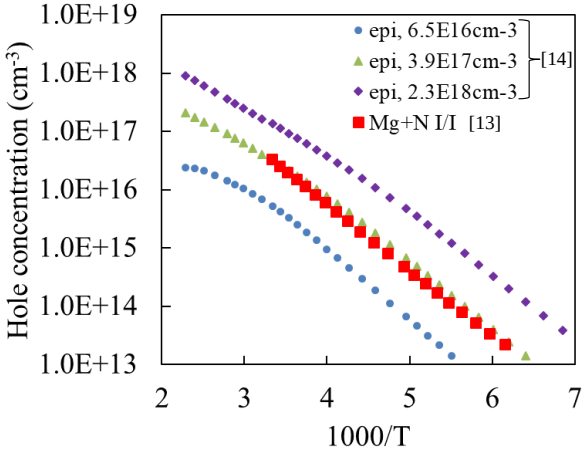

Fig. 4. Temperature dependence of hole concentration

the AlN removal, nickel and gold electrode were formed on p-GaN epi-layer.

We performed the Hall-effect measurement of the fabricated devices in the range of 160 to 300K. The temperature dependence of hole concentration is shown in Fig.4. As a result, a p-type conduction through the Mg and N sequential I/I layer was clearly observed and the temperature dependence of the hole concentration was obtained. The hole concentration assuming that the thickness of the Mg and N I/I layer was 300 nm were almost the same as those of the p-GaN epi-layer with a Mg concentration of 3.9×10^{17} cm^{-3} [14]. The hole mobility of the Mg and N I/I layer was about 16 cm^{-2} V^{-1} s^{-1} at room temperature, slightly smaller than that of the p-GaN epi-layer. Although the activation ratio of the Mg and N I/I layer is expected to be lower than that of p-GaN epi-layer, it was demonstrated that a p-type conduction through the Mg and N I/I layer can be realized by activation annealing at atmospheric pressure.

3. Control of the MOS channel characteristics on p-type ion implanted layer

For the applications of the GaN power devices, it is important to realize high channel mobility to differentiate from SiC devices. We reported that inversion-type MOSFET operation is possible on an epitaxially grown p-type GaN layer and the channel mobility of more than 100 cm^2 V^{-1} s^{-1} can be obtained [15]. For realizing a vertical-type devices, it is desirable to form MOS channel on a p-type I/I layer. Therefore, we investigated the control of channel characteristics on Mg I/I layer [16].

Mg ions were implanted on the n-GaN epitaxial layer grown by MOCVD on the n-GaN (0001) substrate. The donor concentration of n-GaN epitaxial layer was around 5×10^{15} cm^{-3}. The implantation energy of Mg was set at 700 keV, and three samples with different implantation doses were fabricated. The Mg I/I dose was set to 4.2×10^{14}, 1.4×10^{14} and 4.2×10^{13} cm^{-2}, respectively. The source and drain regions were selectively formed by Si I/I. An activation annealing of Mg and Si was simultaneously performed at 1300 °C for 5 minutes in N_2 atmosphere at atmospheric

pressure with an AlN encapsulation cap. Finally, the AlN cap was chemically removed. Then a plasma-CVD apparatus with TEOS gas deposited a 100-nm-thick SiO_2 layer at 300 °C. Titanium and aluminum were used as the gate, source, and drain metal. Forming gas annealing was performed at 400 °C for 30 min. In order to clarify the MOS channel property, the long channel lateral MOSFETs with the channel length of 100 μm and the gate width of 100 μm were evaluated.

In Fig. 5, it is shown the I_d-V_g transfer characteristics measured at V_d = 0.5 V. As the Mg dose increased, the threshold voltage (V_{th}) increased and the drain current decreased, obviously. The V_{th} is determined as a gate bias intercept of the linear extrapolation of I_d. The V_{th} were 9.2 V, 4.2 V, and 2.2 V on the Mg I/I layer with the Mg dose of 4.2×10^{14}, 1.4×10^{14} and 4.2×10^{13} cm^{-2}, respectively. It was shown that the V_{th} can be controlled by Mg I/I dose.

In Fig. 6, it is shown the field effect mobility (μ_{fe}) curves calculated from the I_d-V_g characteristics. The μ_{fe} gradually increased by applying the gate bias and showed a peak at certain gate voltage. By decreasing Mg dose, the maximum

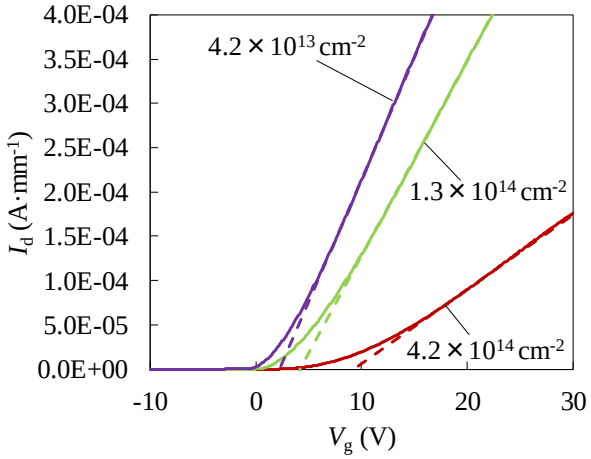

Fig. 5. The linear region I_d-V_g transfer characteristics of fabricated MOSFETs measured at V_d = 0.5 V [16].
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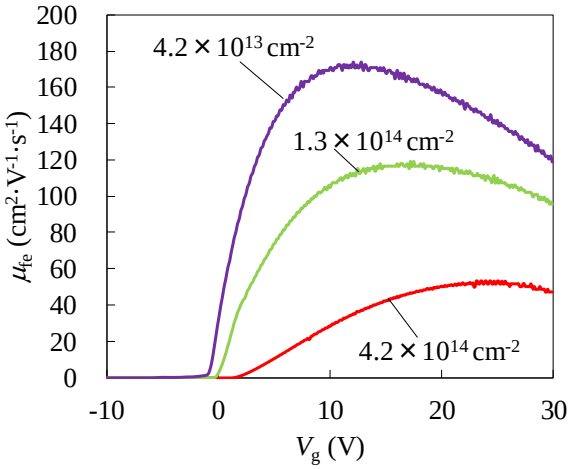

Fig. 6. The V_g dependence of the field effect mobility obtained on different Mg ion implantation dose layers [16].
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μ_{fe} increased, and the peak values were 53, 119 and 173 cm^2 V^{-1} s^{-1} on the Mg I/I layer with the Mg dose of 4.2×10^{14}, 1.4×10^{14} and 4.2×10^{13} cm^{-2}, respectively.

Therefore, the MOS channel characteristics can be controlled by Mg I/I dose and a high channel mobility of more than 100 cm^2 V^{-1} s^{-1} can be realized on p-type I/I layer.

4. Vertical GaN planar-gate MOSFETs

We demonstrated the vertical GaN planar-gate MOSFETs with low on-resistance and high breakdown voltage by combining the improvement of the pn junction breakdown voltage by sequential N I/I and the control of the MOS channel characteristics on the p-type I/I layer [10].

In Fig. 7, it is shown a schematic images of the fabricated vertical GaN planar-gate MOSFETs by I/I process. A short cell pitch design of 5 μm was used to reduce the channel resistance. The designed size of the active region on the photomask was 91 μm × 40 μm. The designed channel length was 1 μm, the JFET length was 1 μm, and the source length was 2 μm. We adopted a single-layer electrode structure to avoid the complicated process of stacked electrodes. The source parasitic resistance of a single-layer electrode structure was large compared to the stacked electrode in vertical contact with the source implanted region because the source electrode of a single-layer electrode structure is in contact with the active region at a position besides the horizontal direction.

Firstly, Mg ions were selectively implanted on the 10-μm-thick n-GaN layer grown by MOCVD on the n-type GaN (0001) substrates. The net donor concentration of the n-GaN epitaxial layer was around 1×10^{16} cm^{-3}. Mg ions were implanted with 10 to 700 keV with a total dose of 6.5×10^{13} cm^{-2}. The Mg concentration near the surface was adjusted to control V_{th} to about 3 V. Additionally, increasing the Mg

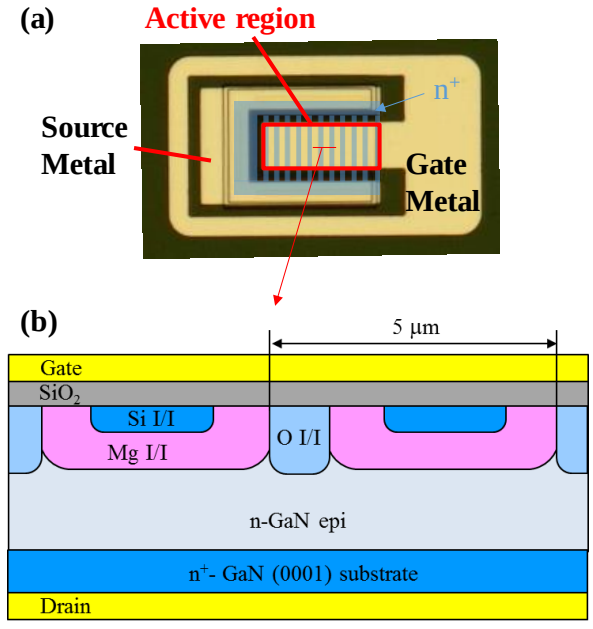

Fig. 7. Schematic images of vertical GaN planar-gate MOSFETs with all ion implantation process. (a) plan view, (b) cross sectional image of active region.

concentration in the deep region provided a sufficiently thick p-well region. Afterwards, N ions were implanted sequentially with 10 to 600 keV and a total dose of 6.7×10^{13} cm^{-2}. Secondly, Si ions were selectively implanted into the source regions with 15 to 40 keV and a total dose of 1.9×10^{15} cm^{-2}. Thirdly, O ions were selectively implanted into the JFET region with 10 to 700 keV and a total dose of 2.3×10^{13} cm^{-2} to reduce the JFET resistance.

After triple I/I, the wafers were annealed at 1300 °C for 5 minutes in a N_2 atmosphere at standard pressure with AlN encapsulation cap. Finally, the AlN cap was chemically removed.

Then a plasma-CVD apparatus with TEOS gas deposited a 100-nm-thick SiO_2 layer at 300 °C. Titanium and aluminum were used as the gate, source, and drain metal, while nickel was used as the body contact metal. Forming gas annealing was performed at 400 °C for 30 min.

In Fig. 8, it is shown the I_d-V_d output characteristics on fabricated GaN vertical MOSFET. The fabricated GaN vertical MOSFETs showed normal MOS channel behaviors such as a suitable drain current control by the gate voltage, good ohmic contact, and a low gate leakage current ($<1.0\times10^{-3}$ A cm^{-2}). In Fig. 9, it is shown the breakdown measurement of the fabricated GaN vertical MOSFET. The

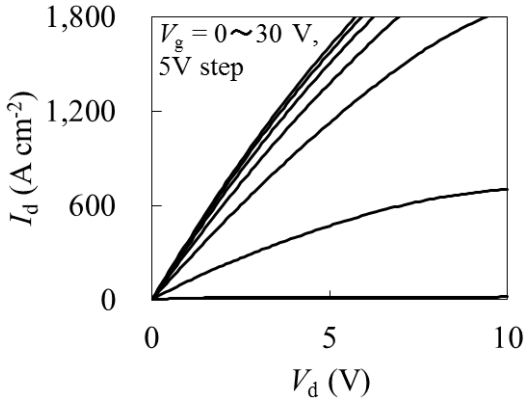

Fig. 8. I_d-V_d output characteristics of fabricated GaN vertical MOSFET [10].

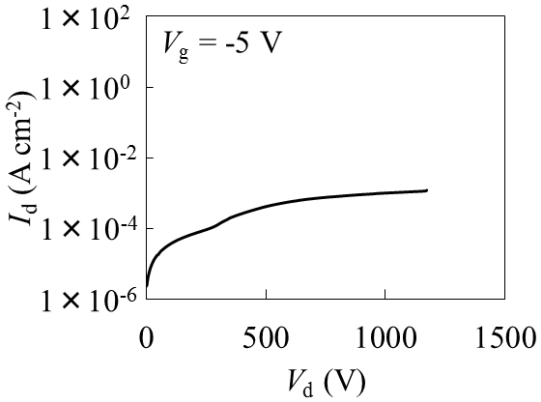

Fig. 9. I_d-V_d breakdown measurement of fabricated GaN vertical MOSFET [10].

fabricated GaN vertical MOSFET catastrophically broke down around 1200V. The V_{th} determined as a gate bias intercept of the linear extrapolation of I_d was about 3 V. However, the threshold voltage of the subthreshold region was negative. Hence, the breakdown voltage was measured while applying -5 V to the gate electrode. The drain leakage current at 1000V is less than 1.0×10^{-3} A cm^{-2}.

The specific on-resistance determined from the slope of the I_d-V_d curve at V_g = 30 V and V_d = 1 V was 2.78 mΩ cm^2. In consideration of the current spread in the drift layer, the area of the active region used to calculate the specific on-resistance was set to 101 μm × 50 μm by adding the drift layer thickness (10 μm) to the designed size of the active region. As described above, we adopted a single-layer electrode structure in this demonstration, so the source parasitic resistance was large compared to the stacked electrode structure. The effective specific on-resistance of the active region was estimated to be about 1.4 mΩ cm^2 by subtracted the source parasitic resistance. This on-resistance is lower than commercially available SiC MOSFETs. Therefore, the vertical GaN planar-gate MOSFETs with high breakdown voltage and low on-resistance could be realized by I/I process.

5. Investigation of p-type high-concentration layer for p-ohmic formation

In order to realize highly reliable GaN vertical MOSFET, it is essential to form a good p-type ohmic contact for fixing a potential of p-well region and extracting hole. For p-type ohmic contact formation, a highly doped p-type layer is generally required. However, when Mg of 1×10^{19} cm^{-3} or more is implanted into GaN and annealed for activation, Mg clusters occur, and the Mg concentration in the GaN matrix decreases to about 3×10^{18} cm^{-3} [17].

In order to suppress Mg clusters and form a p-type high concentration layer by I/I, we tried to clarify the formation mechanism of Mg clusters [18]. It was expected that the Mg concentration and implantation defects are related to Mg cluster formation, but both of them changes simultaneously depending on the Mg dosage. Therefore, by implanting an inert element into the p-type GaN epitaxial layer, we controlled the amount of implanted defects and the Mg concentration, independently.

A 1-μm-thick n-GaN layer and a 500-nm-thick p-GaN layer were epitaxially grown by MOCVD on the n-GaN substrate sequentially. The net donor concentration of n-GaN epi-layer was around 1.0×10^{16} cm^{-3} and the Mg concentration of p-GaN epi-layer was around 1.0×10^{19} cm^{-3}. N ions were implanted with 15 to 350 keV and a total dose of 6×10^{14} and 1.8×10^{15} cm^{-2} to form a 500-nm-depth BOX profile with 1×10^{19} and 3×10^{19} cm^{-3}, respectively. After N I/I, the wafers were annealed at 1300 °C for 5 minutes in a N_2 atmosphere at atmospheric pressure with an AlN encapsulation cap.

In Fig. 10, it is shown the Mg profile after annealing. In the sample without N I/I, annealing does not cause Mg diffusion, however, in the N I/I sample of 1×10^{19} cm^{-3}, Mg

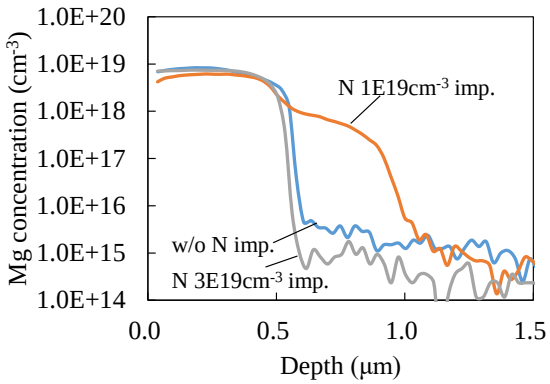

Fig. 10. Mg profiles of p-GaN epitaxially grown samples after annealing

diffused and the Mg concentration increased in the depth of 0.5 to 1 μm. On the other hand, no Mg diffusion occurred in the N-implanted sample of 3×10^{19} cm^{-3}. In Fig. 11, it is shown the cross-sectional low-angle annular dark-field (LAADF)-STEM images and three dimensional Mg atom maps obtained by 3D atom probe (3DAP) technique of the annealed samples. There were no defects or clusters in the sample without N I/I, however, many defects occurred in the N-implanted samples. Mg clusters were formed in the N-implanted sample of 1×10^{19} cm^{-3} but not formed in the sample of 3×10^{19} cm^{-3}.

According to the first-principles calculation of the formation energy of Mg in GaN, the formation energy of Mg

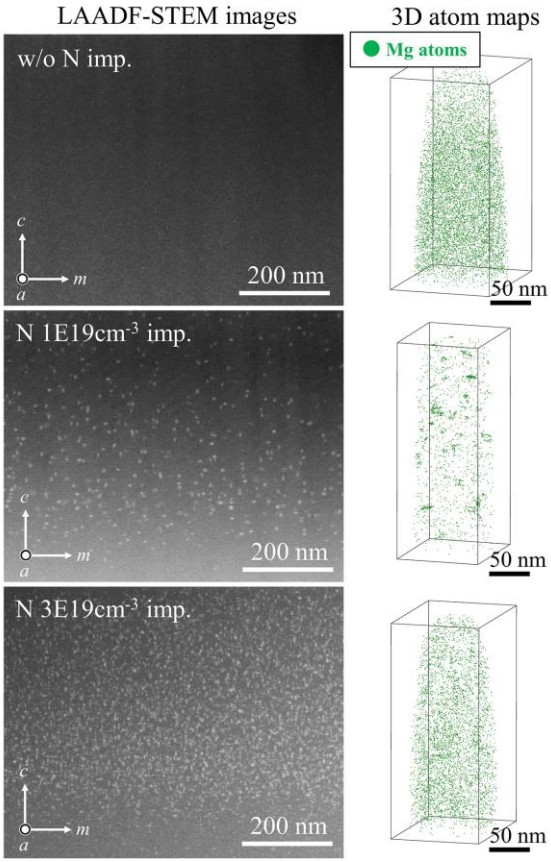

Fig. 11. LAADF-STEM images and 3D atom maps obtained by 3DAP of p-GaN epi-layer after annealing

acceptors increases as the Fermi level approaches the conduction band [19]. Assuming that a driving force for Mg clustering and diffusion is generated by an increase in the formation energy of Mg acceptors, it is considered that the Mg clustering and diffusion tend to occur as the number of Mg acceptors increase. However, high-concentration p-type epitaxial layer without N implantation does not cause Mg clustering and diffusion even after high temperature annealing. This result suggests that dislocations and defects mediate the migration of Mg, and Mg cannot move without dislocations and defects even though the driving force is generated. On the other hand, Mg clustering and diffusion do not occur even in the sample implanted with high concentration N. This result suggests that too many defects were formed by high concentration N implantation and could not be recovered sufficiently by annealing, and the p-type epitaxial layer changed to i-type, resulting in a decrease in the formation energy of Mg acceptors. Therefore, it is theoretically quite difficult to form a p-type high-concentration layer by ion implantation. To solve this issue and form a p-type high concentration layer by I/I, it is considered effective to reduce dislocations and defects before activation annealing, or to perform activation annealing while inactivating Mg acceptors.

Based on the above considerations, we recently reported a study on shallow implantation at low energy to suppress defect introduction by I/I [20].

Mg and N ions were implanted on the n-GaN epitaxial layer grown by MOCVD on the n-GaN (0001) substrate. The donor concentration of n-GaN epitaxial layer was around 1×10^{16} cm^{-3}. Mg and N ions were selectively implanted with 10 keV with a dose of 9×10^{13} cm^{-2}. After Mg and N I/I, the wafers were annealed at 1300 °C for 5 minutes in a N_2 atmosphere at atmospheric pressure with an AlN encapsulation cap. Finally, the AlN cap was chemically removed. Nickel and gold were used as p-contact (anode) electrode. Titanium and aluminum were used as cathode electrode.

In Fig. 12, it is shown the Mg profile of Mg and N shallowly implanted samples. In the Mg-only implanted sample, intense Mg diffusion occurred during annealing, and

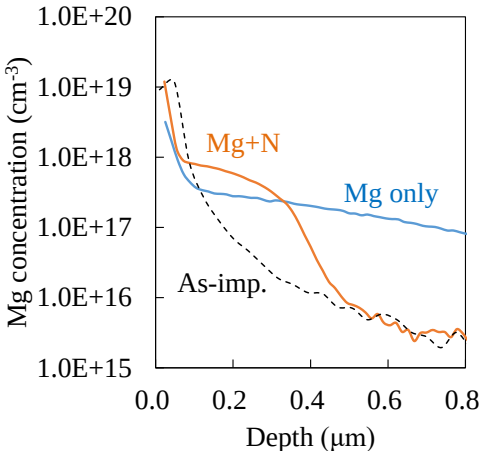

Fig. 12. Mg profiles of shallowly implanted samples

the Mg concentration near the surface decreased to around 3×10^{18} cm^{-3}. On the other hand, in the Mg and N implanted sample, the Mg diffusion was suppressed and the Mg concentration near the surface was maintained above 1×10^{19} cm^{-3} even after annealing. Furthermore, from the 3DAP analysis, it was confirmed that the Mg concentration in the GaN matrix was maintained at 1×10^{19} cm^{-3} or higher.

In Fig. 13, it is shown the results of TLM measurement of the shallowly implanted samples. Almost no current flowed in the Mg-only implanted sample. On the other hand, a current corresponding to the electrode spacing was confirmed in the Mg and N implanted sample although it has the Schottky-like contact characteristics. This result suggests that the shallow and high-concentration Mg-implanted layer was highly p-type activated. In the future, we will investigate the improvement of contact characteristics by further improvement of the I/I conditions and electrode formation conditions.

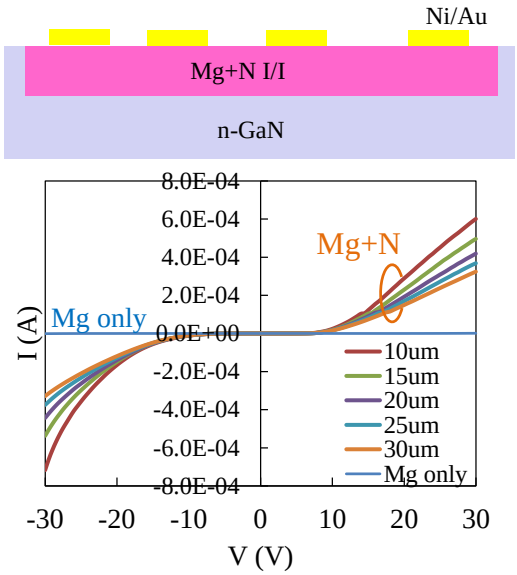

Fig. 13. TLM measurement of shallowly implanted samples

6. Conclusions

We have developed the p-type I/I technique into GaN and demonstrated the vertical GaN planar-gate MOSFETs with high breakdown voltage and low on-resistance fabricated by I/I process. We confirmed that good MOSFET characteristics were obtained by forming active regions such as p-well, source, and JFET region by I/I.

On the other hand, there are still many challenges for realizing practical GaN vertical MOSFETs such as further activation of I/I layer, improvement of hole conductivity, control of MOS channel characteristics, and reliability. Therefore, continuous development is necessary.

Acknowledgements

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