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Locally Doped Transferred Contacts for WSe_2 Transistors

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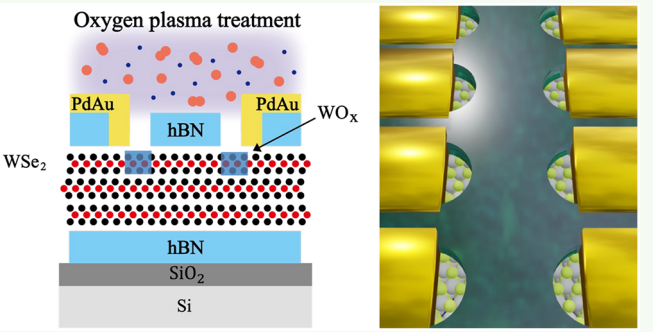
ABSTRACT: While two-dimensional (2D) materials have shown great promise for scaling technology nodes beyond the limits of silicon devices, key challenges remain for realizing high-quality and practical 2D field-effect transistors (FETs), including lowering contact resistance, demonstrating device structures with high electrical stability, reducing interface charge trapping, and integrating n- and p-FETs for beyond-complementary metal oxide semiconductor devices. High contact resistance often stems from Schottky contacts and Fermi level pinning and can be reduced by local doping or transferred contacts, respectively. However, these approaches to date have been mutually incompatible. Here, we combine both into a single structure and demonstrate a locally doped, transfer-contact stack containing access regions adjacent to the metal via contacts embedded in hexagonal boron nitride. Doping is applied by oxygen plasma treatment of access regions, while the fully encapsulated WSe_2 channel remains pristine, creating a lateral p^+-i-p^+ junction. We demonstrate a reduction in contact resistance by up to >30,000 times with the contact strategy, with a lowest individual contact resistance of ~3.6 kΩ · μm, limited by the doping density at the contacts. Our results highlight increasing doping in the contact region as being crucial for achieving improved contact resistance in p-type WSe_2 devices. For our FET devices, the geometry of gates, doped access regions, and the channel are all defined by an electron beam lithography giving full and precise control over size and position. The p-FET behavior is strongly enhanced with a high on/off ratio up to 10^7, but ambipolar characteristics from the intrinsic channel are still retained. Negligible, temperature-independent hysteresis is achieved from T = 10 to 300 K, with only back gate carrier control. High electrical stability is evident in the excellent reproducibility of transfer characteristics between multiple contact sets on a single device and different devices. The doping reduces contact resistance by reducing the Schottky barrier height and width, achieving Ohmic IV characteristics. The doping appears very stable, with negligible degradation of performance, keeping the device for 50 days in atmosphere. This reasonably simple device structure incorporates two important strategies to enhance contact quality, improving p-FET performance and retaining intrinsic channel quality.



KEYWORDS: *Two-dimensional, transition metal dichalcogenides, tungsten diselenide, oxygen plasma, p-type doping, hole injection, field effect transistor, tungsten oxide*

INTRODUCTION

Two-dimensional (2D) materials have been revolutionizing fundamental research and technology by the presence of remarkable physical and electric properties in a naturally ultrathin body down to a single monolayer. Graphene, perhaps the most widely researched of the 2D material family, possesses distinctive electrodynamic and transport properties;[1−3] however, the zero bandgap makes it unsuitable for logic operations. In response, semiconducting 2D transition-metal dichalcogenides (TMDs) have emerged with significant potential in transistor applications and as a possible solution for the scaling of such technologies.[4] Challenges for silicon devices stem from interface effects including surface roughness and dangling bonds that degrade carrier mobility, or short channel effects,[5] whereas 2D TMDs are free from dangling bonds, can be integrated with ultrasmooth 2D dielectrics such as hexagonal-boron nitride (hBN),[6] and retain high mobility in the ultrathin limit, thereby overcoming the performance degradation that occurs for silicon devices as body thickness and channel length are reduced in the few nanometer limit.[7]

However, despite their significant potential, challenges remain for high-performance TMD field-effect transistors (FETs),[8] including contact resistance, reducing charge trapping from interface stages, and integrating both n- and p-

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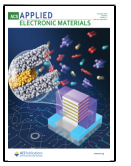

behavior for complementary metal oxide semiconductor (CMOS) applications.[9] For p-type FETs in particular, contact quality and the metal−semiconductor interface are crucially important, where interface effects can significantly impact contact resistance, semiconductor polarity, and subthreshold swing (S.S.). Issues may include interfacial roughness, contaminants/defects, and Fermi-level pinning (FLP) with the formation of metal-induced gap states (MIGS), interface dipoles, and disorder-induced gap states (DIGS).[10] Reducing the height and/or width of the subsequent Schottky barrier at the metal−semiconductor interface is crucial to lowering contact resistance, and strategies to mitigate these issues can be broadly grouped into interface/contact engineering,[11−15] surface treatment,[16] and the use of suitable contact metals with optimized work functions.[12,17,18] In particular, there is currently intense interest in two specific methods that improve contact quality and enhance p-FET performance, namely, (1) transferred contact integration[11,19−21] and (2) surface charge transfer doping by oxygen plasma treatment.[16,22−27] So far, these techniques have only been used separately; here, we combine both in a single structure. Relying on either method alone has disadvantages; for example, doping techniques have previously been combined with direct metal evaporation of contacts, which has potential to damage the 2D material.[20,28] On the other hand, transferred contacts have not yet been integrated with highly doped contact areas. Our hybrid approach applies oxygen plasma doping locally to the contact regions within a transferred contact structure, improving contact resistance while maintaining the high quality of the WSe_2 channel. The channel remains encapsulated in hBN, thereby retaining pristine characteristics, while gate-adjacent regions are oxidized to tungsten oxide (WO_x),[24,29,30] creating a p-doped access region between the metal and the semiconducting channel. We achieve strongly enhanced p-FET behavior in ambipolar, ultrathin, three-layer (3L) WSe_2 FETs and demonstrate negligible temperature-independent hysteresis, indicating a low trap density with only back-gate control. The device shows excellent electrical stability, with highly reproducible transfer curves between different devices as well as for multiple contacts on the same device. We also show excellent stability over time for at least 50 days in atmospheric conditions.

RESULTS AND DISCUSSION

The device concept is shown in Figures 1(a) and (b), and optical micrographs of two samples are given in Figures 1(c) and (d). Holes are etched in a hBN flake, and metal contacts defined by electron beam (e-beam) lithography create the via contacts. After evaporation and lift-off, the metal partially covers the holes leaving a gap for local doping. The structure is assembled by a dry transfer process which avoids contacting the 2D material with processing contaminants, preserving its high pristine quality, and WSe_2 exfoliation and device assembly is carried out inside a glovebox. Exposing the device to mild oxygen plasma oxidizes the WSe_2 surface layer in the access region to form the WO_x surface charge transfer doping layer. Parameters are chosen to ensure that only the top WSe_2 layer is oxidized, as described in Supporting Information. A simplified process flow is outlined in Figures 1(e) to (k), and a detailed description is given in Methods. In particular, the etching approach is able to create high-quality smooth arbitrary structures in hBN.[31,32] The WSe_2 thickness is identified as trilayer for both devices by atomic force

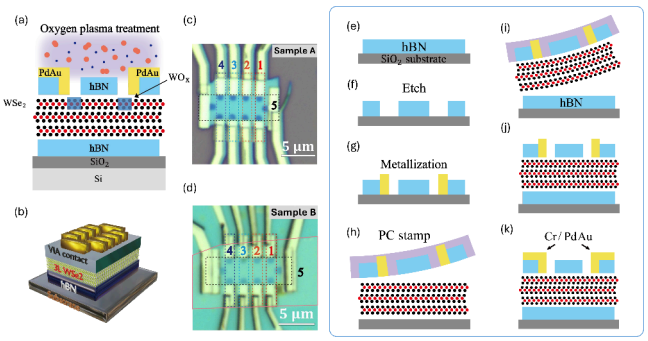

Figure 1. (a, b) Schematic device structure illustrating WO_x formation after oxidation and 3D cartoon image, respectively. (c, d) Optical images of samples A and B, respectively. Sets of two-terminal contact groups are labeled 1 to 5. In (d), the WSe_2 location is outlined for clarity. (e−k) Basic step-by-step fabrication process. An hBN flake around 30 nm is selected for via contact preparation and patterned with etched holes. Metal (PdAu) is deposited partially covering the holes leaving an open region for selective area doping. A PC/PDMS stack is used to transfer the hBN/via contact layer onto trilayer WSe_2, and then both layers are transferred onto a bottom hBN flake to encapsulate the device. Finally Cr/PdAu is deposited connecting via contacts to bond pads.

microscopy (AFM), Raman spectroscopy, and photoluminescence (PL) spectroscopy, as shown in Figures S1 and S2.

Distinctive advantages of our device structure include precise and full control over the size and location of the doping area and the intrinsic channel length/geometry, since all etching and metal deposition steps and their alignment are defined by electron beam lithography. Alternative techniques of separately transferring hBN masks[27,33,34] or hBN/top-gate stacks[35] onto the 2D TMD rely on user skill thus limiting control over the position and size of the doping area and the channel. Additionally, there is potential for contamination of the FET channel when the TMD and hBN are transferred in separate steps, or when spin coating a photoresist mask layer.[36,37] Ours is a relatively simple method for 2D FET design incorporating transferred contacts and selective area doping, with potential for systematic and precise investigation of the impact of doped region and intrinsic channel geometry on electrical performance. The channel regions are fully encapsulated (above and below) with hBN, which is vital for ensuring pristine and atomically smooth interfaces with minimized surface defects.

Figure 2(a) shows transfer characteristics for sample A, before and after 60 s oxygen plasma treatment and red and blue traces, respectively. The oxidation process is performed using a reactive ion etching (RIE) system at room temperature, 15 sccm O_2 flow rate, and low power of 10 W to ensure oxidation is limited to the topmost WSe_2 layer for all exposure times used in this study. Post oxidation transfer characteristics show a significantly enhanced p-branch and clear off-state near back gate voltage V_{BG} = 0 V, with the p-FET enhancement arising from hole injection via surface charge transfer doping in the access regions. An n-branch is still observed at positive gate voltages, indicating that the intrinsic ambipolar nature of the mechanically exfoliated WSe_2 in the channel region is preserved, even after the p-doping process, and highlighting the efficacy of the encapsulation process. The ability to maintain both n- and p-type behavior within a single material could be advantageous for beyond-CMOS technologies,[9,38] where both behaviors are required, and where integrating the

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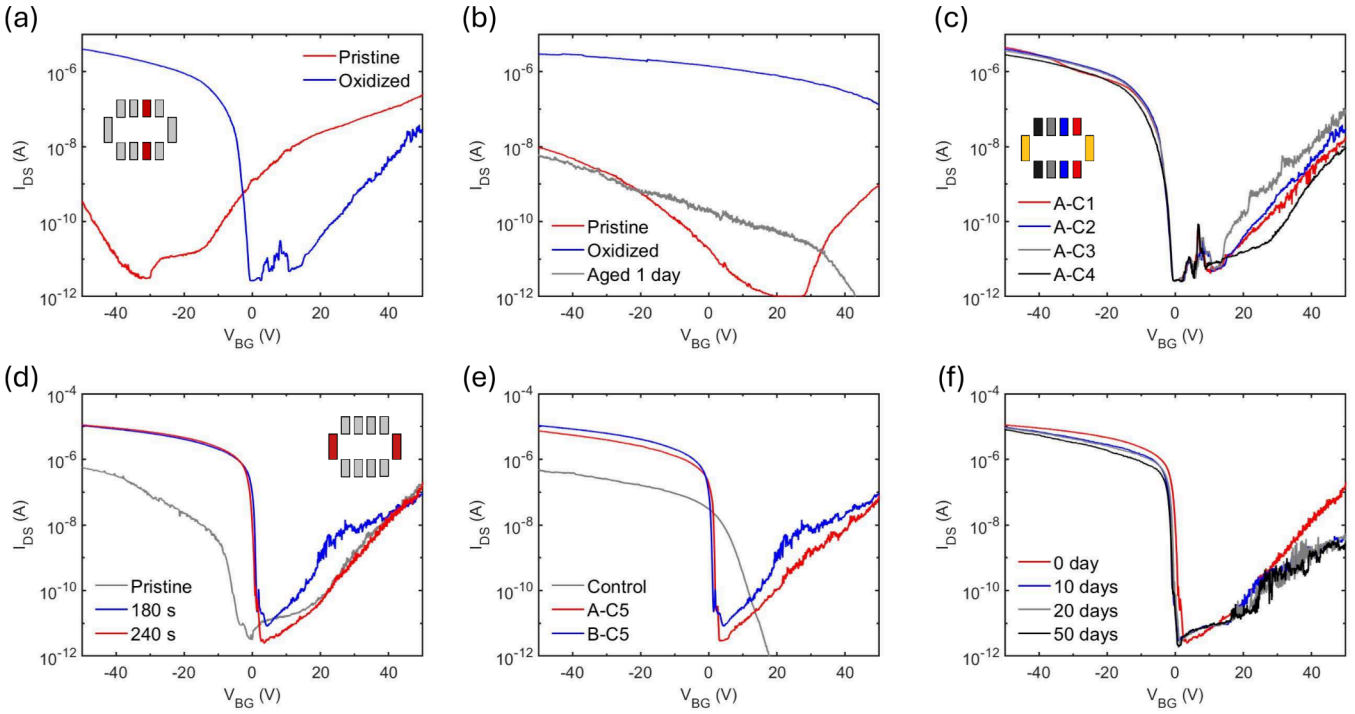

Figure 2. (a) Transfer characteristics of I_{DS} as a function of V_{BG}, sample A, before and after 60 s oxidation. Insets in (a) and (d) show schematic illustrations of contacts with the source-drain pair measured shown in red. Data are representative of device behavior since contact pairs show high reproducibility. (b) Transfer characteristics for a control device of unencapsulated WSe_2 on SiO_2/Si before and after 60 s oxidation, red and blue traces, respectively. The gray trace shows device behavior after exposure to atmosphere for 1 day. (c) Transfer characteristics measured for various contact arrangements in sample A, defined in the legend. The inset shows a schematic diagram of the contacts where colors correspond to different traces in the figure. (d) Representative transfer characteristics for sample B. Data are presented in the unoxidized condition (gray), after 180 s oxidation (blue), and after further 60 s oxidation (red). (e) Comparison of transfer characteristics for samples A and B and a second control device of unencapsulated WSe_2 on an SiO_2/Si substrate. Samples A and B are oxidized for 60 and 180 s, respectively. (f) Transfer characteristics for sample B after the second oxidation (total cumulative oxidation time 240 s) and after being left at atmosphere in a desiccant cabinet for 10, 20, and 50 days. Data in (e) and (f) are measured for the same contact arrangement as (d).

two may help reduce device footprint and enable more versatile applications.

For comparison, Figure 2(b) shows transfer characteristics for a control device of few-layer WSe_2 on a SiO_2/Si substrate without hBN encapsulation. Prior to oxidation, the pristine WSe_2 displays ambipolar transport (red trace). In contrast to the locally doped transferred contact stacks, the entire surface is exposed to oxygen plasma, and the current does not turn off within the measurement range. This example illustrates the essential requirement for local area doping for functional p-type WSe_2 FETs with the threshold voltage (V_{th}) within an acceptable measurement range. The control device also shows rapid degradation over time; the gray trace shows transfer characteristics after the device is placed in atmospheric conditions for 1 day, with significantly lower current and V_{th} drift indicating surface deterioration and changes in doping levels.

In contrast, exceptionally high electrical stability is demonstrated for our locally doped transferred contact devices, in terms of high reproducibility both between multiple contact sets on a single device and for different devices, as well as in negligible degradation over time. Figure 2(c) shows two-terminal transfer characteristics for different contact groups on sample A. The turn-on behavior, on state-current, and V_{th} are exceptionally similar.

Sample A was oxidized for 60 s initially, as this is sufficient to convert the top WSe_2 layer to WO_x (Supporting Information Figures S1, S2, and S3). However, after this step, the IV sweeps remain slightly asymmetric, as will be discussed with reference to Figure 4. Therefore, additional oxidation steps of 60 s each were performed, with a total oxidation time of 180 s resulting in more uniform doping and quasi-ohmic contacts. Based on this finding, sample B was initially oxidized for 180 s, followed by a further 60 s to increase the uniformity of IV characteristics, although transfer characteristics following both oxidation steps are very similar.

The transfer characteristics for sample B are listed in Figure 2(d). Similar to sample A, the p-branch is strongly enhanced after oxidation with V_{th} close to V_{BG} = 0 V. Transfer characteristics are also highly reproducible between samples A and B as shown in Figure 2(e), and data are shown after their initial oxidation steps of 60 and 180 s, respectively. For comparison, data are shown from a second control device of WSe_2 on a SiO_2/Si substrate, also oxidized for 60 s, which shows shallower turn on, lower on current, and the absence of an n-branch at positive V_{BG}. Since electrical stability is a key issue for doped 2D materials,[39,40] sample B is measured for up to 50 days after the second oxidation step. Figure 2(f) shows transfer characteristics as a function of day number, while keeping the device in the atmosphere in a desiccant cabinet. Remarkable air stability is achieved with negligible change in the off current, on current, or V_{th} position.

After oxidation, the channel resistance (R_{CH}) and the combined resistance of the metal−semiconductor contacts and doped access regions ($2R_C + 2R_{acc}$) are estimated from four-point measurements, with data presented in Figure S4. It is not

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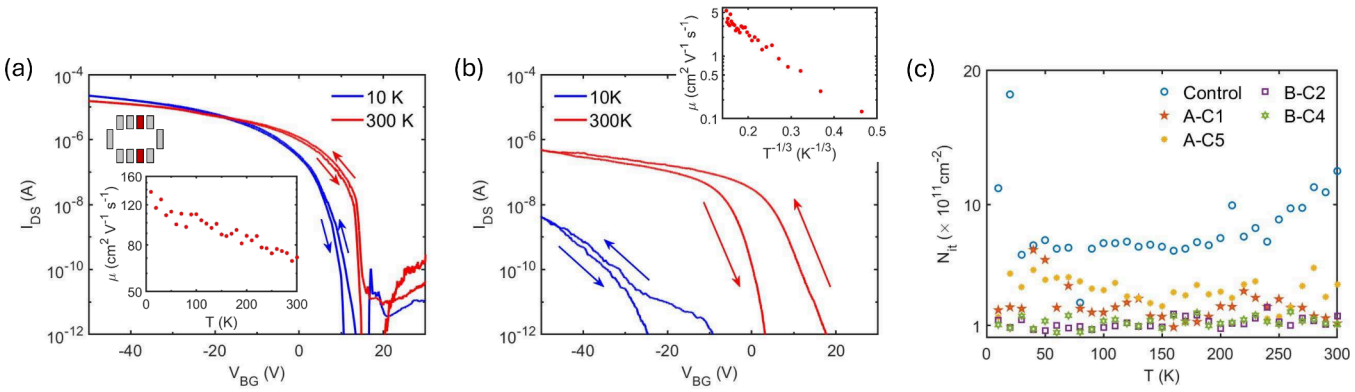

Figure 3. Hysteresis characterization. (a) Transfer characteristics for sample B at T = 10 and 300 K, for sweep rate ∼0.24 V s^{-1}. The arrows indicate the sweep directions. Insets: Contacts measured (red) and mobility as a function of temperature at V_{BG} = −50 V. (b) Transfer characteristics of a control device of WSe_2 on a SiO_2/Si substrate at T = 10 and 300 K. Inset: linear relation between $\ln(\mu)$ as a function of $T^{-1/3}$ at V_{BG} = −50 V. (c) Carrier trap density for samples A and B and the control device as a function of temperature. Labeling, e.g., "A-C1" refers to sample (A or B) and contact pair as defined in Figures 1(c) and (d).

possible to separate $2R_C + 2R_{acc}$ to independently estimate contact resistance; therefore, separate devices are fabricated without an hBN capping layer so that there are no transitions between doped and undoped regions after oxidation, thereby allowing the contact resistance to be extracted.[27,34] We estimate a minimum individual contact resistance $R_C \sim 3.6$ kΩ · μm and a maximum resistance reduction from the pristine state of up to >30,000 times, shown in Figures S5 and S6. Plotting contact resistance as a function of doping density, Figure S6(d) shows a clear trend of reduced resistance with higher doping density, indicating that the contact resistance of our devices is limited by the doping level achieved through our oxidation process, $p_{2D} \sim 1.2 \times 10^{13}$ cm^{-2}. This is consistent with the current lowest reported contact resistance from surface charge transfer doping by surface oxidation of $2R_C \sim 0.642$ kΩ · μm being obtained at a higher doping density of 3.94×10^{13} cm^{-2}. The oxidation strategy used ozone plasma treatment for 30 min at an oxygen flow rate of 3 L/min, for Pd/Au contacts in exfoliated three-layer WSe_2.[27] This relationship highlights increasing doping at the contacts as essential for achieving low contact resistance. For context, other reported values of individual contact resistance R_C range from ∼0.9−6.1 kΩ · μm;[41] ∼1.4 kΩ · μm;[30] ∼1.45 kΩ · μm;[35] ∼3−4 kΩ · μm;[24] ∼3.6 kΩ · μm[34] for exfoliated WSe_2 flakes, and ∼40 kΩ · μm for metal−organic chemical vapor deposition (MOCVD) grown bilayer WSe_2,[15] and on/off ratio up to 10^5.

For a broader contextual comparison, various other strategies have been employed with the goal of achieving low-resistance contacts for p-type WSe_2 FETs. An ultralow contact resistance of 0.5 kΩ · μm was achieved using an epitaxially grown VSe_2 contact layer on bilayer CVD-grown WSe_2. The transistors were located between naturally occurring cracks in the VSe_2 layer, which formed van der Waals (vdW) contacts,[42] and devices demonstrated very high on-currents up to 1.72 mA· μm^{-1} and on/off ratios up to 10^6. An alternative charge transfer doping strategy, integrating few-layer α-$RuCl_3$ at the contact regions in monolayer WSe_2 transistors, achieved a contact resistance of ∼4 kΩ · μm, with an on-current of 35 μA· μm^{-1} and on/off ratio exceeding 10^9.[43] Near-ideal vdW interfaces between TMDs and contact electrodes have also been demonstrated using metal evaporation techniques, where carefully minimizing radiative heating led to a low contact resistance of ∼3.3 kΩ · μm for Pt contacts to multilayer CVD WSe_2, with saturation currents >10 μA · μm^{-1} and an on/off ratio of 10^7. This resistance increased to ∼229 kΩ · μm for monolayer WSe_2, attributed to a higher Schottky barrier due to the elevated position of the valence band edge.[44] For the transferred contacts approach to contact integration, Pt contacts embedded in hBN achieved a low contact resistance of ∼5 kΩ · μm for monolayer WSe_2, with an on-state current of 7.4 μA · μm^{-1} and an on/off ratio of 10^8.[45] In another study, bilayer WSe_2 p-FETs using transfer contacts demonstrated a contact resistance of ∼3.5 kΩ · μm with Pt as the contact metal, achieving an on/off ratio of 10^6 and an on-current of 5 μA · μm^{-1}.[20]

Returning to the electrical characteristics of our locally doped via contact stacks. Devices display negligible hysteresis independent of temperature; Figure 3(a) shows typical forward and backward transfer characteristics for sample B at T = 10 and 300 K. Similar characteristics are observed for sample A as shown in Figure S7(a). For context, noticeable hysteresis has previously been observed for plasma-doped samples with back-gate control, which modulates carriers in the contact regions, doped areas, and the channel. In these studies, devices were fabricated on SiO_2 substrates, i.e., without hBN encapsulation. For example, in ref 46, significant hysteresis was present for a gate voltage sweep range of ±70 V, attributed to interface trap charges, becoming almost negligible for a ±20 V sweep range. In a separate study, noticeable room-temperature hysteresis became negligible below $T \sim 50$ K for back-gated samples, whereas top-gated samples showed negligible hysteresis across all temperatures. This led to the conclusion that the hysteresis was primarily due to water trapped at the WSe_2/SiO_2 interface.[33] Significant hysteresis has also been observed for a WSe_2 device with the entire surface exposed to oxygen plasma, but it became negligible for devices with hBN covering the channel region.[34] This is consistent with other studies showing that capping layers can significantly reduce hysteresis, as demonstrated in ref 18 using Al_2O_3 grown by atomic layer deposition (ALD). For transfer contact devices, negligible hysteresis can be achieved when devices are fully encapsulated with hBN and fabricated in a glovebox;[20] however, when the same devices are fabricated in air or when metal is directly evaporated through hBN vias, hysteresis becomes more pronounced.[20] Additionally, ref 45 reported low hysteresis of

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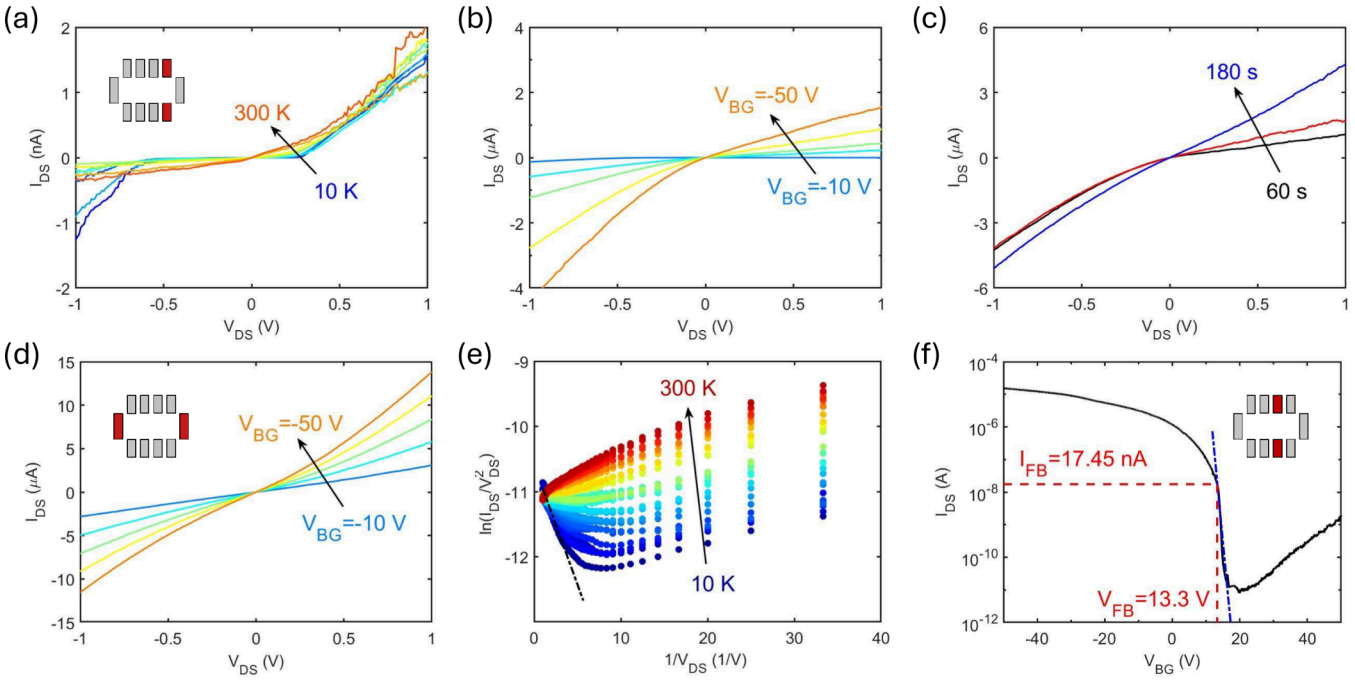

Figure 4. IV sweeps and Schottky barrier height/width extraction. (a) Pristine IV characteristics of sample A at V_{BG} = −50 V as a function of temperature, for the contact arrangement shown in the inset. (b, c) Corresponding IV characteristics after 60 s oxidation at fixed gate voltages from V_{BG} = −10 to −50 V in steps of −10 V and after different oxidation times at V_{BG} = −50 V, respectively, at T = 300 K. (d) IV characteristics of sample B after 240 s oxidation at fixed gate voltages from V_{BG} = −10 to −50 V in steps of −10 V at T = 300 K. The inset shows the contact arrangement. (e) Fowler-Nordheim (FN) plot of $\ln\left(\frac{I_{DS}}{V_{DS}^2}\right)$ as a function of $\frac{1}{V_{DS}}$ at T = 10 to 300 K in steps of 10 K. The linear fit to T = 10 K data (black dashed line) is used to estimate barrier width. (f) Corresponding transfer characteristics, the blue dash-dotted line shows a fit to the exponential subthreshold behavior. The deviation from this trend identifies the flat band current and voltage and thereby Schottky barrier height. This is subsequently used in (e) to extract barrier width by fitting data at 10 K using the FN-tunneling relation. (d, e) Data for sample B for the contact arrangement shown in the inset of (f). Data for other contacts are shown in Supporting Information.

<0.5% for transfer contacts with a gate voltage sweep range of ±100 V. Our device achieves negligible hysteresis consistent with high-quality transfer contact devices,[20] even with our inclusion of an etched access region in which the WSe_2 (WO_x) is exposed to the atmosphere prior to (and after) oxidation. This suggests good stability of the doped contact areas, and trap states within the WO_x do not negatively impact the channel characteristics of our devices.[39] Incidentally, a high on/off ratio is achieved for sample B, up to 1×10^7, Figure 3(a).

We compare samples A and B with a control device, where WSe_2 is directly transferred onto a SiO_2/Si substrate without hBN encapsulation. In contrast, the control device shows significant hysteresis, Figure 3(b), which we attribute to traps at the SiO_2/Si interface. Here the channel is fully encapsulated in hBN in comparison to previous reports where temperature-dependent hysteresis is observed for doped access regions in WSe_2 with back-gate control,[33] illustrating the significance for full encapsulation to improve device performance. To quantify the hysteresis we estimate a corresponding change in carrier density due to trapped charges[47] as $N_{it} = C_{ox}\Delta V_{th}/e$, where ΔV_{th} is the difference between forward and backward sweeps at I_{DS} around 10 pA, and C_{ox} is capacitance per unit area.[48] Figure 3(c) shows data for samples A and B and the control device. The control device shows the largest carrier trap density compared to samples A and B, which we attribute to the absence of an hBN layer between the WSe_2 and SiO_2 since inserting hBN can lower surface roughness and reduce disorder effects from trap sites in the SiO_2. Additionally the encapsulation fabrication method where WSe_2 is directly picked up by a top hBN layer likely results in cleaner interfaces and a lower trap density. We also measure the electrical hysteresis after sample B is aged for 50 days in atmosphere, and we find it continues to remain very low, as shown in Figure S8, Supporting Information. The IV characteristics over time are also given for completeness in Figure S9.

We also estimate the field effect mobility μ_{2P} by a simple two-point measurement. The mobility is extracted as $\mu_{2P} = Lg_m/w\, C_{ox}\, V_{DS}$, where the L is channel length, and w is channel width. The transconductance g_m is estimated from linear relation of transfer characteristics as $g_m = dI_{DS}/dV_{BG}$.[48] Highest room-temperature mobilities ~80 $cm^2\ V^{-1}\ s^{-1}$ are obtained for sample B with a trend of increasing mobility with decreasing temperature. A typical example is shown in Figure 3(a) inset. Data for other contacts on sample B and for sample A are shown in Figure S7. For comparison, we estimate a room-temperature mobility for sample B using a four-point (4P) measurement of around 145 $cm^2\ V^{-1}\ s^{-1}$. The higher 4P estimate is consistent with inclusion of channel and contact resistance in the two-point measurement.[16,48] As shown in Figure 3(b) inset, the mobility for the control device shows a linear trend in $\ln(\mu)$ as a function of $T^{-1/3}$, consistent with 2D variable range hopping from disorder-induced localized states.[49,50] This can be attributed this to greater disorder from surface roughness, dangling bonds, and impurities creating traps at the WSe_2/SiO_2 interface.[51]

Reducing the Schottky barrier (SB) is essential to reducing contact resistance.[9] We find a reduction of both barrier height

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and width for the locally doped transferred contact stacks, evidenced in analysis of tunneling mechanisms and also in greater hole injection, i.e., higher hole currents after oxidation. We note that the utilization of transferred contacts[11,20] and surface charge transfer doping from WO_x formation[16,29] can both lead to Fermi-level depinning and reducing the SB, although estimating the pinning factor requires comparison of different metal work functions.[11,29] Prior to oxidation, i.e., in the pristine condition, low-temperature data typically shows flat regions around V_{DS} = 0 V characteristic of tunneling behavior, as shown in Figure 4(a) for sample A. Corresponding IV characteristics as a function of V_{BG} after 60 s oxidation are shown in Figure 4(b). The behavior is slightly asymmetric around V_{DS} = 0 V but is neither strictly ohmic nor Schottky and may suggest the doping concentration in the access regions may be nonuniform or potential barriers at the source and drain contacts may be asymmetric. We therefore perform repeat O_2 plasma oxidation steps for 60 s each time, as shown in Figure 4(c), and the total oxidation time is given in the legend. A linear trend appears after 180 s oxidation, suggesting more uniform doping concentration and nearly ohmic contacts. Similar data are obtained for other contacts to sample A, as shown in Figure S11. Sample B is therefore exposed to an initial 180 s oxygen plasma treatment. However, we find that a further 60 s of oxidation is required to produce more symmetric and quasi-ohmic characteristics, as shown in Figure 4(d). We speculate that if there is any directionality to exposure during the oxygen plasma treatment process, the depth of the etched holes may cause shadowing of particular regions and therefore nonuniform exposure, necessitating the need for a second oxidation step to produce more uniform doping despite the 180 s initial exposure time. This could potentially be investigated by mounting the sample on an angled stage and continuously rotating it during the oxidation process to ensure uniform plasma exposure across all regions. Additionally, oxidation parameters such as plasma power, flow rate, and exposure time could be further optimized to improve uniformity. Reducing the thickness of the top hBN capping layer may also help minimize any shadowing effects.

To further investigate the transport mechanisms, data are represented in Fowler-Nordheim (FN) plots, i.e., $\ln\left(\frac{I_{DS}}{V_{DS}^2}\right)$ as a function of $\frac{1}{V_{DS}}$. Representative data for sample B are shown in Figure 4(e). Briefly, transport through a tunnel barrier at low T, i.e., where thermionic emission is negligible, can be characterized either by direct tunnelling (DT) or FN tunneling.[52,53] This analysis was initially motivated by the observation of tunneling-like characteristics in Figure 4(a). Direct tunnelling, where current tunnels through the entire width of the barrier at low source-drain bias, is described by

$$\ln\left(\frac{I_{DS}}{V_{DS}^2}\right) \sim \ln\left(\frac{1}{V_{DS}}\right) - \frac{2d\sqrt{2m\phi}}{\hbar} \quad (1)$$

For sufficiently high source-drain bias, FN tunneling occurs and current tunnels through a triangular region at the top of the barrier expressed by

$$\ln\left(\frac{I_{DS}}{V_{DS}^2}\right) \sim -\frac{4d\sqrt{2m\phi^3}}{3\hbar e}\frac{1}{V_{DS}} \quad (2)$$

where d is barrier width, m is effective mass, ϕ is barrier height, $\hbar$ is the reduced Planck constant, and e is the unit of electronic charge. Our devices show a transition from DT to FN tunneling as bias increases, Figure 4(e). Data for sample A corresponding to Figure 4(a) are plotted in an FN manner in Figure S10, and data for other contact groups for sample B are shown in Figure S12. We estimate the slope of the lowest temperature data, T = 10 K in the FN regime, indicated by the dashed black line in Figure 4(e). The lowest available T data is used to remove the contribution of thermionic emission, and the slope can be related to barrier height ϕ and barrier width d according to eq 2. We first independently estimate barrier height ϕ is from transfer characteristics at flat band current and voltage as shown in Figure 4(f).[27,54,55] This value is then used in eq 2 to estimate d. Values between $\phi \sim 260$ to 315 meV and $d \sim 0.3$ to 0.7 nm are estimated for different contact groups on sample B, Figure S12. For comparison, the van der Waals gap that exists for transferred contacts ~0.3 nm.[29] Prior to oxidation, we estimate $\phi \sim 395$ meV and $d \sim 2.3$ nm for sample A, Figure S10. It has been suggested that a scenario where the WO_x region does not extend under contacts results in a reduction of the Schottky barrier width instead of height,[33] whereas extending far under contacts would change the barrier height rather than width. Our estimates appear to be a mix of these scenarios but with a larger relative change of d compared to ϕ, suggesting the barrier width change is the major mechanism for greater charge injection into the channel, and this device architecture and fabrication process mostly controls the barrier width. In our work, we employ high work function PdAu contacts, for which p-type characteristics are expected to dominate and the relatively high work functions of these metals facilitate hole injection. In light of previous studies,[11,12,16] metals with even higher work functions such as Pt may result in stronger p-type behavior for TMDs, along with higher on-currents due to improved hole injection efficiency. In the absence of Fermi-level pinning, using Pt could potentially further reduce the Schottky barrier height and, thus, enhance the p-FET performance. This presents a promising avenue for future work aimed at optimizing contact resistance and maximizing the device performance.

CONCLUSIONS

We have demonstrated a contact-doping approach compatible with transferred contacts, achieving dramatic contact resistance reduction and enabling negligible, temperature-independent hysteresis in transport measurements of WSe_2. In particular, the hole injection is greatly increased through the reduction of the Schottky barrier in WSe_2. High electrical stability is achieved both in terms of high reproducibility in transfer characteristics for different contact arrangements and different samples, as well as excellent air stability for up to 50 days at atmosphere. The results highlight the importance of heterostructure design for WSe_2 FETs, particularly the need for full encapsulation with a 2D dielectric when doped access regions are incorporated by selective oxidation. By defining access regions and contacts *a priori* in the hBN dielectric by electron beam lithography, we achieve precise control of the doped region location and size, as well as channel geometry. Incorporating contacts embedded in hBN directly transferred onto the WSe_2 material minimizes contamination and preserves the pristine nature of the TMD channel. This is a promising approach for the development of doped TMD structures with high-quality channel and contacts. Our results

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also highlight achieving higher-density doping at contacts as being highly important for achieving low-resistance p-type contacts for WSe_2.

METHODS

Device Fabrication and Characterization. WSe_2 from HQ graphene is mechanically exfoliated on a 285 nm SiO_2 substrate, and the trilayer WSe_2 is identified by optical contrast. The thickness is further confirmed by atomic force microscopy (AFM), Raman shift, and photoluminescence spectroscopy (PL) measurements, as described in Supporting Information. Hexagonal boron nitride (hBN) is also mechanically exfoliated on a SiO_2 substrate and annealed by ramping the temperature to 300 °C in 1 h, maintaining at 300 °C for 3 h, then naturally cooling to room temperature. Around 30 nm thick hBN is used for via contact fabrication. The via hole patterns are defined in the hBN using e-beam lithography after spin coating the chip with poly(methyl methacrylate) (PMMA) A4 photoresist. After developing, the hBN is etched using an Inductive Coupled Plasma (ICP) system with parameters Ar (20 sccm), O_2 (5 sccm), and SF_6 (20 sccm), for a total time of 120 s. The sample is then cleaned using Propylene Glycol (PG), acetone (ACE), then isopropanol (IPA) to remove the photoresist. The via contact metal pattern is then defined by e-beam lithography after spin coating the chip with PMMA (A4). Around 35−40 nm PdAu is deposited, partially covering the etched areas in the hBN such that a hole remains adjacent to the contacts for selective area doping. A lift-off process is used to remove unwanted metal by rinsing the chip in ACE then IPA. For the dry transfer process, Polydimethylsiloxane (PDMS) covered with a Polycarbonate (PC) thin film is used as a stamp and used to pick up the via contact hBN. We then pick up the trilayer WSe_2 and transfer to the bottom hBN flake, thus fully encapsulating the device. The entire stack is then annealed by heating to 300 °C in 1 h, maintaining at 300 °C for 1 h, and then allowed to cool naturally to room temperature. We used e-beam lithography to define contact metal tracks and bond pads, followed by e-beam evaporation of Cr/PdAu 10/80 nm. A final lift-off process is required to remove the unwanted metal. The gate electrode and etched hole layout and geometry are identical for samples A and B. The only difference is that sample A is etched into a rectangular shape to ensure the via contact metal crosses the WSe_2 edge. For sample B, the via contacts design is adjusted so that contacts cross the edge without an extra etching process.

Electrical Measurements. Electrical transport measurements are performed using a Keysight B1500A semiconductor parameter analyzer and LakeShore cryogenic probe station between 10^{-2} and 10^{-3} mBar.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.4c01574.

WSe_2 thickness calibration; Conductive properties of the WO_x oxide layer; Samples A and B channel and combined contact/access region resistance; Contact resistance estimate; Hysteresis and mobility estimates; Aging characteristics; Fowler-Nordheim analysis, sample A; Oxidation time dependence of IV characteristics; Schottky barrier height and width estimates (PDF)

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon Films. *Science* **2004**, *306*, 666−669.

(2) Zhang, Y.; Tan, Y.-W.; Stormer, H. L.; Kim, P. Experimental observation of the quantum Hall effect and Berry's phase in graphene. *Nature* **2005**, *438*, 201−204.

(3) Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Katsnelson, M. I.; Grigorieva, I. V.; Dubonos, S. V.; Firsov, A. A. Two-dimensional gas of massless Dirac fermions in graphene. *Nature* **2005**, *438*, 197−200.

(4) Wang, S.; Liu, X.; Zhou, P. The Road for 2D Semiconductors in the Silicon Age. *Adv. Mater.* **2022**, *34*, 2106886.
(5) Wang, S.; Liu, X.; Xu, M.; Liu, L.; Yang, D.; Zhou, P. Two-dimensional devices and integration towards the silicon lines. *Nat. Mater.* **2022**, *21*, 1225−1239.
(6) Huang, X.; Liu, C.; Zhou, P. 2D semiconductors for specific electronic applications: from device to system. *npj 2D Mater. Appl.* **2022**, *6*, 51.
(7) Patoary, N. H.; Xie, J.; Zhou, G.; Al Mamun, F.; Sayyad, M.; Tongay, S.; Esqueda, I. S. Improvements in 2D p-type WSe_2 transistors towards ultimate CMOS scaling. *Sci. Rep.* **2023**, *13*, 3304.
(8) Schram, T.; Sutar, S.; Radu, I.; Asselberghs, I. Challenges of Wafer-Scale Integration of 2D Semiconductors for High-Performance Transistor Circuits. *Adv. Mater.* **2022**, *34*, 2109796.
(9) Knobloch, T.; Selberherr, S.; Grasser, T. Challenges for nanoscale CMOS logic based on two-dimensional materials. *Nanomaterials (Basel)* **2022**, *12*, 3548.
(10) Liu, X.; Choi, M. S.; Hwang, E.; Yoo, W. J.; Sun, J. Fermi Level Pinning Dependent 2D Semiconductor Devices: Challenges and Prospects. *Adv. Mater.* **2022**, *34*, 2108425.
(11) Liu, Y.; Guo, J.; Zhu, E.; Liao, L.; Lee, S.-J.; Ding, M.; Shakir, I.; Gambin, V.; Huang, Y.; Duan, X. Approaching the Schottky−Mott limit in van der Waals metal−semiconductor junctions. *Nature* **2018**, *557*, 696−700.
(12) Ngo, T. D.; Yang, Z.; Lee, M.; Ali, F.; Moon, I.; Kim, D. G.; Taniguchi, T.; Watanabe, K.; Lee, K.-Y.; Yoo, W. J. Fermi-Level Pinning Free High-Performance 2D CMOS Inverter Fabricated with Van Der Waals Bottom Contacts. *Advanced Electronic Materials* **2021**, *7*, 2001212.
(13) Jang, J.; Ra, H.-S.; Ahn, J.; Kim, T. W.; Song, S. H.; Park, S.; Taniguch, T.; Watanabe, K.; Lee, K.; Hwang, D. K. Fermi-Level Pinning-Free WSe_2 Transistors via 2D Van der Waals Metal Contacts and Their Circuits. *Adv. Mater.* **2022**, *34*, 2109899.
(14) Zheng, Y.; Gao, J.; Han, C.; Chen, W. Ohmic Contact Engineering for Two-Dimensional Materials. *Cell Reports Physical Science* **2021**, *2*, 100298.
(15) Oberoi, A.; Han, Y.; Stepanoff, S. P.; Pannone, A.; Sun, Y.; Lin, Y.-C.; Chen, C.; Shallenberger, J. R.; Zhou, D.; Terrones, M.; Redwing, J. M.; Robinson, J. A.; Wolfe, D. E.; Yang, Y.; Das, S. Toward High-Performance p-Type Two-Dimensional Field Effect Transistors: Contact Engineering, Scaling, and Doping. *ACS Nano* **2023**, *17*, 19709−19723.
(16) Lee, K.; Ngo, T. D.; Lee, S.; Shin, H.; Choi, M. S.; Hone, J.; Yoo, W. J. Effects of Oxygen Plasma Treatment on Fermi-Level Pinning and Tunneling at the Metal−Semiconductor Interface of WSe_2 FETs. *Advanced Electronic Materials* **2023**, *9*, 2200955.
(17) Nakajima, R.; Nishimura, T.; Ueno, K.; Nagashio, K. Work Function Modulation of Bi/Au Bilayer System toward p-Type WSe_2 FET. *ACS Applied Electronic Materials* **2024**, *6*, 144−149.
(18) Pendurthi, R.; et al. Monolithic three-dimensional integration of complementary two-dimensional field-effect transistors. *Nat. Nanotechnol.* **2024**, *19*, 970−977.
(19) Telford, E. J.; Benyamini, A.; Rhodes, D.; Wang, D.; Jung, Y.; Zangiabadi, A.; Watanabe, K.; Taniguchi, T.; Jia, S.; Barmak, K.; Pasupathy, A. N.; Dean, C. R.; Hone, J. Via Method for Lithography Free Contact and Preservation of 2D Materials. *Nano Lett.* **2018**, *18*, 1416−1420.
(20) Jung, Y.; Choi, M. S.; Nipane, A.; Borah, A.; Kim, B.; Zangiabadi, A.; Taniguchi, T.; Watanabe, K.; Yoo, W. J.; Hone, J.; Teherani, J. T. Transferred via contacts as a platform for ideal two-dimensional transistors. *Nature Electronics* **2019**, *2*, 187−194.
(21) Satterthwaite, P. F.; et al. Van der Waals device integration beyond the limits of van der Waals forces using adhesive matrix transfer. *Nature Electronics* **2024**, *7*, 17−28.
(22) Yamamoto, M.; Dutta, S.; Aikawa, S.; Nakaharai, S.; Wakabayashi, K.; Fuhrer, M. S.; Ueno, K.; Tsukagoshi, K. Self-Limiting Layer-by-Layer Oxidation of Atomically Thin WSe_2. *Nano Lett.* **2015**, *15*, 2067−2073.
(23) Yamamoto, M.; Nakaharai, S.; Ueno, K.; Tsukagoshi, K. Self-Limiting Oxides on WSe_2 as Controlled Surface Acceptors and Low-Resistance Hole Contacts. *Nano Lett.* **2016**, *16*, 2720−2727.
(24) Wang, S.; Zhao, W.; Giustiniano, F.; Eda, G. Effect of oxygen and ozone on p-type doping of ultra-thin WSe_2 and $MoSe_2$ field effect transistors. *Phys. Chem. Chem. Phys.* **2016**, *18*, 4304−4309.
(25) Kang, W.-M.; Lee, S.; Cho, I.-T.; Park, T. H.; Shin, H.; Hwang, C. S.; Lee, C.; Park, B.-G.; Lee, J.-H. Multi-layer WSe_2 field effect transistor with improved carrier-injection contact by using oxygen plasma treatment. *Solid-State Electron.* **2018**, *140*, 2−7.
(26) Sivan, M.; Li, Y.; Veluri, H.; Zhao, Y.; Tang, B.; Wang, X.; Zamburg, E.; Leong, J. F.; Niu, J. X.; Chand, U.; Thean, A. V.-Y. All WSe_2 1T1R resistive RAM cell for future monolithic 3D embedded memory integration. *Nat. Commun.* **2019**, *10*, 5201.
(27) Borah, A.; Nipane, A.; Choi, M. S.; Hone, J.; Teherani, J. T. Low-Resistance p-Type Ohmic Contacts to Ultrathin WSe_2 by Using a Monolayer Dopant. *ACS Applied Electronic Materials* **2021**, *3*, 2941−2947.
(28) Kong, L.; Zhang, X.; Tao, Q.; Zhang, M.; Dang, W.; Li, Z.; Feng, L.; Liao, L.; Duan, X.; Liu, Y. Doping-free complementary WSe2 circuit via van der Waals metal integration. *Nat. Commun.* **2020**, *11*, 1866.
(29) Ngo, T. D.; Choi, M. S.; Lee, M.; Ali, F.; Yoo, W. J. Anomalously persistent p-type behavior of WSe_2 field-effect transistors by oxidized edge-induced Fermi-level pinning. *J. Mater. Chem. C* **2022**, *10*, 846−853.
(30) Moon, I.; Lee, S.; Lee, M.; Kim, C.; Seol, D.; Kim, Y.; Kim, K. H.; Yeom, G. Y.; Teherani, J. T.; Hone, J.; Yoo, W. J. The device level modulation of carrier transport in a 2D WSe_2 field effect transistor via a plasma treatment. *Nanoscale* **2019**, *11*, 17368−17375.
(31) Hsieh, Y.-C.; Lin, Z.-Y.; Fung, S.-J.; Lu, W.-S.; Ho, S.-C.; Hong, S.-P.; Ho, S.-Z.; Huang, C.-H.; Watanabe, K.; Taniguchi, T.; Chan, Y.-H.; Chen, Y.-C.; Wu, C.-L.; Chen, T.-M. Engineering the Strain and Interlayer Excitons of 2D Materials via Lithographically Engraved Hexagonal Boron Nitride. *Nano Lett.* **2023**, *23*, 7244−7251.
(32) Ho, S.-C.; Chang, C.-H.; Hsieh, Y.-C.; Lo, S.-T.; Huang, B.; Vu, T.-H.-Y.; Ortix, C.; Chen, T.-M. Hall effects in artificially corrugated bilayer graphene without breaking time-reversal symmetry. *Nature Electronics* **2021**, *4*, 116−125.
(33) Kato, R.; Uchiyama, H.; Nishimura, T.; Ueno, K.; Taniguchi, T.; Watanabe, K.; Chen, E.; Nagashio, K. p-Type Conversion of WS_2 and WSe_2 by Position-Selective Oxidation Doping and Its Application in Top Gate Transistors. *ACS Appl. Mater. Interfaces* **2023**, *15*, 26977−26984.
(34) Liu, X.; Pan, Y.; Yang, J.; Qu, D.; Li, H.; Yoo, W. J.; Sun, J. High performance WSe_2 p-MOSFET with intrinsic n-channel based on back-to-back p−n junctions. *Appl. Phys. Lett.* **2021**, *118*, 233101.
(35) Ngo, T. D.; Huynh, T.; Moon, I.; Taniguchi, T.; Watanabe, K.; Choi, M. S.; Yoo, W. J. Self-Aligned Top-Gate Structure in High-Performance 2D p-FETs via van der Waals Integration and Contact Spacer Doping. *Nano Lett.* **2023**, *23*, 11345−11352.
(36) Arnold, A. J.; Schulman, D. S.; Das, S. Thickness Trends of Electron and Hole Conduction and Contact Carrier Injection in Surface Charge Transfer Doped 2D Field Effect Transistors. *ACS Nano* **2020**, *14*, 13557−13568.
(37) Im, H. H.; Lee, D.; Lee, G.; Kim, H.-Y.; Kim, J. Self-Aligned Contact Doping of WSe_2 Metal−Insulator−Semiconductor Field-Effect Transistors Using Hydrogen Silsesquioxane. *ACS Applied Electronic Materials* **2023**, *5*, 2394−2400.
(38) Ren, Y.; Yang, X.; Zhou, L.; Mao, J.-Y.; Han, S.-T.; Zhou, Y. Recent Advances in Ambipolar Transistors for Functional Applications. *Adv. Funct. Mater.* **2019**, *29*, 1902105.
(39) Ho, P.-H.; Chang, J.-R.; Chen, C.-H.; Hou, C.-H.; Chiang, C.-H.; Shih, M.-C.; Hsu, H.-C.; Chang, W.-H.; Shyue, J.-J.; Chiu, Y.-P.; Chen, C.-W. Hysteresis-Free Contact Doping for High-Performance Two-Dimensional Electronics. *ACS Nano* **2023**, *17*, 2653−2660.
(40) Kwon, S.-J.; Han, T.-H.; Ko, T. Y.; Li, N.; Kim, Y.; Kim, D. J.; Bae, S.-H.; Yang, Y.; Hong, B. H.; Kim, K. S.; Ryu, S.; Lee, T.-W.

https://doi.org/10.1021/acsaelm.4c01574
ACS Appl. Electron. Mater. 2024, 6, 8319−8327

Extremely stable graphene electrodes doped with macromolecular acid. *Nat. Commun.* **2018**, *9*, 2037.
(41) Lee, D.; Choi, Y.; Kim, J.; Kim, J. Recessed-Channel WSe_2 Field-Effect Transistor via Self-Terminated Doping and Layer-by-Layer Etching. *ACS Nano* **2022**, *16*, 8484−8492.
(42) Wu, R.; et al. Bilayer tungsten diselenide transistors with on-state currents exceeding 1.5 milliamperes per micrometre. *Nature. Electronics* **2022**, *5*, 497−504.
(43) Xie, J.; et al. Low Resistance Contact to P-Type Monolayer WSe2. *Nano Lett.* **2024**, *24*, 5937−5943.
(44) Wang, Y.; Kim, J. C.; Li, Y.; Ma, K. Y.; Hong, S.; Kim, M.; Shin, H. S.; Jeong, H. Y.; Chhowalla, M. P-type electrical contacts for 2D transition-metal dichalcogenides. *Nature* **2022**, *610*, 61−66.
(45) Liu, Y.; Liu, S.; Wang, Z.; Li, B.; Watanabe, K.; Taniguchi, T.; Yoo, W. J.; Hone, J. Low-resistance metal contacts to encapsulated semiconductor monolayers with long transfer length. *Nature Electronics* **2022**, *5*, 579−585.
(46) Ngo, T. D.; Choi, M. S.; Lee, M.; Ali, F.; Hassan, Y.; Ali, N.; Liu, S.; Lee, C.; Hone, J.; Yoo, W. J. Selective Electron Beam Patterning of Oxygen-Doped WSe_2 for Seamless Lateral Junction Transistors. *Advanced Science* **2022**, *9*, 2202465.
(47) Alexander-Webber, J. A; Sagade, A. A; Aria, A. I; Van Veldhoven, Z. A; Braeuninger-Weimer, P.; Wang, R.; Cabrero-Vilatela, A.; Martin, M.-B.; Sui, J.; Connolly, M. R; Hofmann, S. Encapsulation of graphene transistors and vertical device integration by interface engineering with atomic layer deposited oxide. *2D Materials* **2017**, *4*, No. 011008.
(48) Mitta, S. B.; Choi, M. S.; Nipane, A.; Ali, F.; Kim, C.; Teherani, J. T.; Hone, J.; Yoo, W. J. Electrical characterization of 2D materials-based field-effect transistors. *2D Materials* **2021**, *8*, No. 012002.
(49) Pradhan, N. R.; Rhodes, D.; Memaran, S.; Poumirol, J. M.; Smirnov, D.; Talapatra, S.; Feng, S.; Perea-Lopez, N.; Elias, A. L.; Terrones, M.; Ajayan, P. M.; Balicas, L. Hall and field-effect mobilities in few layered p-WSe_2 field-effect transistors. *Sci. Rep.* **2015**, *5*, 8979.
(50) Yu, Z.; Ong, Z.-Y.; Li, S.; Xu, J.-B.; Zhang, G.; Zhang, Y.-W.; Shi, Y.; Wang, X. Analyzing the Carrier Mobility in Transition-Metal Dichalcogenide MoS_2 Field-Effect Transistors. *Adv. Funct. Mater.* **2017**, *27*, 1604093.
(51) Chan, M. Y.; Komatsu, K.; Li, S.-L.; Xu, Y.; Darmawan, P.; Kuramochi, H.; Nakaharai, S.; Aparecido-Ferreira, A.; Watanabe, K.; Taniguchi, T.; Tsukagoshi, K. Suppression of thermally activated carrier transport in atomically thin MoS_2 on crystalline hexagonal boron nitride substrates. *Nanoscale* **2013**, *5*, 9572−9576.
(52) Beebe, J. M.; Kim, B.; Gadzuk, J. W.; Daniel Frisbie, C.; Kushmerick, J. G. Transition from Direct Tunneling to Field Emission in Metal-Molecule-Metal Junctions. *Phys. Rev. Lett.* **2006**, *97*, No. 026801.
(53) Smith, L. W.; Batey, J. O.; Alexander-Webber, J. A.; Hsieh, Y.-C.; Fung, S.-J.; Albrow-Owen, T.; Beere, H. E.; Burton, O. J.; Hofmann, S.; Ritchie, D. A.; Kelly, M.; Chen, T.-M.; Joyce, H. J.; Smith, C. G. Giant Magnetoresistance in a Chemical Vapor Deposition Graphene Constriction. *ACS Nano* **2022**, *16*, 2833−2842.
(54) Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS_2 Transistors with Scandium Contacts. *Nano Lett.* **2013**, *13*, 100−105.
(55) Alharbi, A.; Shahrjerdi, D. Analyzing the Effect of High-k Dielectric-Mediated Doping on Contact Resistance in Top-Gated Monolayer MoS_2 Transistors. *IEEE Trans. Electron Devices* **2018**, *65*, 4084−4092.

https://doi.org/10.1021/acsaelm.4c01574
ACS Appl. Electron. Mater. 2024, 6, 8319−8327