

Novel Mixed-Dimensional hBN-Passivated Silicon Nanowire Reconfigurable Field Effect Transistors: Fabrication and Characterization

Sayantan Ghosh,* Muhammad Bilal Khan, Phanish Chava, Kenji Watanabe, Takashi Taniguchi, Slawomir Prucnal, René Hübner, Thomas Mikolajick, Artur Erbe, and Yordan M. Georgiev*



Cite This: *ACS Appl. Mater. Interfaces* 2023, 15, 40709–40718



Read Online

ACCESS |



Metrics & More

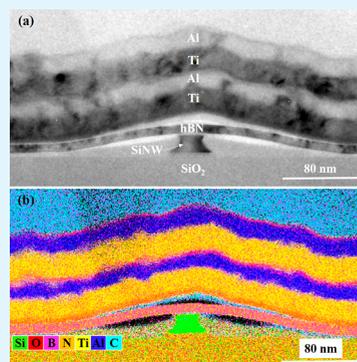


Article Recommendations



Supporting Information

ABSTRACT: This work demonstrates the novel concept of a mixed-dimensional reconfigurable field effect transistor (RFET) by combining a one-dimensional (1D) channel material such as a silicon (Si) nanowire with a two-dimensional (2D) material as a gate dielectric. An RFET is an innovative device that can be dynamically programmed to perform as either an n- or p-FET by applying appropriate gate potentials. In this work, an insulating 2D material, hexagonal boron nitride (hBN), is introduced as a gate dielectric and encapsulation layer around the nanowire in place of a thermally grown or atomic-layer-deposited oxide. hBN flake was mechanically exfoliated and transferred onto a silicon nanowire-based RFET device using the dry viscoelastic stamping transfer technique. The thickness of the hBN flakes was investigated by atomic force microscopy and transmission electron microscopy. The ambipolar transfer characteristics of the Si-hBN RFETs with different gating architectures showed a significant improvement in the device's electrical parameters due to the encapsulation and passivation of the nanowire with the hBN flake. Both n- and p-type characteristics measured through the top gate exhibited a reduction of hysteresis by 10–20 V and an increase in the on–off ratio (I_{ON}/I_{OFF}) by 1 order of magnitude (up to 10^8) compared to the values measured for unpassivated nanowire. Specifically, the hBN encapsulation provided improved electrostatic top gate coupling, which is reflected in the enhanced subthreshold swing values of the devices. For a single nanowire, an improvement up to 0.97 and 0.5 V/dec in the n- and p-conduction, respectively, is observed. Due to their dynamic switching and polarity control, RFETs boast great potential in reducing the device count, lowering power consumption, and playing a crucial role in advanced electronic circuitry. The concept of mixed-dimensional RFET could further strengthen its functionality, opening up new pathways for future electronics.



KEYWORDS: *mixed-dimensional reconfigurable FET, ambipolar, nickel silicide, flash lamp annealing, hBN encapsulation, subthreshold swing*

INTRODUCTION

The physical downscaling of silicon-based MOSFET technology has reached its limitations. Subsequently, the quest for alternative technological solutions based on new materials and device concepts augments the downscaling of integrated circuits. One such state-of-the-art advancement that has been intensively researched in the past decade to improve the functionality of nanowire field effect transistors (FETs) is called reconfigurability.¹ Reconfigurability is based on electrostatic control of the transistor's polarity. Transistors that are built on this concept are called reconfigurable FETs (RFETs).² A nanowire RFET is a Schottky junction-based device that can be reversibly configured to n- or p-polarity by controlling the electrostatic potential applied at the polarity gates. Due to this property, the functional complexity of a system can be enhanced by these transistors without increasing the device count. In the most generic process, the device is based on an intrinsic Si nanowire with nickel (Ni) contact pads placed on

both ends. Subsequent annealing results in the formation of silicide regions in the nanowire. Consequently, silicide-Si-silicide Schottky junctions are formed. By control of the Schottky barrier at the two ends of the nanowire with the help of gate potentials, the type and flow of charge carriers within the channel can be dynamically modulated. For ambipolarity, an electrostatic potential on the back gate or a single top gate enables the n- or p-transport, depending on the polarity of the gate voltage.

An ambipolar RFET device can be switched to its ON state by the application of both positive and negative voltages. This

Received: April 4, 2023

Accepted: August 8, 2023

Published: August 22, 2023



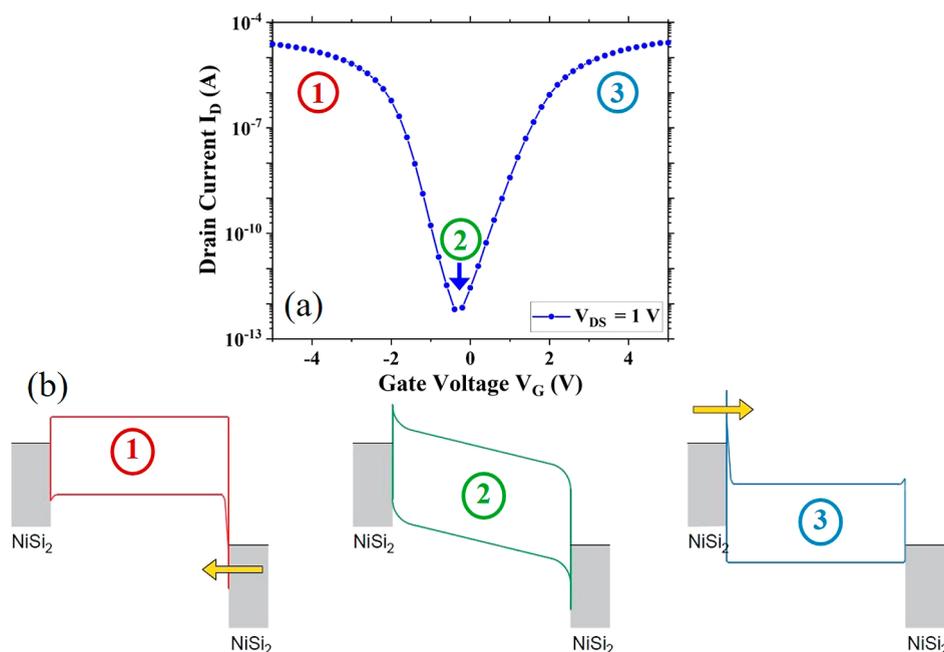


Figure 1. Ambipolar RFET characteristics (a) typical IV characteristics of a silicon nanowire RFET (b) energy band diagram of an ambipolar RFET under biased condition showing (1) hole conduction by tunneling with upward band bending, (2) off-state region dominated by high energy charge carrier conduction, and (3) electron conduction by tunneling with downward band bending.

nature of switching on the RFET device by sweeping the gate voltage from a high potential to a low potential is known as ambipolarity.³ In ambipolar devices, both types of charge carriers take part in the conduction in a single voltage sweep. The ambipolar RFET realized in this work is predominantly single-gated. This gate can be either a common back gate or a fabricated top gate. The gate electrode covers the Schottky junction region on either side of the nanowire channel. By applying a suitable voltage on the gate, the Schottky barrier is tuned accordingly to steer charge carriers into the channel for current conduction. In the OFF state of the device, the presence of both electron and hole barriers causes a limited off-current to flow, which is mainly due to high energy thermionic emission. When a positive bias voltage is applied to the gate structure, the energy of the bands is lowered, reducing the barrier height for the electrons. This leads to the injection of electrons into the channel by tunneling, contributing to an electron current or n-type conduction taking place. Simultaneously by sweeping the gate bias voltage to a low negative potential, the energy bands rise, reducing the barrier height for holes and promoting hole conduction. As the conduction band edge also rises at the same time, the electrons are blocked due to the high electron barrier height. Hence, the current is totally dominated by hole conduction only and is termed p-type conduction. The IV characteristics of an ambipolar RFET device and the band bending at different bias voltages are depicted in Figure 1.

As a single-gate architecture is used for ambipolar operation, the preferred gate structure is mostly the top gate. The top gate provides a better field effect capacitive coupling over the Schottky junctions and the nanowire channel than the back-gated architecture. This is due to the difference in thickness of the top gate dielectric and the buried oxide layer. The relation between the capacitance and the thickness of the dielectric is given by the following equation

$$C_{o_x} = \frac{\epsilon_o \kappa A}{t_{o_x}} \quad (1)$$

where C_{o_x} is the oxide capacitance which corresponds to capacitive coupling of the gate over the channel, ϵ_o represents the relative permittivity of free space, κ is the dielectric constant, A is the area, and t_{o_x} represents the thickness of the oxide or dielectric. Due to the lower thickness value of the top gate dielectric, a higher capacitive control of the channel is achieved, requiring a much smaller operational voltage for switching the device on. This also improves the subthreshold swing (SS) of the device.

Contrary to conventional transistors, charge carrier injection in the channel is selectively controlled at the Schottky junctions, thereby avoiding the need of having an inherently doped channel material. Tuning the Schottky barrier at both ends of the nanowire is one of the basic requirements for current transport in reconfigurable devices. This is achieved by electrostatic coupling and enhanced gate control over the channel material with a proper encapsulating and passivating dielectric material. Such transistors have been demonstrated using different channel materials such as carbon nanotubes,⁴ graphene,⁵ silicon (either as nanowires, utilizing FinFET or fully depleted silicon-on-insulator (FDSOI) transistors to achieve a high gate coupling),^{6–9} and 2D semiconductors.¹⁰ However, exploration of dielectric materials is relatively scarce.

The scientific exploration of 2D materials after the isolation of graphene in 2004¹¹ paved the way for a promising option in the field of nanoelectronics due to their stability at atomic thickness, high intrinsic mobility, optical transparency, and high strain limit compared to conventional semiconductors and insulators. One such material, which has excellent insulating properties with a large direct band gap of about 6 eV, is hexagonal boron nitride (hBN).^{12,13} 2D hBN has a structure analogous to graphene much like a honeycomb maze and is therefore known as “white graphene.” The hexagonal

sublattice of hBN consists of alternating boron and nitrogen atoms with the electron-deficient boron atoms laying directly above the electron-rich nitrogen atoms or vice versa in adjacent layers.¹⁴ The asymmetry in the sublattices causes polarized covalent bonds leading to the large band gap of hBN, making it act as an insulator. Interlayer van der Waals forces dictate the thickness of multilayer hBN, and the mechanically exfoliated monolayer is about 0.4 nm thick.¹⁴ Atomically thin hBN has flat interfaces due to the absence of surface dangling bonds and is, therefore, resistant to oxidation. It also acts as a good gate insulator with a dielectric constant ranging between 3 and 4 (similar or comparable to that of SiO₂)¹⁵ and can be even incorporated as an encapsulating layer for the active channel material of devices to prevent degradation of relatively unstable channel materials.¹⁶ hBN is chemically stable and can withstand 1000 °C at ambient conditions, 1400 °C in vacuum, and up to 2850 °C in an inert atmosphere.¹⁴ The thermal conductivity is about 484 W m⁻¹ K⁻¹ for 2D hBN with an elastic constant of 220–510 N m⁻¹ and a Young's modulus of about 1 TPa, thus making it an excellent material for flexible insulation.¹⁷

The top-down fabricated reconfigurable devices reported in this work are the first of their kind to incorporate silicon nanowires as the channel material along with 2D hBN as the gate dielectric and encapsulating layer. The focus of this work is on the development of the fabrication process, including structural studies of the device. Furthermore, the electrical transfer characteristics of such Si-hBN devices are measured based on different gating architectures to show a significant improvement in SS values, reduction of hysteresis, and increase in p and n currents due to the 2D encapsulation and passivation.

RESULTS AND DISCUSSION

The initial structural characterization of the mixed-dimensional RFET devices includes tapping-mode atomic force microscopy (AFM) analysis. Height profiles are extracted from multiple AFM scans to determine the thickness of the hBN flakes. Figure 2a shows an optical micrograph of two single nanowire-based devices.¹⁸ The first device is without an hBN dielectric layer, while the second device is capped with a thin hBN layer. AFM analysis is performed on these two devices, and the AFM topography is shown in Figure 2b. Three individual line profiles are drawn from the edges of the hBN flake to determine its thickness. The thickness of the hBN flake is approximately 10 nm, as can be seen from Figure 2c.

For further analysis of the hBN encapsulation of the nanowire, cross-sectional TEM analysis is performed. Figure 3 shows a representative bright-field TEM image. It is to be noted that the sectioning of the device is carried out across the single nanowire structure (i.e., perpendicular to the length of the nanowire). The cross-sectioning is performed to study and analyze the RFET device, especially the conformity of the hBN flake around the single nanowire. As seen from Figure 3a, the hierarchy of the RFET device starts with the buried SiO₂ layer at the bottom of the single nanowire channel. The nanowire channel has a trapezoidal shape with a height and a width of about 20 and 25 nm, respectively. The hBN thickness is confirmed to be approximately 10 nm and is shown to cover the nanowire channel from the top. On top of the dielectric layer, a stack of titanium (Ti) and aluminum (Al) acts as the gate electrode for the device.

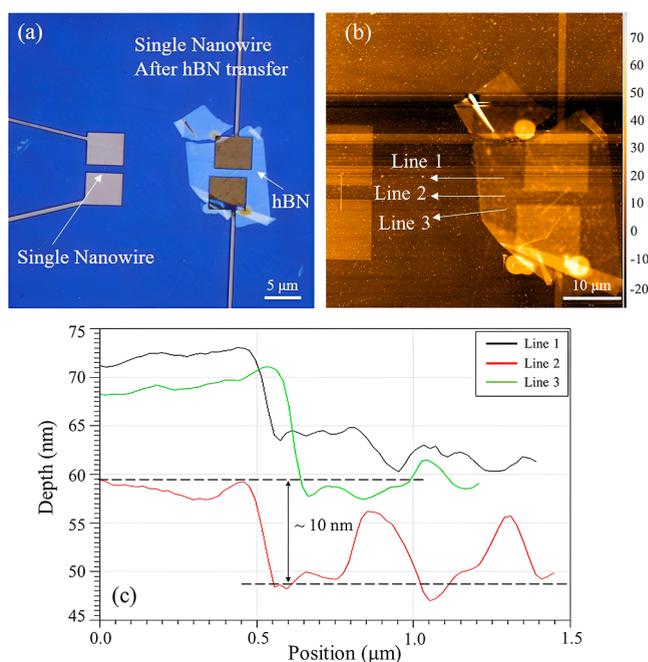


Figure 2. AFM characterization of the fabricated devices. (a) Visible light micrograph of two different single silicon nanowire devices with and without hBN dielectric layer. (b) AFM scan of the fabricated devices is shown in image (a). Lines 1, 2, and 3 are three different line profiles for determining the thickness of the hBN flake. (c) Thickness of hBN is based on the height profile lines 1, 2, and 3 in the image (b). Thickness of the hBN flake shown here is approximately 10 nm.

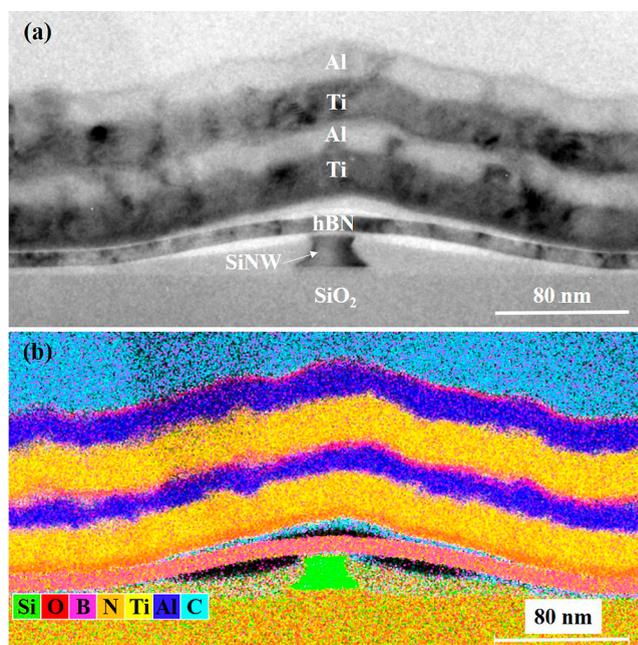


Figure 3. (a) Bright-field TEM micrograph of a sectioned nanowire device. The device structure consists of a buried SiO₂ layer underneath the silicon nanowire. On top of the nanowire channel is the hBN dielectric, which is shown to cover the nanowire. A stack of Ti and Al serves as the gate electrodes above the hBN. (b) Corresponding superimposed EDXS-based element distribution maps of the hBN-silicon-nanowire-based device.

The bright-field TEM image shows the stretch of the hBN flake and the position where it finally sits on the buried oxide

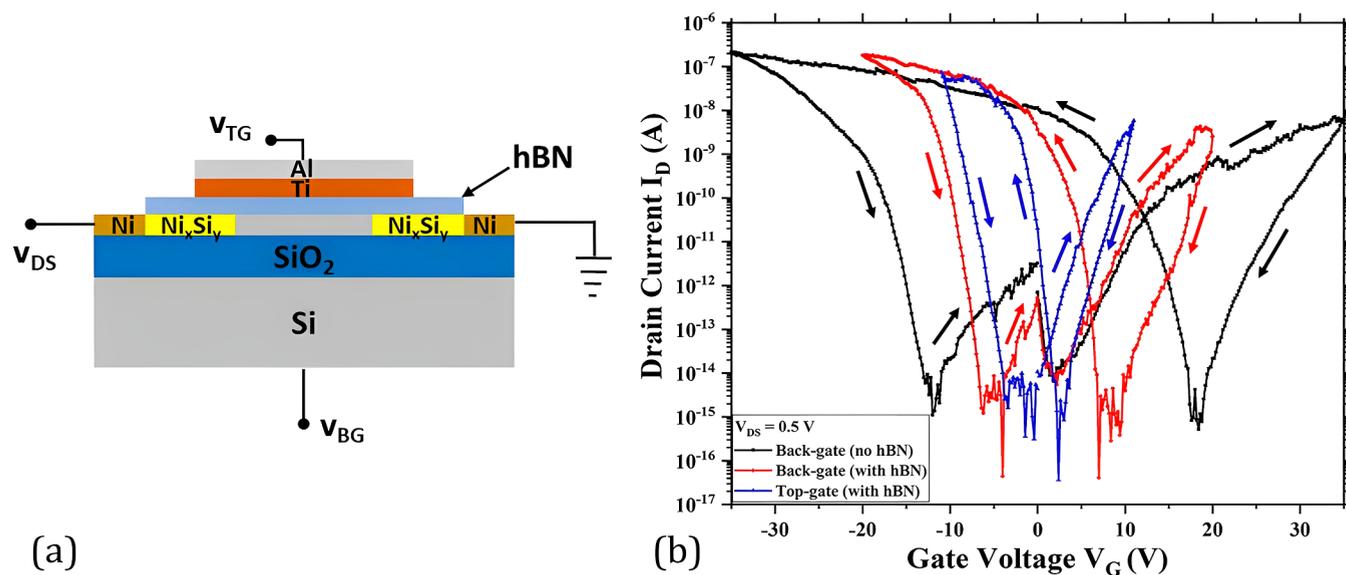


Figure 4. (a) Cross-sectional view of the device, including the voltage naming conventions used in this work. The device structure consists of a bottom Si layer on top of which is a 100 nm buried SiO₂ layer. The single nanowire is fabricated on top of the buried oxide layer. Ni contact pads are placed on both sides of the Si nanowire. Annealing creates Ni_xSi_y Schottky junctions in the nanowire. hBN is transferred on top of the device as the gate dielectric. A bilayer of Ti and Al serves as the top gate for the device. (b) Transfer characteristics of a single silicon nanowire-based device comprising an hBN flake as the dielectric layer. Different gating schemes are incorporated to deduce the IV characteristics. The length and width of the nanowire are 3 μm and 25 nm, respectively. The arrows in the transfer characteristics denote the direction of the curve based on the gate voltage sweep.

layer (away from the silicon nanowire channel). The structure of the top gate follows the curvature of the hBN flake. To study the element distribution in the sectioned device, a spectrum imaging analysis based on energy-dispersive X-ray spectroscopy (EDXS) is applied. The superposition of the corresponding element distribution maps of the device is shown in Figure 3b. The region enriched with boron (B) and nitrogen (N) confirms the presence of the hBN dielectric layer above the silicon nanowire channel. It is seen that the hBN flake sits on top of the silicon nanowire channel but does not conformally encapsulate its sidewalls. The EDXS-based analysis also confirms the presence of voids (denoted by the black areas in the element map). It is also to be noted that a dual layer of Ti and Al is evaporated on top of the hBN dielectric. The reason for using a dual-layer structure is that the first gate stack of Ti and Al was slightly misaligned with the silicon nanowire during the top gate fabrication. Hence, another broader layer of Ti and Al was precisely aligned and deposited above it for better capacitive coupling of the gate to the hBN stack. The growth of the oxide layer around the nanowire and in between the metal top gates (as seen in Figure 3b) is a likely phenomenon in ambient conditions. Such growth of oxide layers has also been outlined in previous studies regarding nanowire devices and silicidation.^{19,20} The presence of carbon (C) on top of the Ti and Al gate stack is due to the protective capping layer deposited during TEM specimen preparation. The formation of carbon with traces of silicon (Si) and oxygen (O) around the cross-section of the nanowire channel and above the hBN flake is mostly caused by the fabrication process of the device. Several scanning electron microscopy images were taken of the nanowire devices before and after hBN transfer in order to characterize the device. Thereby, organic substances on the surface of the sample were cracked and deposited as carbon layers.

Furthermore, the effect of hBN as a dielectric layer for silicon nanowire-based devices on their electrical properties is investigated. For this, the electrical measurements are carried out in an ambient atmosphere. The measurement schematic and transfer characteristics of a single nanowire-based device are presented in Figure 4. Three types of transfer characteristics are obtained by the following measurement schemes:

1. Back gating the device before hBN is transferred. The back gate voltage (V_{BG}) is swept between 35 and -35 V in a closed loop.
2. Back gating the device after the transfer of the hBN flake. V_{BG} is swept between 20 and -20 V in a closed loop.
3. Top gating the devices using hBN as the gate dielectric. The top gate voltage (V_{TG}) is swept between 10 and -10 V in a closed loop.

Lower gate voltages (V_G) are applied after hBN transfer to avoid the dielectric breakdown of the hBN. A drain to source voltage (V_{DS}) of 0.5 V is used to obtain the transfer characteristics. The device showed ambipolar behavior with improved electrostatic gate coupling after hBN transfer, which results in an enhanced SS value of the device (Table 1). The best values of SS are obtained by top gating the device. It is also evident from Figure 4b that the shift of the minima of the transfer curves is clearly reduced (toward the origin (0 V))

Table 1. SS Values of the hBN-Passivated Single Nanowire-Based Device Using Different Gating Schemes

carrier type	SS (V/dec)		
	back gate (without hBN)	back gate (with hBN)	top gate (with hBN)
n	1.82	1.68	0.97
p	1.07	0.78	0.50

after the transfer of the hBN flake. The characteristics also show an improvement in hysteresis after hBN transfer with the lowest hysteresis for the top-gated configuration. These are mainly due to the hBN passivation of the nanowire which reduces the interface charge states and charged hydroxyl sites.^{21,22} The hysteresis is calculated by taking the corresponding gate voltage value from the center of the subthreshold regime during successive forward and reverse voltage sweeps. This records the dynamics of charge trapping and detrapping in the nanowire channel and the interface. As seen from the graph in Figure 4b, the n- and p-conduction hysteresis reduces from 13 and 28 V, respectively, for back-gated unpassivated state to approximately 2.4 and 6.8 V for the hBN-encapsulated top-gated measurement. Simultaneously, the on-current (I_{ON}) and on-off ratio (I_{ON}/I_{OFF}) levels are enhanced after the passivation of the single nanowire by hBN and with the measurements recorded through the top gate. This is reflected by the modest increase in the n-type on-off ratio and 1 order of magnitude increase in the p-type ratio for the hBN-passivated top-gated measurements. The convention used for calculating I_{ON} and I_{OFF} is explained in detail in the Supporting Information (see Figure S1). The extracted electrical parameters of the hBN-passivated single nanowire-based device with different gating schemes are listed in Table 2.

Table 2. Extracted Parameters from the Transfer Characteristics of the hBN-Passivated Single Nanowire-Based Device at a V_{DS} of 0.5 V Using Different Gating Schemes

parameter	carrier type	back gate (without hBN)	back gate (with hBN)	top gate (with hBN)
I_{ON} (A)	n	5.8×10^{-9}	2.4×10^{-9}	5.7×10^{-9}
	p	8.4×10^{-9}	1.8×10^{-8}	2.6×10^{-8}
I_{OFF} (A)	n	7.8×10^{-16}	7.6×10^{-16}	8.4×10^{-16}
	p	8.2×10^{-16}	1.2×10^{-15}	8.4×10^{-16}
I_{ON}/I_{OFF} ratio	n	$\sim 10^7$	$\sim 10^7$	$\sim 10^7$
	p	$\sim 10^7$	$\sim 10^7$	$\sim 10^8$
hysteresis (V)	n	13	6.2	2.4
	p	28	13.5	6.8

The output characteristics for the single nanowire-based device are shown in Figure S2. The corresponding off-state output characteristics are evaluated by a two-probe measurement for a V_{DS} sweep of 0 to 0.5 V keeping the V_G constant at 0 V (see Figure S2a). Three separate measurements are carried out at different times. The first measurement is before hBN is transferred on the nanowire, the second is after hBN is transferred, and the final measurement is after the top gate is fabricated. For the first two measurements (at such negligible V_G), a near linear regime is exhibited with a considerable increase in the drain current (I_D) after the passivation of the nanowire with hBN. For the final measurement after the top gate is fabricated, it is seen that the I_D has a significant increase in current with a characteristic showing Schottky type supra linear shape. Since the top gates help in better hBN encapsulation of the single nanowire, better dielectric passivation is expected. This might have led to superior charge carrier transport through the nanowire channel without the influence of the gate voltages. Simultaneously, the on-state output characteristics of the hBN ambipolar device are also

measured based on the top-gated transfer characteristics. For the n-type characteristics, V_{DS} is varied from 0.25 to 1 V while increasing the V_{TG} from 0 to 10 V in steps of 1 V (Figure S2b). For the p-type behavior, similar voltage steps are maintained but in a negative direction (see Figure S2c). A clear Schottky behavior is seen in both types of conduction for high values of V_{DS} , which provide a fair conclusion to the contact properties based on the ambipolar shape of the transfer characteristics. For the hole conduction, saturation is seen for low V_{TG} values. It is also to be noted that in both cases, I_D increases with an increase in V_{TG} . This implies that high V_{TG} enables more band bending at the Schottky junctions, leading to increased tunneling of carriers. This eventually leads to a higher current flow.

Additionally, to realize the role of the device performance based on the hBN thickness, two hBN-passivated single nanowire-based devices are compared. These two devices exhibit contrasting hBN thicknesses, with one measuring 10 nm and the other measuring 20 nm. The top-gated transfer characteristics of these two devices are obtained and are shown in the Supporting Information Figure S3. For both devices, the V_{TG} is swept in a butterfly loop while varying the V_{DS} from 0.25 to 1 V in steps of 0.25 V. It is clearly prominent from both the graphs that the devices exhibit ambipolar behavior with a distinctive rise in the I_{ON} levels for both the branches with the increase in V_{DS} . However, compared to the device with 20 nm hBN as a dielectric, the one with 10 nm shows higher on-currents, lower hysteresis, and better SS. The on-off ratio (I_{ON}/I_{OFF}) levels for the 10 nm hBN device are visible for more than one decade compared to the 20 nm hBN device. This is understandable since thinner hBN would provide better passivation and encapsulation to the single nanowire. This will, in turn, lead to the device exhibiting better electrical conduction due to reduced charge scattering. Furthermore, considering the measurements are conducted by top gating through the hBN dielectric, it is expected of the device with the thinner hBN to have a better capacitive coupling. This, in turn, improves the SS of the 10 nm hBN device compared to the 20 nm one. Finally, it is also observed that the hysteresis of the n- and p-branch is much lower for the thinner hBN device hinting at the absence of interface trap states and oxide charges due to the better passivation of the nanowire. In these scenarios, it is clearly understood that the tunability and reconfigurability of the devices are unaltered for either thickness of the hBN. However, the variability in thickness does play a vital role in enhancing the device's electrical performance. These results serve as a proof of concept that hBN can be employed as a gate dielectric for one-dimensional silicon nanowire-based devices, presented for the first time to the best of our knowledge. The electrostatic coupling can be further enhanced by improving the interface between hBN and the silicon nanowire. The quality, thickness, and uniformity of the hBN can also impact the device's performance. To achieve this, a well-controlled deposition of hBN using chemical vapor deposition (CVD) or epitaxy can be employed.²³ Furthermore, nanowires having smooth edges instead of sharp cuts can enable better contact between nanowire surfaces and hBN. Moreover, the properties of hBN can also be tuned, e.g., by doping or defect-induced variations.²⁴ This attribute can be exploited to flexibly fabricate devices to attain the desired performance.

To further understand the contact between the nanowires and hBN, the dielectric is also transferred on a nanowire array-based device. The array has 20 nanowires with a pitch of 200

nm. The transfer characteristics are listed in Figure 5. The three gating schemes are used similarly to the single nanowire-

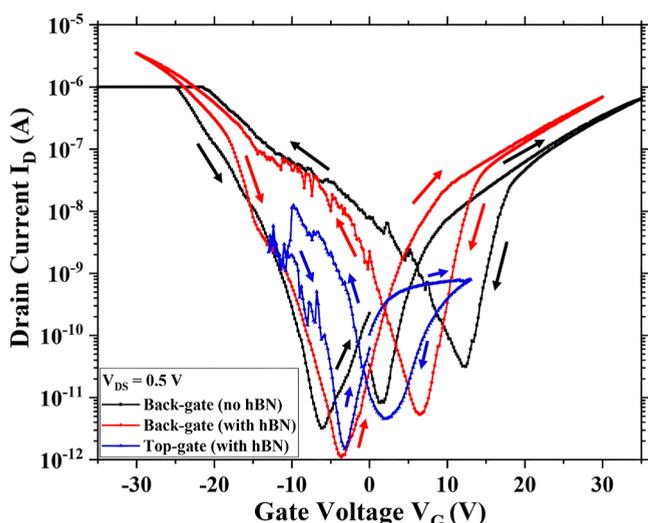


Figure 5. Transfer characteristics of a device consisting of a nanowire array. hBN is used as a dielectric layer. The lengths and widths of the nanowires are 3 μm and 25 nm, respectively. The pitch between the nanowires is 200 nm. The black curve shows a straight line below -20 V due to the compliance set in the measurement tool. For the rest of the transfer characteristics, the compliance was set at a higher drain current value. Similar to Figure 4b, the arrows in the transfer characteristics denote the direction of the curve based on the gate voltage sweep.

based device. With back gating, the device with the hBN flake showed an improvement in on- and off-currents and, hence, in the on-off ratio by nearly 2 orders of magnitude (Table 4).

Table 3. SS Values of hBN-Passivated Nanowire Array-Based Devices Using Different Gating Schemes

carrier type	SS (V/dec)		
	back-gate (without hBN)	back-gate (with hBN)	top-gate (with hBN)
n	2.56	1.76	3.05
p	5	3.06	1.5

Table 4. Extracted Parameters from the Transfer Characteristics of the hBN-Passivated Nanowire Array-Based Device at a V_{DS} of 0.5 V Using Different Gating Schemes

parameter	carrier type	back gate (without hBN)	back gate (with hBN)	top gate (with hBN)
I_{ON} (A)	n	6.4×10^{-7}	6.8×10^{-7}	8.0×10^{-10}
	p	7.3×10^{-8}	2.7×10^{-7}	8.2×10^{-9}
I_{OFF} (A)	n	3.2×10^{-11}	5.3×10^{-12}	4.5×10^{-12}
	p	3.2×10^{-11}	5.3×10^{-12}	4.5×10^{-12}
$I_{\text{ON}}/I_{\text{OFF}}$ ratio	n	$\sim 10^4$	$\sim 10^5$	$\sim 10^2$
	p	$\sim 10^3$	$\sim 10^5$	$\sim 10^3$
hysteresis (V)	n	8	7.6	6.9
	p	16	11	4.2

This means that passivation by hBN of the 20 nanowires helps to improve these parameters. Similarly from Figure 5, it is seen

that the shift of the transfer curve minima is largely reduced. Subsequently, the hysteresis of the device reduces from its unpassivated state to hBN-passivated top gate state (see Table 4) exactly analogous to how it was observed for the single nanowire-based device. However, it is also to be noted that compared to the single nanowire-based device, the nanowire array-based device has higher off-currents (almost 4 orders of magnitude). The reason for this can be that the minimum current I_{OFF} is dependent on the V_{DS} value, with V_{G} being negligible. Therefore at room temperature, with a considerable V_{DS} and negligible V_{G} , an adequate amount of thermally activated charge carriers can pass through the drain-source contacts. Nonetheless, for a single nanowire, this current value is low. However, it is understandable that the array-based device consists of 20 single nanowires in parallel. Each of these nanowires contributes charge carriers thermionically in the off-state, thus increasing the off-current. Furthermore, the device maintained the off-current when the transfer characteristics were obtained with top gating, but the on-current was reduced. This is attributed to the weak interface between nanowire arrays and hBN (Supporting Information Figure S4). Since nanowires have a pitch of 200 nm, hBN is seen to cover only the top part of the nanowires and not the sidewalls. With an increasing pitch of the nanowires, the hBN coverage of the nanowires can be expected to improve and vice versa. It is expected that for nanowire arrays with a larger distance between the nanowires, a thinner hBN would bend in the gap. This would provide passivation and encapsulation from all three sides of the nanowire. However, with a low pitch of 200 nm, the hBN only sits on the top of the nanowire and does not encapsulate it like in the case of the single nanowire-based device. Thus, although back-gated characteristics improved due to the added effect of the multiple nanowires, the top gate result degraded due to weak electrostatic coupling. This is reflected in the SS values of these measurements (Table 3). The SS values improved after hBN transfer with back gate measurements. Although both these measurements provide capacitive gate coupling through the same back gate, the measurement after hBN transfer has a better SS value due to the surface passivation of the nanowires by hBN. With hBN reducing the interface state density of the top surface of the nanowire, the SS value is strongly influenced.²⁵ However, the SS of the n-branch degraded with the top gate measurements compared to its back gate due to lower gate coupling through the hBN on the multiple nanowires.

Furthermore, a gate leakage current analysis is performed during each measurement step to prevent the flow of high current through the dielectric layer during continuous voltage scans. The repeated flow of high currents can eventually lead to dielectric breakdown and degradation of the hBN-passivated nanowire-based devices. The measured leakage current analysis for hBN-passivated single nanowire- and nanowire array-based devices with different gating schemes are shown in Supporting Information Figure S5. For both the single nanowire- and nanowire array-based devices, the leakage current is measured by sweeping the gate voltage from a low potential to a high potential. Repeated voltage scans that produce currents above 10 pA can be fatal for the dielectric and the device. Therefore, compliance of 10 pA was set in the measurement setup prior to the analysis. As seen from Figure S5, the gate leakage current I_{G} (denoted by the red curve) is always under the set limit of 10 pA and showed minimal leakage through the gate dielectric. In the scope of this work, a total of 18 nanowire devices are

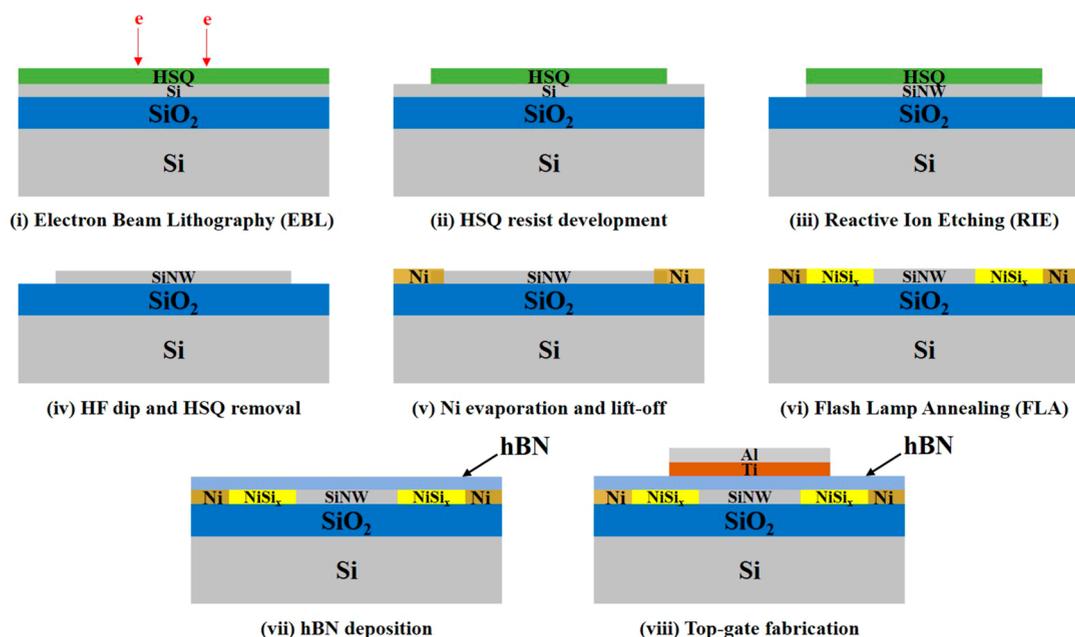


Figure 6. A schematic representation of the top-down fabrication process flow of the novel mixed-dimensional RFET device. (i) Starting with SOI substrate, a negative resist HSQ is spin-coated for patterning with EBL, (ii) development of HSQ resist creates the HSQ patterns in the shape of the nanowire, (iii) HSQ patterns are then transferred to the top 20 nm device layer using anisotropic reactive ion etching, (iv) HF dip is carried out to remove the top HSQ later, (v) source and drain Ni contact pads are fabricated by EBL, metal deposition, and lift-off technique, (vi) FLA creates the NiSi₂ Schottky junction inside the nanowire, (vii) exfoliated hBN is transferred onto the device by dry-stamping technique, and (viii) top gates are fabricated on top of the hBN layer by EBL, metal deposition, and lift-off.

fabricated. Out of 12 are single nanowires and 6 are nanowire array devices. Exfoliated hBN is successfully transferred to 12 of the devices, while the top gate is fabricated on 5 of them. Out of the five top-gated single nanowire-based devices, three are nominally identical with hBN thickness varying between 10 and 15 nm. The other two devices had significantly thicker hBN gate dielectric, which led to weaker gate coupling and considerably worse device characteristics (as explained in the earlier section). On the other hand, the three devices with thinner hBN consistently exhibited similar device performances. The electrical parameters of these nominally identical three devices are extracted to derive the statistical analysis including the mean values and standard deviations (SD). This is shown in Supporting Information Table S1. Figure S6 presents the extracted electrical parameters of the three devices along with their resulting mean and SD values. The SD values in Figure S6a–c are relatively higher than their mean values. This is because the currents extracted have deviations of a couple of orders of magnitude owing to the device-to-device variability. Since the nanowires are fabricated by a top-down approach, these devices are robust and stable. hBN also helps to protect the devices from the outside environment. Therefore, over an extended period of time, the devices maintained consistent functionality and performance. The fabrication of these 12 nanowire devices with hBN is also carried out over different time spans. Their similar device behavior implied the reproducibility of the devices and the reliability of the fabrication process that is employed.

EXPERIMENTAL SECTION

The substrate material used for the fabrication of a mixed-dimensional RFET is a $1 \times 1 \text{ cm}^2$ silicon-on-insulator (SOI) substrate. It consists of layers of silicon-insulator-silicon stacked on top of each other. The device or active top layer of the substrate consists of 20 nm intrinsic

silicon, followed by a 102 nm thick buried oxide (BOx) layer and a $775 \mu\text{m}$ p-doped Si carrier wafer. In this work, the fabrication of nanowires is based on the top-down approach, which allows the large-scale integration of devices. The top-down approach involves the use of a substrate material, which is subjected to successive subtractive procedures to ultimately achieve a nanostructure. The detailed process of silicon nanowire fabrication is described in our previous work¹⁸ and schematically shown in Figure 6. At first, the SOI substrate is cleaned thoroughly in various chemicals, including Piranha solution, acetone, isopropanol (IPA), and deionized (DI) water. Then, a 2% hydrogen silsesquioxane (HSQ) (XR-1541 from DuPont) negative-tone resist is spin-coated on the substrate at 2000 rpm for 30 s, creating a 40 nm thick HSQ layer. The nanowires are exposed using a RAITH e-LINE PLUS electron beam lithography (EBL) system at an acceleration voltage of 10 kV, a base dose of $1000 \mu\text{C cm}^{-2}$, an aperture with the size of $30 \mu\text{m}$, and a beam area step size of 2 nm. The exposure parameters are optimized according to the nanowire dimensions and were used throughout this work for patterning the appropriate nanostructures. After the exposure, the substrate is subjected to a resist development, which removes the unexposed resist.²⁶ A SENTECH inductively coupled plasma reactive ion etching (ICP-RIE) Si 500 system is used to anisotropically transfer the HSQ pattern to the active device layer. The fabrication of source and drain Ni contacts at both ends of the nanowire includes a similar process of EBL patterning, metal deposition using a UHV e-beam evaporation system from BESTEC, and a lift-off process. Flash lamp annealing (FLA) is performed on the substrate after the Ni contact deposition to achieve diffusion of Ni into the nanowire to form the NiSi₂ phase.¹⁸ Ni silicidation in the nanowire creates a heterostructure of NiSi₂–Si–NiSi₂ forming two Schottky junctions on either side. A prior study was conducted to develop a Ni silicidation process of silicon nanowires by rapid thermal annealing (RTA).²⁷ This study was further continued to compare the results with FLA.¹⁸ The optimization of the FLA parameters with different energy densities, flash pulse durations, and various inert gas conditions was performed to achieve homogeneous Ni silicide formation in the nanowire. The optimum FLA treatment is obtained for the energy density of about 89 J cm^{-2} for 6 ms in continuous nitrogen flow.

The hBN flakes are prepared using the mechanical exfoliation technique²⁸ on a polydimethylsiloxane (PDMS) substrate (approximately $1 \times 1 \text{ cm}^2$) employing commercial scotch tape. Suitable hBN flakes are then identified with the help of an optical microscope based on their thickness, lateral dimensions, and uniformity. The hBN flakes are transferred onto the nanowire using the dry-stamping technique²⁹ by aligning the desired flake onto the nanowire with the help of a micromanipulator setup that is coupled to an optical microscope. The schematic of the hBN transfer process and optical micrographs of the mixed-dimensional RFET devices are shown in Figure 7. With

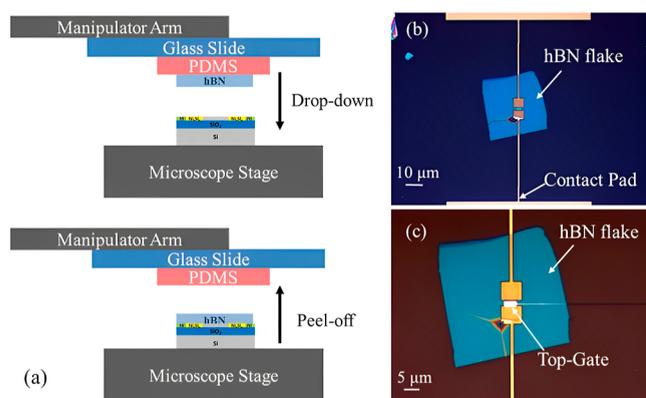


Figure 7. (a) Transfer of hBN flake indicating the steps of drop-down and peel-off process onto the silicon nanowire-based devices using the dry viscoelastic stamping transfer technique. (b) Visible-light micrograph image of a transferred hBN flake on a single silicon nanowire-based device showing the architecture of contact pads and connection lines. (c) Visible-light micrograph image of a mixed-dimensional RFET device with a top-gate present on the hBN layer.

favorable hBN flakes on the silicon nanowires, single top gates are placed based on EBL patterning, metal deposition, and lift-off processes. A stack of titanium (Ti) and aluminum (Al) is typically used as the top gate.

Bright-field transmission electron microscopy (TEM) images are recorded using an image- C_s -corrected TITAN 80-300 microscope (FEI) operated at an accelerating voltage of 300 kV. With a TALOS F200X microscope equipped with an X-FEG electron source and a Super-X EDX detector system (FEI), high-angle annular dark-field scanning TEM (HAADF-STEM) imaging and spectrum imaging analysis based on energy-dispersive X-ray spectroscopy (EDXS) are performed at 200 kV. Before (S)TEM analysis, the specimen mounted in a high-visibility low-background holder is placed for 8 s into a FISCHIONE 1020 plasma cleaner to eliminate any potential contamination. Cross-sectional TEM specimens of the mixed-dimensional RFET devices are prepared by in situ lift-out using a Helios 5 CX-focused ion beam (FIB) device (Thermo Fisher). To protect the sample surface, a carbon cap layer is deposited beginning with electron-beam-assisted and subsequently followed by Ga-FIB-assisted precursor decomposition. Afterward, the TEM lamella is prepared using a 30 keV Ga-FIB with adapted currents. Its transfer to a 3-post copper lift-out grid (Omniprobe) is done with an EasyLift EX nanomanipulator (Thermo Fisher). To minimize sidewall damage, Ga ions with only 5 keV energy are used for the final thinning of the TEM lamella to electron transparency. Tapping mode AFM analysis is carried out using a NANOFRAZOR SCHOLAR tool from HEIDELBERG INSTRUMENTS. For the electrical transfer characteristics measurements, a semiautomated SÜSS MICROTTECH probe system PA200 connected with a 4200-SCS KEITHLEY INSTRUMENTS characterization system is used.

SUMMARY

A novel hybrid mixed-dimensional RFET concept is demonstrated by introducing 2D hBN in nanowire-based

electronics. The fabricated devices exhibit an improvement in SS values, a reduction in hysteresis, and an enhancement of the p and n on-currents. To conclude, hBN can be used as an effective dielectric and passivating layer for one-dimensional nanowire devices. Since the properties of the hBN can be tuned, versatile devices can be fabricated using this robust material. However, optimization of the device design and control over the hBN thickness is required for superior device performance. This first demonstration of hBN incorporation in nanowire-based devices potentially opens up a new paradigm in semiconductor electronics. Furthermore, system-level integration of these devices can be achieved using CVD or epitaxy-based deposition of hBN.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsami.3c04808>.

Information on the convention for calculation of on- and off-currents, on-state and off-state output characteristics, transfer characteristics based on different hBN thicknesses RFET devices, additional TEM and EDXS image of hBN-passivated silicon nanowire array-based device, and leakage current analysis (PDF)

AUTHOR INFORMATION

Corresponding Authors

Sayantana Ghosh – Institute of Ion Beam Physics and Materials Research, Helmholtz-Zentrum Dresden-Rossendorf (HZDR), Dresden 01328, Germany; Technische Universität Dresden, Dresden 01069, Germany; orcid.org/0000-0003-1347-1365; Email: s.ghosh@hzdr.de

Yordan M. Georgiev – Institute of Ion Beam Physics and Materials Research, Helmholtz-Zentrum Dresden-Rossendorf (HZDR), Dresden 01328, Germany; Institute of Electronics at the Bulgarian Academy of Sciences, Sofia 1784, Bulgaria; Email: y.georgiev@hzdr.de

Authors

Muhammad Bilal Khan – Institute of Ion Beam Physics and Materials Research, Helmholtz-Zentrum Dresden-Rossendorf (HZDR), Dresden 01328, Germany; orcid.org/0000-0003-4627-9433

Phanish Chava – Institute of Ion Beam Physics and Materials Research, Helmholtz-Zentrum Dresden-Rossendorf (HZDR), Dresden 01328, Germany; Technische Universität Dresden, Dresden 01069, Germany

Kenji Watanabe – National Institute for Materials Science, Tsukuba 305-0044, Japan; orcid.org/0000-0003-3701-8119

Takashi Taniguchi – National Institute for Materials Science, Tsukuba 305-0044, Japan; orcid.org/0000-0002-1467-3105

Slawomir Prucnal – Institute of Ion Beam Physics and Materials Research, Helmholtz-Zentrum Dresden-Rossendorf (HZDR), Dresden 01328, Germany; orcid.org/0000-0002-4088-6032

René Hübner – Institute of Ion Beam Physics and Materials Research, Helmholtz-Zentrum Dresden-Rossendorf (HZDR), Dresden 01328, Germany; orcid.org/0000-0002-5200-6928

Thomas Mikolajick – Namlab gGmbH, Dresden 01187, Germany; Technische Universität Dresden, Dresden 01069, Germany; Technische Universität Dresden, Center for Advancing Electronics Dresden (CfAED), Dresden 01069, Germany; orcid.org/0000-0003-3814-0378

Artur Erbe – Institute of Ion Beam Physics and Materials Research, Helmholtz-Zentrum Dresden-Rossendorf (HZDR), Dresden 01328, Germany; Technische Universität Dresden, Dresden 01069, Germany; Technische Universität Dresden, Center for Advancing Electronics Dresden (CfAED), Dresden 01069, Germany; orcid.org/0000-0001-6368-8728

Complete contact information is available at:
<https://pubs.acs.org/10.1021/acsami.3c04808>

Author Contributions

S.G., M.B.K., and P.C. contributed equally to this work. K.W. and T.T. provided the hBN crystals. S.P. and R.H. helped in FLA and structural characterization of the samples, respectively. T.M., A.E., and Y.M.G. supervised the work and reviewed the manuscript.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

We are thankful to T. Schönherr and C. Neisser for their help in the device fabrication and to A. Kunz for TEM specimen preparation. This work has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement no 899282 (RADICAL). We are also grateful to the HZDR Ion Beam Center TEM facilities and the funding of TEM Talos by the German Federal Ministry of Education and Research (BMBF; grant no. 03SF0451) in the framework of HEMCP.

REFERENCES

- (1) Simon, M.; Heinzig, A.; Trommer, J.; Baldauf, T.; Mikolajick, T.; Weber, W. M. Top-down Technology for Reconfigurable Nanowire FETs with Symmetric On-Currents. *IEEE Trans. Nanotechnol.* **2017**, *16*, 812–819.
- (2) Heinzig, A.; Slesazek, S.; Kreupl, F.; Mikolajick, T.; Weber, W. M. Reconfigurable Silicon Nanowire Transistors. *Nano Lett.* **2012**, *12*, 119–124.
- (3) Mikolajick, T.; Galderisi, G.; Rai, S.; Simon, M.; Böckle, R.; Sistani, M.; Cakirlar, C.; Bhattacharjee, N.; Mauersberger, T.; Heinzig, A.; et al. Reconfigurable Field Effect Transistors: A technology Enablers Perspective. *Solid-State Electron.* **2022**, *194*, 108381.
- (4) Lin, Y.-M.; Appenzeller, J.; Knoch, J.; Avouris, P. High-Performance Carbon Nanotube Field-Effect Transistor with Tunable Polarities. *IEEE Trans. Nanotechnol.* **2005**, *4*, 481–489.
- (5) Lin, Y.-M.; Chiu, H.-Y.; Jenkins, K. A.; Farmer, D. B.; Avouris, P.; Valdes-Garcia, A. Dual-Gate Graphene FETs with $f_{-}\{T\}$ of 50 GHz. *IEEE Electron Device Lett.* **2010**, *31*, 68–70.
- (6) Colli, A.; Tahraoui, A.; Fasoli, A.; Kivioja, J. M.; Milne, W. I.; Ferrari, A. C. Top-Gated Silicon Nanowire Transistors in a Single Fabrication Step. *ACS Nano* **2009**, *3*, 1587–1593.
- (7) Heinzig, A.; Mikolajick, T.; Trommer, J.; Grimm, D.; Weber, W. M. Dually Active Silicon Nanowire Transistors and Circuits with Equal Electron and Hole Transport. *Nano Lett.* **2013**, *13*, 4176–4181.
- (8) Khan, M.; Ghosh, S.; Prucnal, S.; Mauersberger, T.; Hübner, R.; Simon, M.; Mikolajick, T.; Erbe, A.; Georgiev, Y. Towards Scalable Reconfigurable Field Effect Transistor using Flash Lamp Annealing. *Device Research Conference (DRC)*, 2020; pp 1–2.
- (9) Sessi, V.; Simon, M.; Slesazek, S.; Drescher, M.; Mulaosmanovic, H.; Li, K.; Binder, R.; Waidmann, S.; Zeun, A.; Pawlik, A.-S.; et al. S2-2 Back-Bias Reconfigurable Field Effect Transistor: A Flexible Add-On Functionality for 22 nm FDSOI. *2021 Silicon Nanoelectronics Workshop (SNW)*, 2021; pp 1–2.
- (10) Fei, W.; Trommer, J.; Lemme, M. C.; Mikolajick, T.; Heinzig, A. Emerging Reconfigurable Electronic Devices based on Two-dimensional Materials: A review. *InfoMat* **2022**, *4*, No. e12355.
- (11) Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.-e.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon Films. *science* **2004**, *306*, 666–669.
- (12) Watanabe, K.; Taniguchi, T.; Kanda, H. Direct-Bandgap Properties and Evidence for Ultraviolet Lasing of Hexagonal Boron Nitride Single Crystal. *Nat. Mater.* **2004**, *3*, 404–409.
- (13) Miró, P.; Audiffred, M.; Heine, T. An Atlas of Two-Dimensional Materials. *Chem. Soc. Rev.* **2014**, *43*, 6537–6554.
- (14) Bhimanapati, G.; Glavin, N.; Robinson, J. A. *Semiconductors and Semimetals*; Elsevier, 2016; Vol. 95, pp 101–147.
- (15) Lee, G.-H.; Cui, X.; Kim, Y. D.; Arefe, G.; Zhang, X.; Lee, C.-H.; Ye, F.; Watanabe, K.; Taniguchi, T.; Kim, P.; et al. Highly Stable, Dual-gated MoS₂ Transistors Encapsulated by Hexagonal Boron Nitride with Gate-controllable Contact, Resistance, and Threshold Voltage. *ACS Nano* **2015**, *9*, 7019–7026.
- (16) Arora, H.; Jung, Y.; Venanzi, T.; Watanabe, K.; Taniguchi, T.; Hübner, R.; Schneider, H.; Helm, M.; Hone, J. C.; Erbe, A. Effective Hexagonal Boron Nitride Passivation of Few-layered InSe and GaSe to Enhance their Electronic and Optical Properties. *ACS Appl. Mater. Interfaces* **2019**, *11*, 43480–43487.
- (17) Kumar, R.; Rajasekaran, G.; Parashar, A. Optimised Cut-off Function for Tersoff-like Potentials for a BN Nanosheet: a Molecular Dynamics Study. *Nanotechnology* **2016**, *27*, 085706.
- (18) Khan, M. B.; Prucnal, S.; Ghosh, S.; Deb, D.; Hübner, R.; Pohl, D.; Rebohle, L.; Mikolajick, T.; Erbe, A.; Georgiev, Y. M. Controlled Silicidation of Silicon Nanowires using Flash Lamp Annealing. *Langmuir* **2021**, *37*, 14284–14291.
- (19) Weber, W. M. Silicon to Nickel Silicide Longitudinal Nanowire Heterostructures: Synthesis, Electrical Characterization and Novel Devices. Ph.D. Thesis, Technische Universität München, 2008.
- (20) Bartur, M.; Nicolet, M.-A. Thermal Oxidation of Nickel Disilicide. *Appl. Phys. Lett.* **1982**, *40*, 175–177.
- (21) Paska, Y.; Haick, H. Interactive Effect of Hysteresis and Surface Chemistry on Gated Silicon Nanowire Gas Sensors. *ACS Appl. Mater. Interfaces* **2012**, *4*, 2604–2617.
- (22) Fahem, Z.; Csaba, G.; Erlen, C.; Lugli, P.; Weber, W.; Geelhaar, L.; Riechert, H. Analysis of the Hysteretic Behavior of Silicon Nanowire Transistors. *Phys. Status Solidi C* **2008**, *5*, 27–30.
- (23) Uchida, Y.; Kawahara, K.; Fukamachi, S.; Ago, H. Chemical Vapor Deposition Growth of Uniform Multilayer Hexagonal Boron Nitride driven by Structural Transformation of a Metal Thin Film. *ACS Appl. Electron. Mater.* **2020**, *2*, 3270–3278.
- (24) Zhang, K.; Feng, Y.; Wang, F.; Yang, Z.; Wang, J. Two Dimensional Hexagonal Boron Nitride (2D-hBN): Synthesis, Properties and Applications. *J. Mater. Chem. C* **2017**, *5*, 11992–12022.
- (25) Hamaide, G.; Allibert, F.; Hovel, H.; Cristoloveanu, S. Impact of Free-Surface Passivation on Silicon on Insulator Buried Interface Properties by Pseudotransistor Characterization. *J. Appl. Phys.* **2007**, *101*, 114513.
- (26) Henschel, W.; Georgiev, Y.; Kurz, H. Study of a High Contrast Process for Hydrogen Silsesquioxane as a Negative tone Electron Beam Resist. *J. Vac. Sci. Technol., B: Microelectron. Nanometer Struct.—Process., Meas., Phenom.* **2003**, *21*, 2018–2025.
- (27) Khan, M. B.; Deb, D.; Kerbusch, J.; Fuchs, F.; Löffler, M.; Banerjee, S.; Mühle, U.; Weber, W. M.; Gemming, S.; Schuster, J.; et al. Towards Reconfigurable Electronics: Silicidation of Top-Down Fabricated Silicon Nanowires. *Appl. Sci.* **2019**, *9*, 3462.
- (28) Gao, E.; Lin, S.-Z.; Qin, Z.; Buehler, M. J.; Feng, X.-Q.; Xu, Z. Mechanical exfoliation of Two-dimensional Materials. *J. Mech. Phys. Solids* **2018**, *115*, 248–262.
- (29) Castellanos-Gomez, A.; Buscema, M.; Molenaar, R.; Singh, V.; Janssen, L.; Van Der Zant, H. S.; Steele, G. A. Deterministic Transfer

of Two-dimensional Materials by All-Dry Viscoelastic Stamping. *2D Materials* **2014**, *1*, 011002.