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Japanese Journal of Applied Physics **64**, 088001 (2025) **BRIEF NOTE**

https://doi.org/**10.35848/1347-4065/adf380**

Step-and-terrace surface formation on (001) β-Ga_2O_3 by wet etching using 2.38 wt% tetramethylammonium hydroxide (TMAH) lithographic developer

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Received July 2, 2025; accepted July 22, 2025; published online August 6, 2025

Wet etching of (001) β-Ga_2O_3 was performed using a standard lithographic developer—an aqueous solution of 2.38 wt% tetramethylammonium hydroxide (TMAH)—at moderate temperatures of 25 °C and 40 °C. At both temperatures, the chemically-mechanically polished surfaces, which consisted of terraces with numerous pits and, in some samples, one- to two-monolayer-high islands, were gradually smoothed through a layer-by-layer etching process. This resulted in a well-defined step-and-terrace surface morphology characterized by pit-free, atomically flat terraces and monolayer steps (~0.56 nm). These findings indicate that developer-based etching offers a simple yet highly effective approach for preparing (001) β-Ga_2O_3 surfaces for subsequent epitaxial growth or device fabrication. © 2025 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

β-Ga_2O_3 is widely recognized as a promising wide-bandgap semiconductor for power electronic applications. Its high Baliga's figure of merit, approximately 8 MV cm^{-1}, exceeds those of 4H-SiC and GaN, enabling the development of low-loss, high-voltage power devices.[1)] In addition, the feasibility of melt growth facilitates the production of high-quality, large-area wafers.[2,3)] Notably, (001)-oriented wafers and carrier-density-controlled epitaxial wafers with diameters up to 4 inches are commercially available from Novel Crystal Technology, Inc. These (001) epitaxial wafers have enabled progress in vertical device demonstrations, including Schottky barrier diodes (SBDs), metal-oxide-semiconductor field-effect transistors (MOSFETs), and NiO/β-Ga_2O_3 heterojunction PN diodes (HJ-PNDs) with kV-class operation, highlighting the material's practical potential for next-generation power electronics.[4,5)]

Although the (001) orientation is currently a widely used platform for vertical device applications, atomic-level surface smoothing of (001) surfaces has not yet been investigated. Commercially available (001) wafers, including epitaxial wafers, are typically subjected to chemical-mechanical polishing (CMP), followed by a sequential cleaning process in the following order: organic solvent cleaning with ultrasonication, hydrofluoric acid (HF) cleaning, sulfuric acid-hydrogen peroxide mixture (SPM) cleaning, and a second round of organic solvent cleaning with ultrasonication. Each cleaning step was followed by rinsing in deionized (DI) water. Figures 1(a), 2(a), and 3(a) show the surface topographies of the as-received (001) substrates (chips separated from wafers), measured using blue-laser-driven tapping-mode atomic force microscopy (AFM; Jupiter XR, Oxford Instruments). The surface morphologies varied among individual samples. Some of the topmost surfaces consisted of steps and terraces with numerous pits [Fig. 1(a)], while others exhibited one- to two-monolayer-high islands on the pitted terraces [Figs. 2(a) and 3(a)]. This non-uniformity may have originated from slight variations in the CMP, HF, and/or SPM cleaning steps described above. Considering both homoepitaxy and heteroepitaxy, as well as device applications, it is desirable for the surface morphology to be uniformly composed of ordered step-and-terrace structures without pits. Therefore, in this study, we investigated two approaches-thermal annealing and wet etching-to achieve such surface morphology.

For binary metal oxide substrates, such as sapphire, TiO_2, and MgO, thermal annealing is commonly employed to obtain atomically flat, stepped surfaces.[6–8)] In the case of β-Ga_2O_3, previous studies have reported annealed surface morphologies on (100), (010), and ($\bar{2}$01) oriented substrates.[4,9–11)] Clearly defined step-and-terrace morphologies were observed only on the (100) substrates after thermal annealing at 1000 °C–1100 °C.[9,10)] In contrast, annealing of (010) and ($\bar{2}$01) substrates at temperatures ranging from 600 °C to 1150 °C resulted in narrow, line-shaped surface structures extending along the [001] and [010] directions, respectively, indicating the predominant formation of (100) facets.[4,11)]

The emergence of (100) facets during annealing was also observed on the (001) plane. To evaluate the effectiveness of thermal annealing in surface smoothing, a (001) β-Ga_2O_3 substrate was annealed using a custom-built tube furnace. A schematic of the annealing setup is shown in Fig. 4(a). The substrate was mounted on a rotating holder inside a horizontal quartz tube, and annealing was conducted at 800 °C, 900 °C, and 1000 °C under an N_2 flow of 2.00 slm at atmospheric pressure. These annealing treatments were sequentially applied to the same substrate to monitor progressive changes in surface morphology. Figure 1 presents the surface morphologies and the corresponding root-mean-square (RMS) roughness values before and after annealing. The initial step-and-terrace-like surface with many pits [Fig. 1(a)] was gradually transformed into line-shaped structures with narrow terraces (~50 nm) aligned along the [010] direction as the annealing temperature increased [Figs. 1(b)–1(d)], likely due to the formation of (100) facets. As a result of the surface transformation, the RMS roughness slightly increased from 0.17 nm (as-received) to 0.20 nm (at 1000 °C). These results suggest that to achieve a pronounced step-and-terrace morphology with wider terraces, other surface smoothing techniques should be explored.

In this context, we focused on wet etching, which is commonly employed in β-Ga_2O_3 processing to reduce

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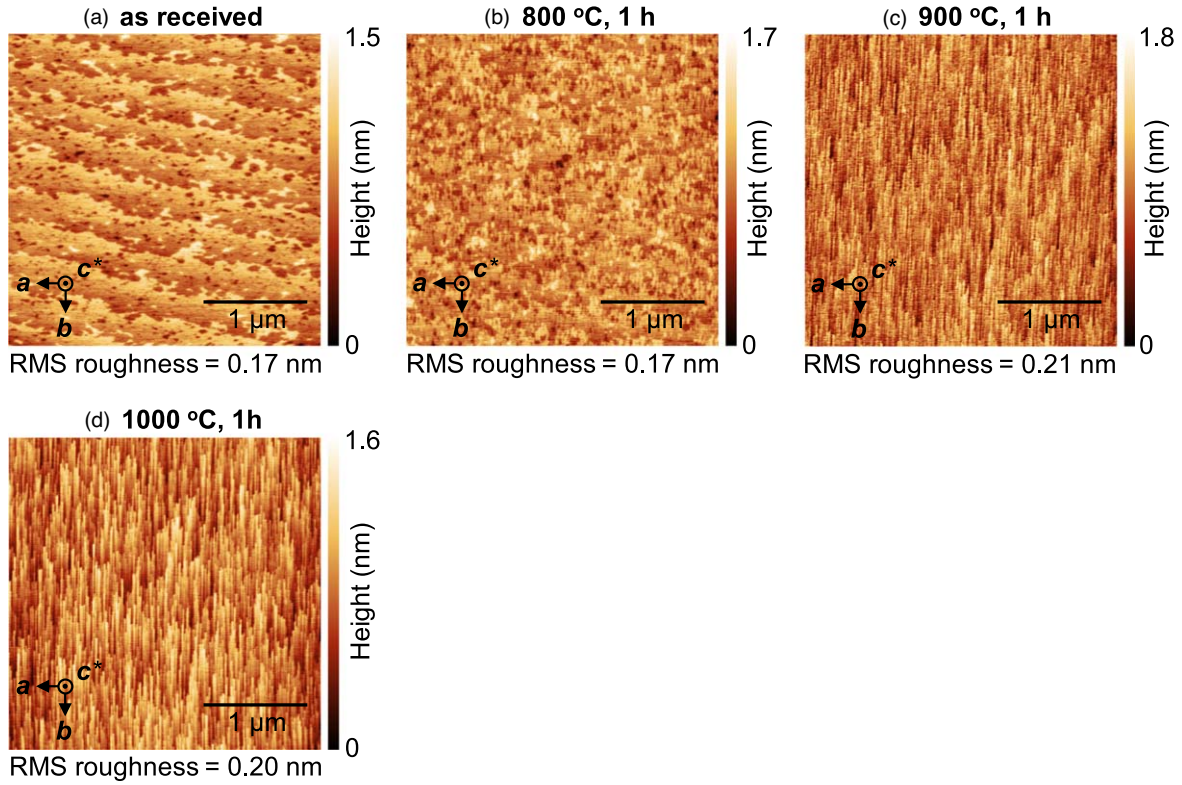

Fig. 1. (a)–(d) AFM images of a (001) β-Ga_2O_3 substrate showing the transformation of surface morphology before and after thermal annealing in a N_2 flow under the atmospheric pressure, at temperatures ranging from 800 °C to 1000 °C. The asterisk symbol of "*" denotes the reciprocal lattice vector.

surface roughness and mitigate plasma-induced damage caused by dry etching. Among various etchants investigated—such as HCl, H_3PO_4, HF, and tetramethylammonium hydroxide (TMAH)—TMAH appears to be the most effective.[12–17] H. K. Lee et al. reported that treatment with TMAH (25 wt%, 90 °C) effectively reduced the surface roughness of (001) substrates induced by Cl_2/BCl_3 inductively coupled plasma reactive ion etching (ICP-RIE), whereas treatment with SPM (H_2SO_4:H_2O_2 = 1:1, 90 °C) was less effective.[12] X. Lu et al. also confirmed the improvement of Cl_2/BCl_3-RIE-induced surface roughness by TMAH treatment.[13] F. Zhang et al. evaluated the performance of trench SBDs on (001) epitaxial wafers that were post-treated with O_2 plasma, HF (49 wt%), or TMAH (25 wt%, 90 °C) after Cl_2/BCl_3 ICP-RIE.[14] Among these treatments, the TMAH-treated devices exhibited the highest breakdown voltages (V_B), confirming the superiority of TMAH etching. A. R. Gutierrez et al. conducted X-ray photoelectron spectroscopy on (001) epitaxial substrates after BCl_3 ICP-RIE followed by post-treatments with diluted HCl (H_2O:HCl [37 wt%] = 10:1), H_3PO_4 (85 wt%), or TMAH (10 wt%, 70 °C).[15] B 1s peaks attributed to BCl_3 were still detected on the HCl- and H_3PO_4-treated surfaces but were absent on the TMAH-treated surface, indicating that TMAH effectively removed the damaged layer. Furthermore, they compared V_B values of SBDs and HJ-PNDs fabricated on ICP-RIE-processed (001) epitaxial substrates and found that the devices treated with TMAH exhibited the highest V_B. TMAH etching was also employed to remove dry etch-induced damage in the fabrication of recessed-gate and slanted-fin-channel lateral MOSFETs, although the details were not discussed.[16,17] These findings collectively suggest that TMAH is the most promising wet etchant for (001) β-Ga_2O_3.

Accordingly, we selected TMAH as the most suitable wet etchant for modifying the surfaces of CMP-treated (001) substrates. However, the aforementioned etching conditions reported in previous studies (10–25 wt%, 70 °C–90 °C) are relatively aggressive when the goal is to remove only a few irregular monolayers. To address this issue, we conducted etching experiments using a standard lithographic developer containing 2.38 wt% TMAH at moderate temperatures (25 °C–40 °C). This mild, developer-based etching approach is both safer and more straightforward than the previously reported TMAH etching methods.

The as-received (001) β-Ga_2O_3 substrates were wet etched using a surfactant-free lithographic developer-an aqueous solution of 2.38 wt% TMAH (AZ 300 MIF Developer, Merck Performance Materials GmbH). The wet etching setup is illustrated in Fig. 4(b). The etchant was maintained at either 25 °C (commonly referred to as room temperature) or 40 °C in a polytetrafluoroethylene (PTFE) beaker placed on a hot plate stirrer. The temperature was monitored and controlled using a PTFE-coated thermocouple immersed in the solution. To ensure uniform temperature distribution, the etchant was continuously stirred at 300 rpm with a PTFE-coated magnetic stir bar. The etching process was initiated by immersing the sample in the etchant and terminated by withdrawing it from the solution, followed by rinsing in DI water. After wet etching, the surface morphology was characterized by AFM. Etching and AFM observation were repeated on the same samples using fresh etchants until the cumulative etching times reached 8 h at 25 °C and 1 h at 40 °C. It should be noted that these process temperatures were well below the boiling point of the 2.38 wt% TMAH solution

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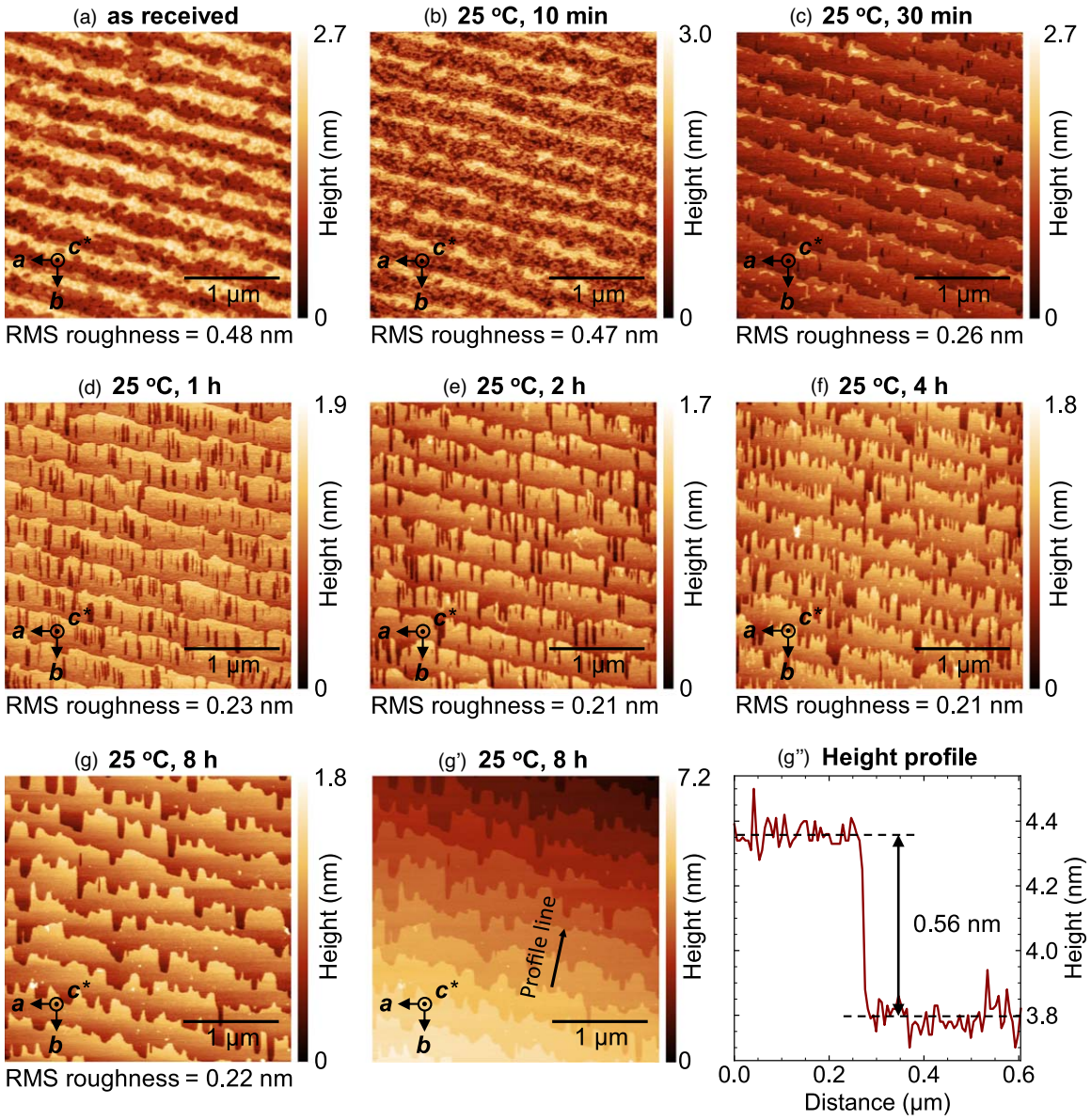

Fig. 2. (a)–(g) and (g′) AFM images of a (001) β-Ga_2O_3 substrate showing the evolution of surface morphology before and after wet etching in 2.38 wt% TMAH at 25 °C, with cumulative etching times ranging from 10 min to 8 h. The topography data in (g) and (g′) are identical but were leveled using different methods: whole-area flattening for (g) and terrace-by-terrace flattening for (g′). (g″) Height profile along the arrow line in (g′).

(100 °C), and thus evaporation was negligible under the experimental conditions.

Room-temperature developer etching successfully produced distinct step-and-terrace structures. Figures 2(a)–2(g) show AFM topography images and corresponding RMS roughness values before and after the etching process. The initial surface consisted of steps and pitted terraces with one- to two-monolayer-high islands [Fig. 2(a)]. Within the first 10 min of etching, the pits expanded while the islands decreased in size [Fig. 2(b)]. As etching progressed to a cumulative time of 30 min, most of the pitted terraces were removed but still remained as small islands near the step edges on the underlying terraces, indicating a shift in the dominant terrace level [Fig. 2(c)]. The newly exposed main terraces also contained small pits. With continued etching up to a cumulative time of 4 h, these pits expanded preferentially along the *b*-axis and extended to the step edges, resulting in the step edges being segmented into fine *b*-axis-elongated structures [Figs. 2(d)–2(f)]. This behavior indicates in-plane anisotropy in the step etch rate, with the (010) step etching faster than the (100) step. Upon further etching, most of the fine step-edge structures were removed, and a well-defined, pit-free step-and-terrace morphology was observed at a cumulative etching time of 8 h [Fig. 2(g)]. Importantly, no new pits were observed after the initial pit removal, suggesting that the etching proceeded in a layer-by-layer mode throughout the entire etching process. The corresponding RMS roughness decreased from 0.48 nm (as-received) to 0.22 nm (after 8 h), consistent with the observed surface evolution.

The observed step height indeed corresponded to the monolayer thickness of the (001) plane. Figure 2(g′) shows the AFM image obtained by planar leveling of Fig. 2(g), using a terrace region as the reference surface. A height profile was extracted along the arrowed line crossing a step, as shown in Fig. 2(g″). The height difference between the terraces was measured to be approximately 0.56 nm. This value matches the interplanar spacing of (001) cleavage

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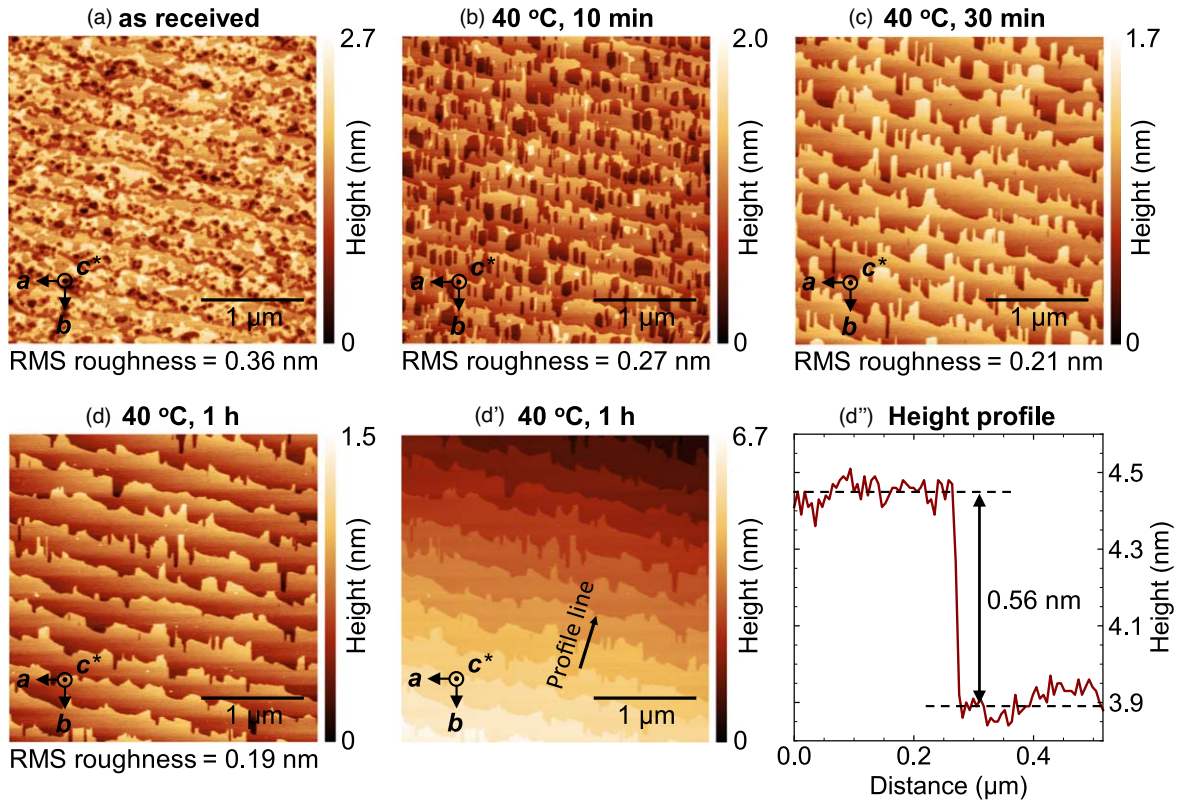

Fig. 3. (a)–(d) and (d′) AFM images of a (001) β-Ga_2O_3 substrate showing the evolution of surface morphology before and after wet etching in 2.38 wt% TMAH at 40 °C, with cumulative etching times ranging from 10 min to 1 h. The topography data in (d) and (d′) are identical but were leveled using different methods: whole-area flattening for (d) and terrace-by-terrace flattening for (d′). (d″) Height profile along the arrow line in (d′).

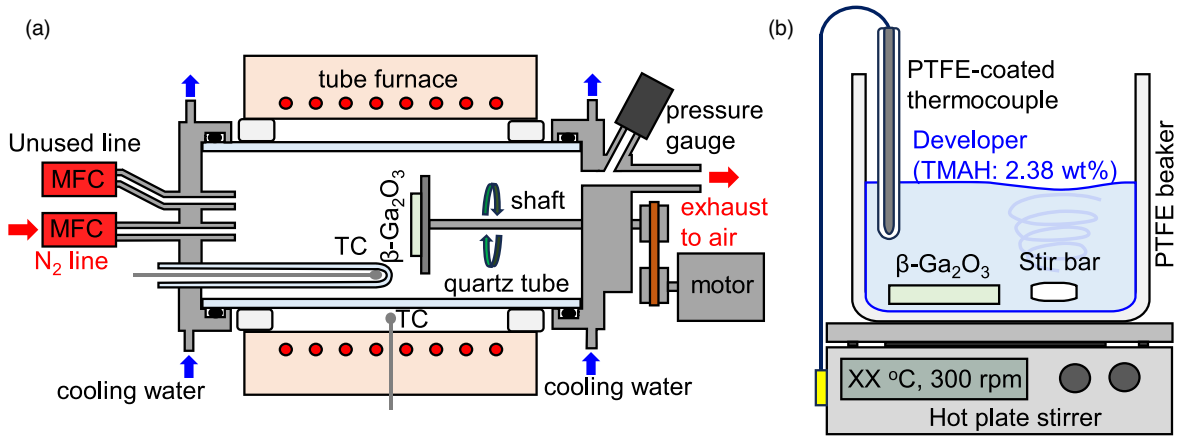

Fig. 4. Schematic illustrations of (a) the thermal annealing and (b) wet etching setups. TC and MFC refer to the thermocouples and mass flow controllers, respectively.

planes,[18,19] given by $c \sin \beta = 0.5630$ nm, calculated using the lattice parameters of β-Ga_2O_3.[20] Similar measurements at other steps confirmed that all steps were one-monolayer high and exhibited no step bunching.

Developer etching at 40 °C also produced a well-resolved step-and-terrace surface morphology similar to that obtained at 25 °C, but in a significantly shorter time. This process was also accompanied by the removal of islands, a shift in the main terrace level, expansion of pits, and smoothing of step edges, as shown in Figs. 3(a)–3(d). Accordingly, the RMS roughness decreased from 0.36 nm (as-received) to 0.19 nm (after 1 h). The etched surface morphology at 40 °C for 1 h closely resembled that at 25 °C for 8 h. Additionally, the resulting step height was equal to the monolayer thickness of the (001) plane, as shown in Figs. 3(d′) and 3(d″). Despite only a 15 °C increase in temperature, the surface treatment effect was significantly enhanced. Further increases in temperature may accelerate the surface smoothing; however, they would also cause excessive evaporation of the etchant, leading to a higher TMAH concentration and increased safety risks. Therefore, we refrained from conducting experiments at higher temperatures.

In conclusion, we have proposed a facile surface preparation technique using a standard lithographic developer to achieve a pit-free, step-and-terrace surface morphology on (001) β-Ga_2O_3 substrates—an outcome not

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attainable through conventional thermal annealing. Although the required etching durations are relatively long, the process can be conducted at low temperatures, including room temperature, which is of considerable practical significance for process implementation. In particular, developer-based etching at room temperature requires no heating equipment other than ambient air conditioning. Furthermore, owing to the ambient-temperature condition and extremely slow etching rate, no stirring system is necessary. The process can also be carried out in a sealed container, thereby improving operational safety. In addition, the technique is compatible with batch processing of large-diameter wafers and epitaxial wafers. Given these advantages, the developer-based etching method holds strong potential as a simple and effective pretreatment step for subsequent epitaxial growth or device fabrication.

All experiments were conducted using reagents and equipment in the Nanofabrication Microscopy Unit at the National Institute for Materials Science (NIMS), under the framework of the Advanced Research Infrastructure for Materials and Nanotechnology (ARIM), supported by the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan (No. JPMXP1225NM5079). This work was financially supported by a Grant-in-Aid for Scientific Research (B) from the Japan Society for the Promotion of Science (JSPS), MEXT, Japan (No. JP24K01368).

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