Planar-type SiGe thermoelectric generator with double cavity structure

S. Koike,[1] R. Yanagisawa,[1] L. Jalabert,[1] R. Anufriev,[1] M. Kurosawa,[2] T. Mori,[3] and M. Nomura[1, a)]
[1)]*Institute of Industrial Science, The University of Tokyo.*
[2)]*Department of Crystalline Materials Science, Graduate School of Engineering, Nagoya University.*
[3)]*National Institute for Materials Science.*

(*Electronic mail: nomura@iis.u-tokyo.ac.jp.)

(*Electronic mail: koike-s@iis.u-tokyo.ac.jp.)

(Dated: 28 November 2023)

Thermoelectric power generation is one of the most promising technologies, which can directly convert thermal energy into electrical energy, and is expected to be applied as power supplies for low-power electronic devices such as sensors. In particular, planar-type devices fabricated based on lithography processes not only enable devices to be significantly smaller and produced at lower cost but also take advantage of materials with smaller dimensions, such as thin films and nanowires, which have attracted much attention in recent years. SiGe is compatible with standard lithography processes and is also a promising thermoelectric material because of its low thermal conductivity. We design and fabricate a planar-type thermoelectric generator with a double cavity structure using a 240 nm thick $Si_{0.8}Ge_{0.2}$ thin film and report its performance improvement. When the temperature difference is applied to the top and bottom surfaces of the device chip, the measured power density normalized by the applied temperature is about 0.43 $\mu Wcm^{-2}K^{-2}$. Finally, the dependence of the power generation performance on SiGe film thickness is discussed. The results from our simulation show that a maximum performance of 1.75 $\mu Wcm^{-2}K^{-2}$ can be achieved by the current device structure, indicating the potential for future applications as thermoelectric energy harvesters.

I. INTRODUCTION

In various fields such as industry, agriculture, and healthcare, sensor devices enable automation, leading to improved operational efficiency. Recently the energy efficiency of low-power devices such as sensors has been rapidly improved, making it possible to drive sensors with power on the order of microwatts for some applications. Therefore, energy harvesters that generate electricity from environmental energy such as light, vibration, electromagnetic waves, and heat have been attracting attention. Especially, thermoelectric power generation, which utilizes thermal energy, has excellent durability and quietness because it has no driving parts, and is highly suitable as an energy harvester that requires semi-permanent operation. Thermoelectric materials are evaluated by a dimensionless thermoelectric figure of merit, $ZT = S^2\sigma T/\kappa$, where S (VK^{-1}) is Seebeck coefficient, σ (Sm^{-1}) is electrical conductivity, T (K) is absolute temperature, and κ ($Wm^{-1}K^{-1}$) is thermal conductivity. Since S, σ, and κ each share parameters such as carrier concentration and are difficult to control independently, complex approaches have been developed to improve thermoelectric performance[1].

In 1993, Hicks *et al.* reported that a significant enhancement of ZT can be obtained by miniaturizing the dimension of materials to the order of a few nanometers or less[2], leading research on the development of low-dimensional materials and performance enhancement through nanostructuring. Since silicon-based materials possess the advantage in nanofabrication techniques, there are many reports showing a reduction in thermal conductivity and an improvement of thermoelectric performance by nanostructuring, such as nanowires[3–5], nanocomposites[6–8], nanocrystals[9,10], porous structures[11–13], and phononic crystals[14–19]. However, such materials with small dimensions are difficult to apply to conventional device structure called vertical-type, which usually utilize bulk materials. Planar-type thermoelectric generators (TEGs)[20–29], on the other hand, can be fabricated based on thin film or nanowires formed on substrates with low cost and high throughput using lithographic processes. SiGe is also highly compatible with semiconductor processes, making it suitable for mass production using existing technology. It has been studied as a high-performance material, especially at high temperatures. However, due to its low thermal conductivity, it also shows relatively good performance even at room temperature[10,30–33].

We fabricated and evaluated a planar-type TEG based on 240 nm thick p-type $Si_{0.8}Ge_{0.2}$. In this study, the techniques for device fabrication and evaluation refer to the previous study by Yanagisawa *et al.*[29] Since we use SiGe with low thermal conductivity, nanostructuring of the material as applied to the Si film is not necessary, and thus the fabrication process is cheaper and has high throughput. The fabricated device structures are designed to maximize power density using thermal and electrical simulation based on the finite element method (FEM). The simulation results indicate that the thickness of the SiGe film has a significant impact on the power generation performance, thus the prediction of the performance of TEG with thicker films is discussed based on the measured device performance.

II. DEVICE STRUCTURE AND FABRICATION

A schematic view of the fabricated planar-type TEG is shown in Fig. 1 (a). The planar-type TEG in this study is based on p-type SiGe thin film and is classified as a uni-leg TEG

[a)]https://www.nlab.iis.u-tokyo.ac.jp/.

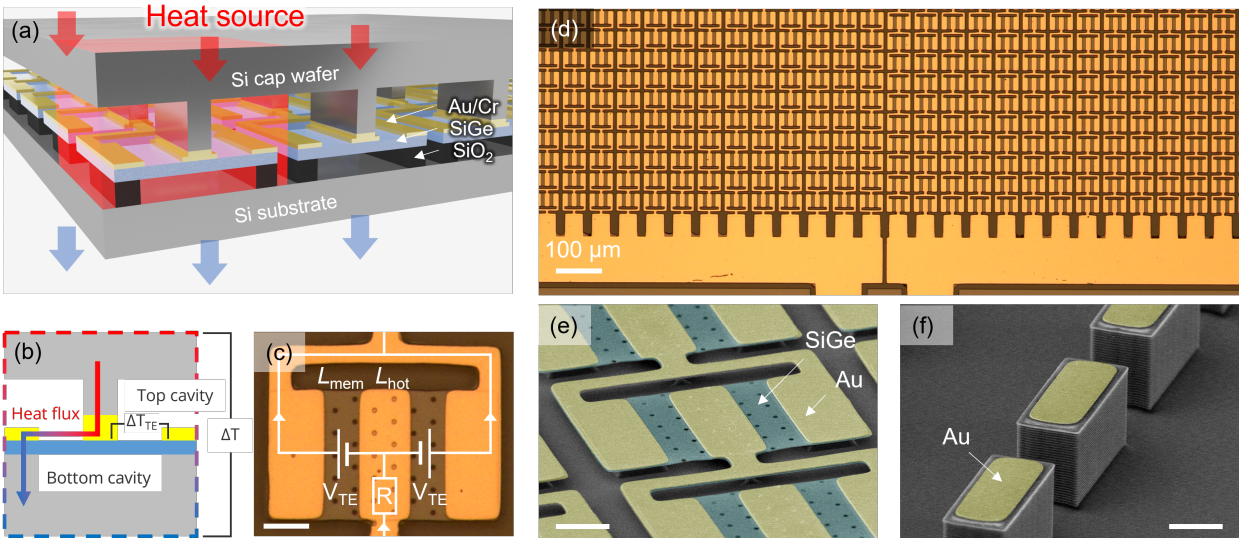

FIG. 1. (a) Schematic view of a thermoelectric generator in this work. The area shown in red is a unit cell. (b) Side view of a unit cell. Top and bottom cavities are formed to convert the temperature difference across a TEG, ΔT, into the temperature difference across the thermoelectric membranes, ΔT_{TE}. (c) Top view of a unit cell. Thermoelectric voltage in a unit cell, V_{TE}, is generated by ΔT_{TE}. R is the internal resistance of a unit cell. (d) Part of a top view of the device layer (120 in series, 20 in parallel). (e,f) SEM image of device layer and cap wafer. Scale bars in (c,e,f), 10 μm.

consisting only of n- or p-type materials. Figure 1(b) shows a cross-sectional view of a unit cell of TEG with a double cavity structure. When the top surface of the device is heated, heat flow is injected from the cap wafer and passes through the SiGe thin film in-plane direction, therefore the temperature difference applied outside the TEG (ΔT) can be efficiently converted to the temperature difference across the thermoelectric thin film (ΔT_{TE}). Figure 1(c) shows the top view of a unit cell and its equivalent electrical circuit. the ΔT_{TE} is converted thermoelectric voltage per unit cell, $V_{\mathrm{TE}} = S\Delta T_{\mathrm{TE}}$ by the Seebeck effect. Here, S is the Seebeck coefficient of the SiGe thin film, and in the figure, R is the internal electrical resistance of a unit cell.

Figure 1(d) shows many cells of TEG integrated into the device wafer. The TEG includes 2400 unit cells (120 series and 20 parallel) connected in an area of 2.36 mm $\times$ 2.65 mm. We separately fabricated the device wafer and the cap wafer and bonded them together to finalize the process. The device wafer (Fig. 1(e)) is fabricated on a p-type $Si_{0.8}Ge_{0.2}$ thin film sputtered on the SiO_2 sacrificial layer. A p-type $Si_{0.8}Ge_{0.2}$ thin film was prepared by ion implanting boron at a dose of 3×10^{20} cm^{-3} into an amorphous SiGe film and annealing at 1000 °C for 1 minute. The lithography processes are used for metal deposition to create the Au/Cr electrodes and reactive ion etching (RIE) to etch and shape the SiGe thin film. To make the bottom cavity structure in the last process for the device layer, the SiO_2 sacrificial layer is removed by vapor hydrofluoric acid treatment through holes for etching in the central part of each unit cell. The cap wafer (Fig. 1(f)) is fabricated on a Si wafer with an insulation layer of 290 nm thick SiO_2 to prevent electrical leakage through the cap wafer. Au pads are deposited to create solid contacts with the device wafer, and the surrounding part is etched to a depth of around 15 μm using Deeper RIE. Lastly, we conducted thermal compression bonding through gold pads on each wafer in the final process. Although this bonding process applies pressure to the Au pads in the contact area, the SiGe thin film with air-bridge structures is rarely broken because large Au pads are prepared outside the area of the TEG to support the cap wafer.

III. STRUCTURAL OPTIMIZATION

Structural parameters of the TEG in this study were optimized, using FEM simulations to obtain the maximum power density using the physical properties of materials shown in Table I. The values without reference in Tab. I were obtained from the COMSOL library, and blank space means that these values were not considered in the simulations. Here, the Seebeck coefficient, electrical conductivity, and thermal conductivity of SiGe thin film refer to the value from a previous study[18], where electrical and thermal measurements were performed on a SiGe thin film obtained from the same wafer. Thermal conductivity measurements were conducted by the micro time-domain thermoreflectance (μ-TDTR). Also, measured contact resistance between the Au/Cr electrode and SiGe, 110 $\Omega\mu$m^2, was applied to the simulations. The 3D model of a unit cell, as shown by the red-colored area in Fig. 1(a), was built and the V_{TE} was simulated when a temperature difference (ΔT = 1 K) was applied between the top and bottom surfaces of the device. Similarly, the internal electrical resistance of a unit cell, which also varies with structural parameters, was estimated, and it is optimized to maximize the power density P calculated from these results. In this study,

TABLE I. Physical properties of materials used in the FEM simulations.

Material	Seebeck coefficient (μVK^{-1})	Electricak conductivity (kSm^{-1})	Thermal conductivity ($Wm^{-1}K^{-1}$)	Density (kgm^{-3})	Heat capacity ($Jkg^{-1}K^{-1}$)
p-type SiGe membrane	113 (measured)	19.7 (measured)	1.93 (measured)	2920	604
Si	-	-	130	2329	700
SiO_2	-	-	1.38	2203	703
Au	-	45600	317	19300	129
Air	-	-	0.263	1.18	1006

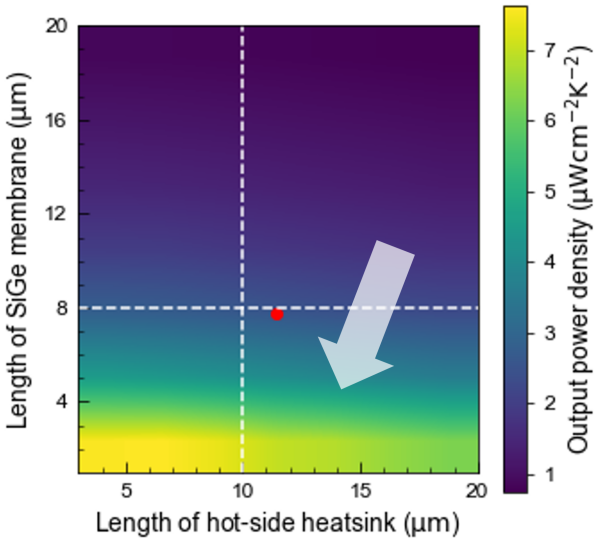

FIG. 2. Structural parameter dependence of output power density. Important parameters (length of the SiGe membrane, L_{mem}, length of the hot side heatsink, L_{hot}) are optimized to maximize the output power density. Although smaller structures for both parameters showed larger performance, a structure with larger structures than white broken lines is fabricated in terms of the process yield rate. The red plot shows the structure of the fabricated TEG.

TEG performance is evaluated by the power density normalized by ΔT, P ($\mu\mathrm{Wcm}^{-2}\mathrm{K}^{-2}$) = $V^2/(4RA\Delta T^2)$. Here, V is the open-circuit voltage of the TEG, R is the internal electrical resistance of the TEG, and A is the area occupied by the TEG. More details of the simulation can be found in our previous study[33].

Figure 2 shows a color map of power density depending on the length of the SiGe thin film, L_{mem}, and the length of the hot-side heatsink in each unit cell, L_{hot}, (Fig. 1(c)), which had a significant impact on device performance among the TEG structural parameters. The shorter L_{mem} in the range of the plot results in better performance, which is attributed to the reduction in the electrical resistance of the device and the footprint of a unit cell. Although the temperature difference across the SiGe thin film, ΔT_{TE}, becomes smaller because thermal resistance in thin films is reduced by making L_{mem} shorter, the effect is relatively small on this scale ($L_{\mathrm{mem}} > 1$ μm). Furthermore, it is indicated that the performance would be better with a smaller L_{hot} structure mainly due to the footprint. In this study, from the viewpoint of process yield, the TEG is designed with the minimum dimensions of L_{mem} = 8 μm and L_{hot} = 10 μm, as shown by the broken lines. The red plot shows the actual fabricated TEG structure (L_{mem} = 7.7 μm, L_{hot} = 11.4 μm), which was expected to achieve the performance of about 2.3 $\mu\mathrm{Wcm}^{-2}\mathrm{K}^{-2}$ from simulation.

IV. PERFORMANCE OF FABRICATED TEG

The open-circuit voltage of the TEG was measured under a temperature difference applied to the top and bottom surfaces of the chip. Figure 3(a) shows the measured open-circuit voltage, showing linear trends depending on the applied temperature difference of 20 K or less under room temperature. The measurements were conducted under vacuum as well as in the atmosphere, and almost the same voltages generated under both conditions. This result means that solid contacts were successfully formed between the device and the cap wafer because if a critical defect occurred during the wafer bonding process, almost no thermoelectric voltage can be generated in a measurement under a vacuum, where heat transport by air is eliminated. The linear fitting of the values measured in the atmosphere yields an open-circuit voltage divided by an applied temperature difference of 4.48 mVK^{-1}. On the other hand, the data shown by the solid line is the voltage expected in an ideal device structure, simulated by FEM, with a slope of 11.08 mVK^{-1}, where ΔT_{TE} is 0.81 K (ΔT_{TE} / ΔT = 81 %). The ΔT_{TE} in our TEG was calculated to be approximately ΔT_{TE} / ΔT = 32.8 %, which is a temperature difference of about 40 % compared to the simulation.

The power density was then calculated using the measured open circuit voltage, the internal electrical resistance (182 Ω), and the footprint that includes the wiring between unit cells (Fig. 3(b)). Measurements in the atmosphere showed that a power density of approximately 100 $\mu\mathrm{Wcm}^{-2}$ was achieved at ΔT = 15 K. The power density divided byΔT is 0.43 $\mu\mathrm{Wcm}^{-2}\mathrm{K}^{-2}$, which is the best performance among planar-type TEGs using SiGe reported so far.

V. POTENTIAL IMPROVEMENT IN DEVICE PERFORMANCE

The FEM simulation results suggest that the thickness of the SiGe film is effective in improving TEG performance. The

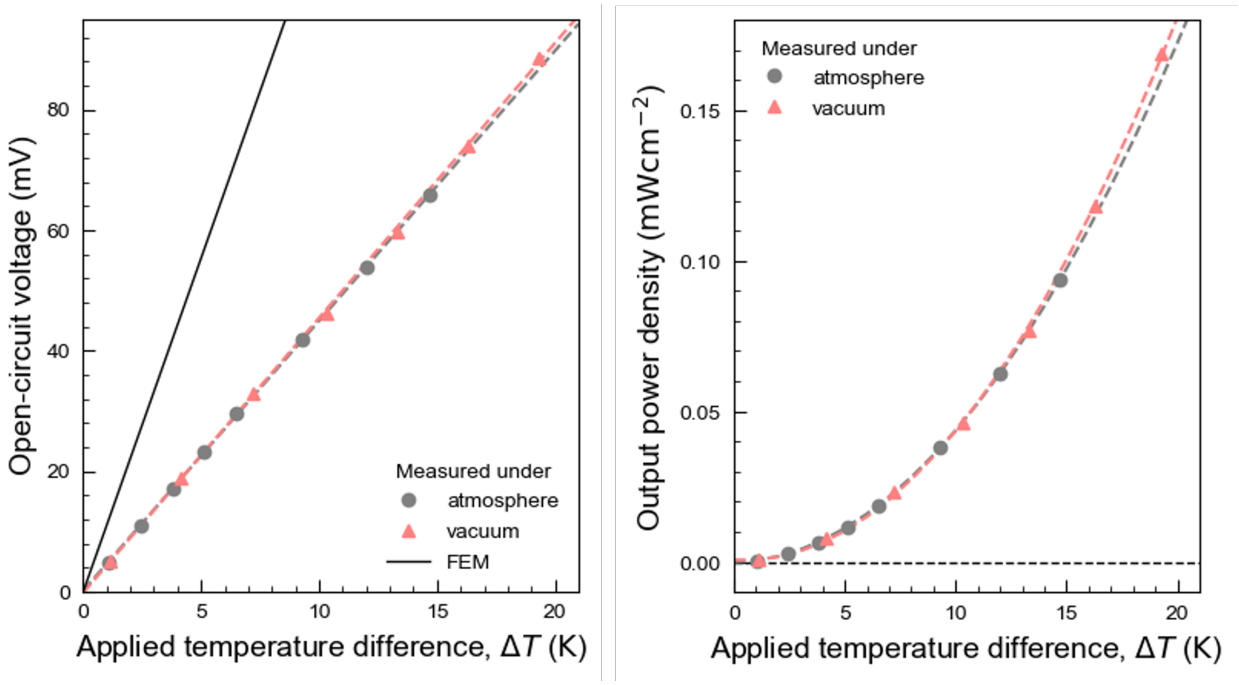

FIG. 3. Measured (a) open-circuit voltage and (b) output power density under atmosphere and vacuum. They have similar values showing that solid contacts are formed between the device layer and the cap wafer. The solid line shows the estimated open-circuit voltage from the FEM simulation where the contact between the device layer and the cap wafer is ideal.

gray plot in Fig. 4(a) shows the performance when only the thickness of the SiGe film is changed from the structure of the TEG fabricated in this study. It is significantly enhanced by increasing the film thickness from 240 nm, attributed to the reduction in electrical resistance of the device. The power density normalized by ΔT reached 9.45 μWcm^{-2}K^{-2} at a film thickness of 3.5 μm. In an even thicker film, the influence of the decrease in ΔT_{TE} due to the reduction in thermal resistance of SiGe film becomes significant and the performance begins to degrade. The plot in red circles shows the measured value and the expected device performance is shown by the solid red line, assuming that the trend from the simulation is followed. Since the TEG fabricated in this study does not include complex fabrication processes, TEG with a thicker SiGe film can be fabricated, whose maximum performance is estimated to be 1.75 μWcm^{-2}K^{-2}. Figure 4(b) shows the performance measured in this study along with the main previous studies of planar-type TEGs with Si-based materials. Up to now, that of planar-type TEGs reported using SiGe has been up to 0.25 μWcm^{-2}K^{-2}, and the results of this study exceed this performance. The normalized power density of 1.75 μWcm^{-2}K^{-2}, which can be achieved by using a thicker SiGe film, is the best performance among planar-type TEGs fabricated with Si-based materials.

VI. CONCLUSION

In this work, we designed and fabricated a planar-type TEG with a double-cavity structure based on a p-type $Si_{0.8}Ge_{0.2}$ thin film, and achieved the normalized power density of 0.43 μWcm^{-2}K^{-2}, the best performance ever reported for SiGe planar-type TEGs. There are two main reasons that contribute to the performance improvement. The first reason is that our device is carefully designed to maximize its performance through thermal and electrical simulations. The structure fabricated in this study was determined considering the yield of our process, but a higher precision lithography process would provide several times higher performance. The second reason is the double cavity structure that thermally insulates the device wafer and cap wafer, which increases the temperature difference across a thermoelectric thin film. Since our device is composed of two different wafers, it has more flexibility in designing the cavity structure than conventional top-down processes.

Moreover, we investigated the effect of utilizing thicker SiGe films on the TEG performance by FEM simulation to predict the potential performance of SiGe planar-type TEGs and showed that a significant improvement can be achieved based on the current fabrication techniques. The device with thicker film has the best data among planar-type TEGs using Si-based materials and is considered to be promising as a thermoelectric energy harvester.

ACKNOWLEDGMENTS

This work was supported by JST CREST Grant No. JPMJCR19Q3, JST Mirai Grant No. JPMJMI19A1, and Kakenhi Grant No. 21H04635.

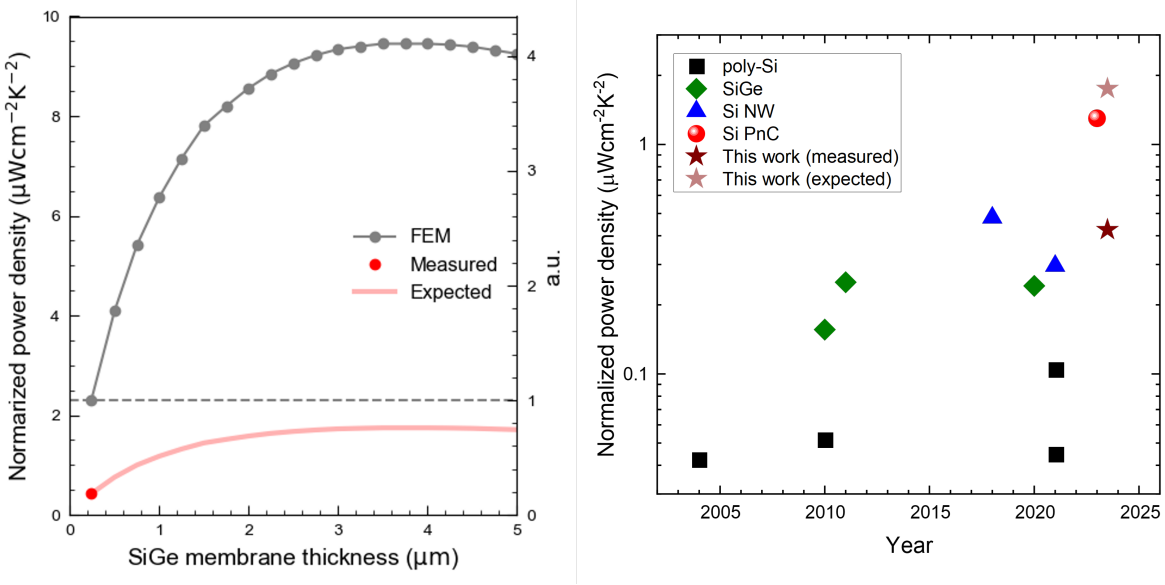

FIG. 4. (a) Grey plots show SiGe membrane dependence of simulated output power density. The red plot and line show the measured and expected performance based on the trend of results from FEM simulations, respectively. (b) Comparison of TEG power factors of hybrid planar-type Si devices reported in the last decades. Colors represent the different material groups[20–29].

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

[1] G. J. Snyder and E. S. Toberer, "Complex thermoelectric materials," Nature materials **7**, 105–114 (2008).

[2] L. D. Hicks and M. S. Dresselhaus, "Effect of quantum-well structures on the thermoelectric figure of merit," Physical Review B **47**, 12727 (1993).

[3] A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar, and P. Yang, "Enhanced thermoelectric performance of rough silicon nanowires," Nature **451**, 163–167 (2008).

[4] W. Park, D. D. Shin, S. J. Kim, J. S. Katz, J. Park, C. H. Ahn, T. Kodama, M. Asheghi, T. W. Kenny, and K. E. Goodson, "Phonon conduction in silicon nanobeams," Applied Physics Letters **110** (2017).

[5] L. Yang, Y. Yang, Q. Zhang, Y. Zhang, Y. Jiang, Z. Guan, M. Gerboth, J. Yang, Y. Chen, D. G. Walker, *et al.*, "Thermal conductivity of individual silicon nanoribbons," Nanoscale **8**, 17895–17901 (2016).

[6] J. Stoetzel, T. Schneider, M. M. Mueller, H.-J. Kleebe, H. Wiggers, G. Schierning, and R. Schmechel, "Microstructure and thermoelectric properties of si-wsi2 nanocomposites," Acta Materialia **125**, 321–326 (2017).

[7] M. S. Dresselhaus, G. Chen, M. Y. Tang, R. Yang, H. Lee, D. Wang, Z. Ren, J.-P. Fleurial, and P. Gogna, "New directions for low-dimensional thermoelectric materials," Advanced materials **19**, 1043–1053 (2007).

[8] S. Yamasaka, Y. Nakamura, T. Ueda, S. Takeuchi, and A. Sakai, "Phonon transport control by nanoarchitecture including epitaxial ge nanodots for si-based thermoelectric materials," Scientific Reports **5**, 14490 (2015).

[9] L. Yang and A. J. Minnich, "Thermal transport in nanocrystalline si and sige by ab initio based monte carlo simulation," Scientific reports **7**, 44254 (2017).

[10] G. Joshi, H. Lee, Y. Lan, X. Wang, G. Zhu, D. Wang, R. W. Gould, D. C. Cuff, M. Y. Tang, M. S. Dresselhaus, *et al.*, "Enhanced thermoelectric figure-of-merit in nanostructured p-type silicon germanium bulk alloys," Nano letters **8**, 4670–4674 (2008).

[11] J. Tang, H.-T. Wang, D. H. Lee, M. Fardy, Z. Huo, T. P. Russell, and P. Yang, "Holey silicon as an efficient thermoelectric material," Nano letters **10**, 4279–4283 (2010).

[12] J.-H. Lee, G. A. Galli, and J. C. Grossman, "Nanoporous si as an efficient thermoelectric material," Nano letters **8**, 3750–3754 (2008).

[13] J. Lim, H.-T. Wang, J. Tang, S. C. Andrews, H. So, J. Lee, D. H. Lee, T. P. Russell, and P. Yang, "Simultaneous thermoelectric property measurement and incoherent phonon transport in holey silicon," ACS nano **10**, 124–132 (2016).

[14] M. Nomura, Y. Kage, D. Müller, D. Moser, and O. Paul, "Electrical and thermal properties of polycrystalline si thin films with phononic crystal nanopatterning for thermoelectric applications," Applied Physics Letters **106** (2015).

[15] R. Anufriev, R. Yanagisawa, and M. Nomura, "Aluminium nanopillars reduce thermal conductivity of silicon nanobeams," Nanoscale **9**, 15083–15088 (2017).

[16] M. Nomura, J. Shiomi, T. Shiga, and R. Anufriev, "Thermal phonon engineering by tailored nanostructures," Japanese Journal of Applied Physics **57**, 080101 (2018).

[17] R. Anufriev, J. Maire, and M. Nomura, "Reduction of thermal conductivity by surface scattering of phonons in periodic silicon nanostructures," Physical Review B **93**, 045411 (2016).

[18] S. Koike, R. Yanagisawa, M. Kurosawa, R. Jha, N. Tsujii, T. Mori, and M. Nomura, "Effect of nanostructuring on thermoelectric performance of sige thin films," Japanese Journal of Applied Physics **62**, 095001 (2023).

[19] M. Nomura, R. Anufriev, Z. Zhang, J. Maire, Y. Guo, R. Yanagisawa, and S. Volz, "Review of thermal transport in phononic crystals," Materials Today Physics **22**, 100613 (2022).

[20] S. Yang and L. Chung, "A thermoelectric energy generator with double cavity design by single polysilicon layer in standard cmos process," IEEE Sensors Journal **21**, 23799–23805 (2021).

[21] S. Yang, M. Cong, and T. Lee, "Application of quantum well-like thermocouple to thermoelectric energy harvester by bicmos process," Sensors and Actuators A: Physical **166**, 117–124 (2011).

[22] S. Yang, J. Wang, and M. Chen, "On the improved performance of thermoelectric generators with low dimensional polysilicon-germanium thermocouples by bicmos process," Sensors and Actuators A: Physical **306**, 111924 (2020).

[23] L. Fonseca, I. Donmez-Noyan, M. Dolcet, D. Estrada-Wiese, J. Santander, M. Salleras, G. Gadea, M. Pacios, J.-M. Sojo, A. Morata, *et al.*, "Transitioning from si to sige nanowires as thermoelectric material in silicon-based microgenerators," Nanomaterials **11**, 517 (2021).

[24]M. Tomita, S. Oba, Y. Himeda, R. Yamato, K. Shima, T. Kumada, M. Xu, H. Takezawa, K. Mesaki, K. Tsuda, *et al.*, "Modeling, simulation, fabrication, and characterization of a $10-\mu\mathrm{W/cm}^2$ class si-nanowire thermoelectric generator for iot applications," IEEE Transactions on Electron Devices **65**, 5180–5188 (2018).

[25]M. Strasser, R. Aigner, C. Lauterbach, T. Sturm, M. Franosch, and G. Wachutka, "Micromachined cmos thermoelectric generators as on-chip power supply," Sensors and Actuators A: Physical **114**, 362–370 (2004).

[26]J. Xie, C. Lee, M.-F. Wang, Y. Liu, and H. Feng, "Characterization of heavily doped polysilicon films for cmos-mems thermoelectric power generators," Journal of Micromechanics and Microengineering **19**, 125029 (2009).

[27]S. Yang and S. Wang, "Development of a thermoelectric energy generator with double cavity by standard cmos process," IEEE Sensors Journal **21**, 250–256 (2020).

[28]J. Su, V. Leonov, M. Goedbloed, Y. van Andel, M. De Nooijer, R. Elfrink, Z. Wang, and R. Vullers, "A batch process micromachined thermoelectric energy harvester: fabrication and characterization," Journal of Micromechanics and Microengineering **20**, 104005 (2010).

[29]R. Yanagisawa, S. Koike, T. Nawae, N. Tsujii, Y. Wang, T. Mori, P. Ruther, O. Paul, Y. Yoshida, J. Harashima, *et al.*, "Planar-type silicon thermoelectric generator with phononic nanostructures for 100 {\mu} w energy harvesting," arXiv preprint arXiv:2307.11382 (2023).

[30]B. Yu, M. Zebarjadi, H. Wang, K. Lukas, H. Wang, D. Wang, C. Opeil, M. Dresselhaus, G. Chen, and Z. Ren, "Enhancement of thermoelectric properties by modulation-doping in silicon germanium alloy nanocomposites," Nano letters **12**, 2077–2082 (2012).

[31]M. Takashiri, T. Borca-Tasciuc, A. Jacquot, K. Miyazaki, and G. Chen, "Structure and thermoelectric properties of boron doped nanocrystalline si0. 8ge0. 2 thin film," Journal of Applied Physics **100** (2006).

[32]J. Lu, R. Guo, W. Dai, and B. Huang, "Enhanced in-plane thermoelectric figure of merit in p-type sige thin films by nanograin boundaries," Nanoscale **7**, 7331–7339 (2015).

[33]S. Koike, R. Yanagisawa, M. Kurosawa, and M. Nomura, "Design of a planar-type uni-leg sige thermoelectric generator," Japanese Journal of Applied Physics **59**, 074003 (2020).