Assessing Degradation in Perovskite Solar Cells via Thermal Hysteresis of Photocurrent and Device Simulation

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ABSTRACT

Understanding the degradation mechanisms of perovskite solar cell (PSC) is paramount to addressing stability-related issues. Photocurrent loss is widely observed in the degraded PSC. Here, we investigate the degradation of PSC by probing the thermal hysteresis of photocurrent (THPC) and the dynamics of thermally active ionic or recombination processes. Degraded devices exhibit a considerably higher degree of variation in the photogenerated current, encompassing a broad spectrum of photo-induced ionic charge accumulation. THPC reveals changes driven by the accumulation of interfacial ionic charges and active defects under photo-thermal drifting, as supported by capacitance analysis. Device simulation corroborates that the interfacial surface defect formed at the interfacial layer in the device structure wields a substantial influence on device degradation, particularly in cases of photocurrent loss. This study underscores the direct correlation between the degradation of PSC and the presence of thermally activated traps and interfacial charge accumulation emphasizing the importance of passivating these pathways to improve device stability.

Keywords: Perovskite degradation; interfacial defect; ion migration; thermal hysteresis of photocurrent; capacitance spectra; SCAPS simulation

1. Introduction

Perovskite solar cell (PSC) under operation accelerates the loss of power conversion efficiency (PCE).[1,2] The degradation is caused by external factors such as irradiation, heat, moisture, oxygen, electric bias, and strain. [3–9] The degradation mechanism is stimulated with increased chemical kinetics at elevated temperatures under illumination, leading to interfacial deterioration. The defects in perovskite induced by aging can significantly deteriorate the transport properties and device parameters.[10–12] The defects in perovskites have been inferred indirectly by simulating the current–voltage characteristics of PSC. Since the photocurrent loss is usually observed in degraded PSCs, monitoring photocurrent under different conditions could provide insights for understanding the intrinsic factor of the device degradation. Direct monitoring of the electrically active defects in the absorber layer has been reported by thermal spectroscopy techniques such as deep-level transient spectroscopy (DLTS),[13–15] photo-induced current transient spectroscopy (PICTS),[16,17] thermal admittance spectroscopy (TAS),[8,18–20] and thermally stimulated current (TSC).[21] These techniques are more sensitive and able to detect the defects. DLTS and PICTS monitor rapid changes in the capacitance/photoconductivity after repeated electrical/optical pulses carried out during the thermal scan. TSC is a simple and effective method for determining the defect levels in semiconductors with high resistivity. It is useful as it can be applied to any kind of electric field profile settled within the sample, including the ohmic configuration. TSC spectra can be done either by applying an electric or illuminating the photoactive materials.[22,23] The photocurrent is driven by varying temperatures under different heating and cooling rates. Heating-rate variation and delayed-heating methods have been applied to investigate possible overlapping components occurring in TSC emissions. A few works using thermally stimulated current on perovskites have been reported, focusing, in particular, on low-temperature ranges, below 300 K. The temperature of PSC could easily reach 35–55 ^{o}C under working conditions. The cause of operational instability of PSC at elevated temperatures remains elusive. Therefore, understanding the intrinsic defect-activation in under-device operation is important for tracking the degradation propagation.

In this work, we monitored the thermal-driven photocurrent in PSC using a Paios measurement system with the user-defined current probing condition. Thermal hysteresis of photocurrent (THPC) was performed at various driving rates of temperatures (240- 360 K) under white light illumination. Heating-rate variation and delayed-heating methods have been applied to investigate possible overlapping components occurring in THPC emissions. The THPC data demonstrated a stark difference in photocurrent variation under different rates of temperature variation for the fresh and degraded devices. We have carried out device simulation using SCAPS a one-dimensional solar cell simulation program for understanding device degradation phenomena.[8,24] These experimental and simulation results corroborate the insights into the degradation route mechanism behind the photocurrent loss in PSCs. The degradation trend could be attributed to an interfacial surface defect in the device structure which supports the experimental observation.

2. Results and discussion

Figure 1a depicts the schematics of the inverted PSC configuration. The details of device fabrication are given in the supporting information and our earlier reports.[20,25,26] In brief, we have prepared halide perovskite (HP) of composition $CH_3NH_3PbI_{3-x}Cl_x$ by a two-step method followed by methylammonium chloride vapor ambient annealing. It has been documented that the Cl inclusion is benign for the growth of better film morphology and hence optoelectronic quality.[27,28] Figure 1b shows a set of representative current-voltage (J-V) curves of the fresh and aged PSCs. The fresh device of PCE is ~ 16.35% (J_{SC}~ 21.43 mAcm^{-2}, V_{OC}~ 0.998 V, and *FF*~ 0.746) and the PCE of the PSC dropped to 6.14% (J_{SC}~ 12.59 mAcm^{-2}, V_{OC}~ 1.06 V, and *FF*~ 0.460) for the aged PSC placed at under heat and light stress (~323 ± 5 K and 1500 hours under continuous illumination). A set of J-V curves for fresh and aged PSCs and statistics of device parameters are given in supporting information (Fig. S1 and S2). We notice a significant drop in photocurrent and *FF* while photovoltage slightly increases. The drop in FF is attributed to the increase in series resistance i.e., the resistivity of the contact layer with aging.[9] The drop in PCE driven by photocurrent and FF has been widely reported in degradation studies.[11,29,30] It could be due to the deterioration of the interface quality, formation of recombination states, and increase in defect density in perovskite bulk or interface under thermal and light stress.

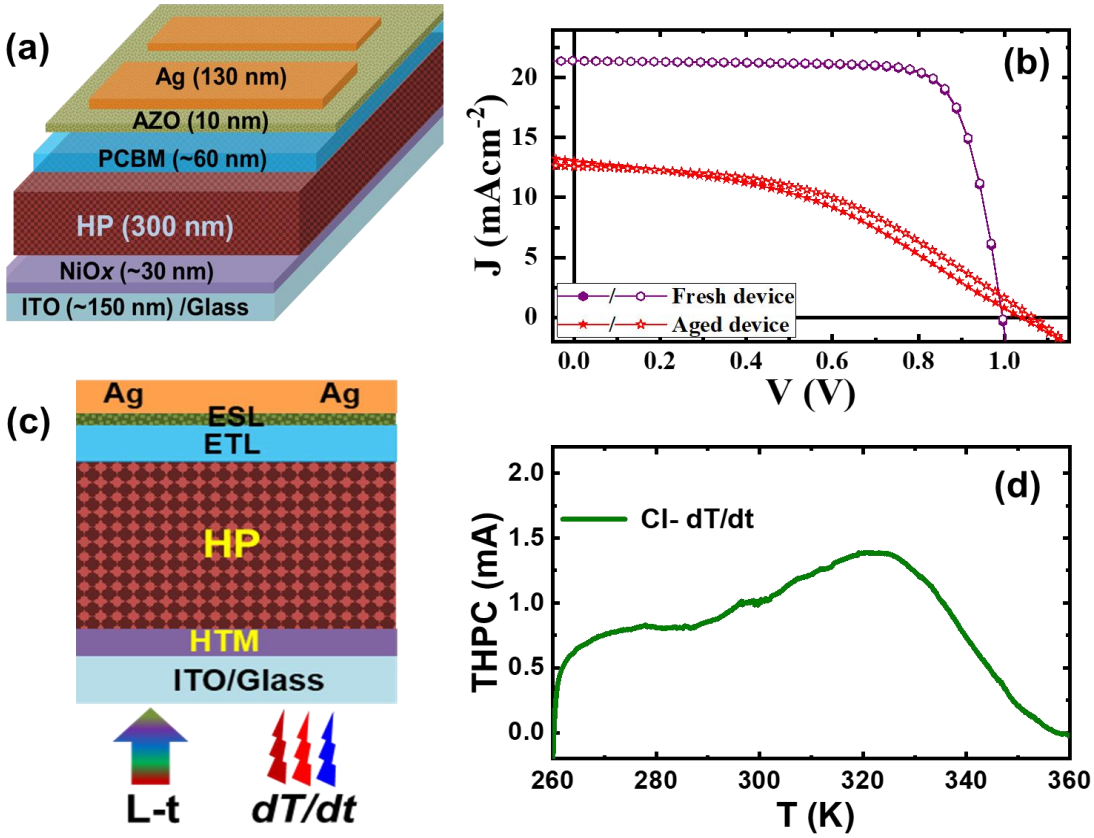

Figure 1. Schematic of the inverted PSC (a) device structure and (b) J-V curves of fresh and aged PSCs. (c) schematic of the THPC measurement and (d) THPC spectra under continuous illumination (CI).

2.1. Perovskite solar cells and THPC analysis

THPC delves into the intricacies of charge defect or charge accumulation within semiconductor devices. This method, in particular, can be utilized to unravel the factors contributing to the reduction in photocurrent in PSC operating under conditions akin to the real-world working temperature range. THPC analysis involves a meticulous exploration of the thermally stimulated photocurrent.

Figure 1c shows the schematic of THPC measurement (Fig. S3a-c) under different illumination conditions. THPC spectrum is an absolute difference between the heating and cooling photocurrent. THPC spectra are showcased, offering valuable insights into the behavior of these solar cells. During this experimental process, free carriers that are initially excited by incident light become entrapped by defects within the material, which can occur under either heating or cooling conditions. The THPC spectrum provides a distinctive signature of charge accumulation, or specific defect levels presented within the perovskite absorber material, whether embedded within the crystal lattice or localized at grain boundaries.

Considering carrier dynamics, the concentration of electrons with varying rates of temperature change can be analyzed by accounting for the kinetic equation.[31,32] THPC spectra can be resolved by assigning the defect level with the multiple peak analysis. The following equations can analyze the thermal energy at T (E_{th}) and effective charge using thermal hysteresis of photocurrent (Q_{THPC}),

$$E_{th} = k_B T \qquad [1]$$

$$Q_{THPC} = \frac{1}{\beta T} \int_{T_1}^{T_2} I_{THPC}^{T_t} \, dT \qquad [2]$$

Where T_t is a resonance temperature peak in the THPC curve, k is the Boltzmann constant, β (K/s) is heating or cooling rate. Details of mathematical analysis are discussed in the Supporting Information.

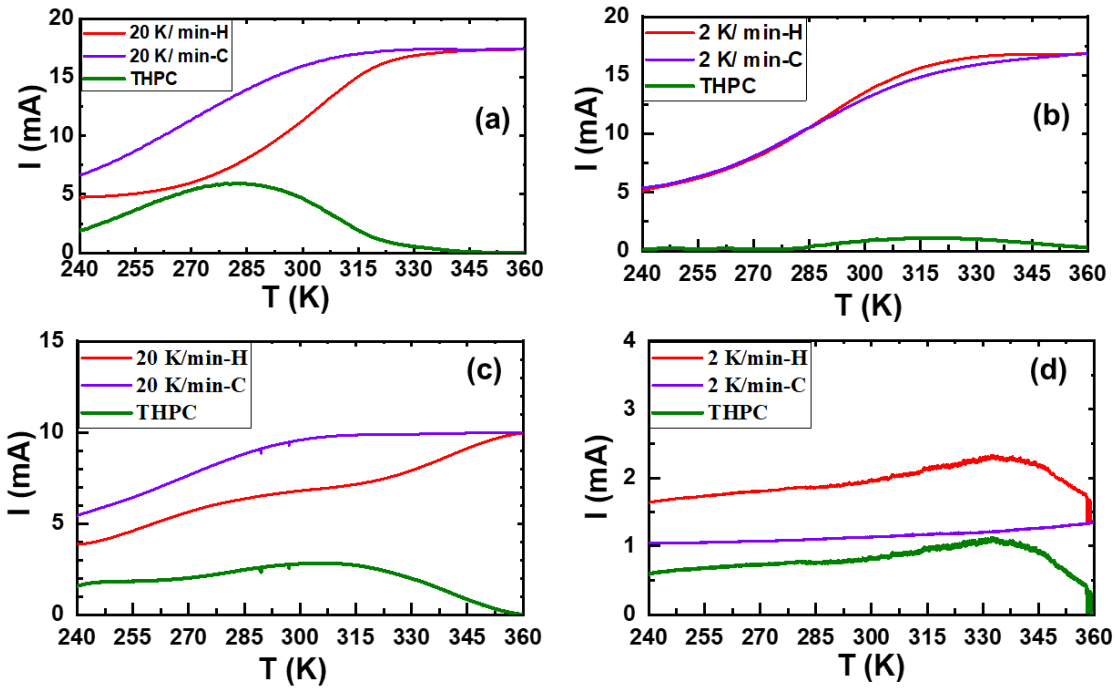

Figure 2. THPC spectra of the fresh PSCs under different temperature drifting rates: (a) 20 K/min and (b) 2 K/min in the temperature range (240-360 K) and corresponding THPC spectra of the aged devices (c, d), respectively.

Firstly, we have monitored the THPC under dark (D-dT/dt), transient illumination (TI-dT/dt), and continuous illumination (CI-dT/dt) as depicted in supporting information (Fig. S3d-f). To focus on the real-time scenario under continuous illumination, we have accounted for the THPC under continuous illumination (CI-dT/dt). Figure 2 displays the photocurrent in PSC at varying temperatures from 240-360 K with heating or cooling rates of 20 K/min and 2 K/min. This temperature range mirrors the operating conditions of PSCs in the real world. For the fresh PSC (Fig. 2a,b), the heating and cooling photocurrent shows much-pronounced photocurrent hysteresis for a faster temperature gradient rate (~ 20 K/min) while that for a slower temperature gradient rate (~ 2 K/min) has low THPC. This observation is attributed to photocurrent saturation through thermal emission in a slow temperature gradient. On the other hand, for the aged PSC (Fig. 2c,d), the photocurrent driving under heating and cooling revealed a stark difference compared to the fresh PSC. Importantly, the aged device showed more loss in cooling photocurrent under a temperature gradient of 2 K/min (Fig. 2c). This could be the consequence of saturated ions or charge accumulation at the deleterious interface in aged devices induced by slower thermal stress in heating up. It suggests that, in aged PSC, the defects or interfacial charge/ions accumulation within the material are more responsive to temperature drift. These aspects are discussed in more depth taking into account capacitance analysis and device simulations in the succeeding section.

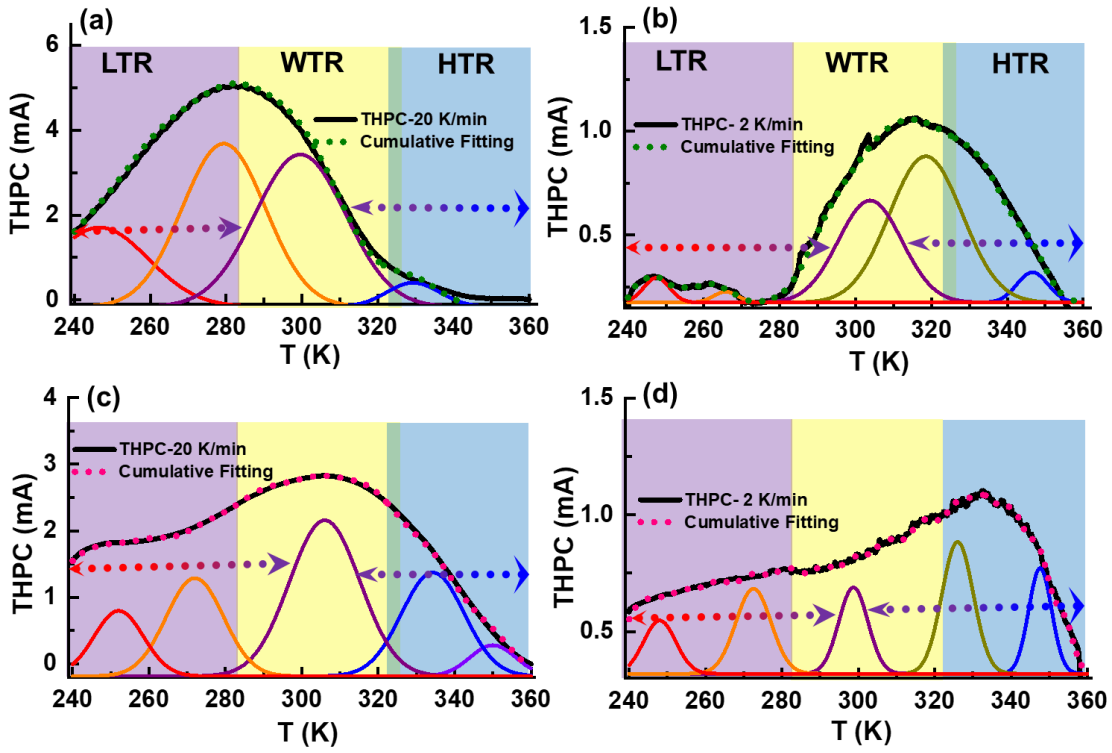

Figure 3. THPC spectra of the fresh (a, b) and aged (c, d) PSCs under different temperature drifting rates: 20 K/min and 2 K/min in the temperature range (240-360 K) and corresponding fitting spectra,

respectively. Here the shaded regions indicate a low-temperature range (LTR), working temperature range (WTR), and high-temperature range (HTR). The three curves under THPC spectra display representative spectral fitting under the LTR, WTR, and HTR regimes. The dotted arrows represent arbitrary multiple peaks (T_1, …. ,T_n) fitting of THPC spectra. The accumulated charge is calculated by evaluating the area under respected fitted curves in detailed (Fig. S4).

To study the THPC quantitatively, we performed a simultaneous multiple peak analysis method to explore the THPC spectra.[33,34] The THPC spectra (solid line), and the cumulative fitting curves (dot line) are shown in Fig. 3 (detail fitted curves in Fig. S4). THPC curves were fitted considering arbitrary resonance temperatures for perfect fitting. Accounting Eq. 2, we estimated the amount of charge under the THPC curves at three temperature ranges defined as LTR ~240 to 283 K, WTR ~ 283 to 323 K, and HTR ~ 323 to 360 K. The charge values calculated for different temperature regimes are listed in Tables S1 and S2. A lower value under a certain temperature range of the charge profile correlates to a less active defect or passive photo quenching. For fresh PSC (Fig. 3a,b; Table S1), more charge accumulates at elevated temperatures as the device works under a slow-temperature gradient. It is to be noted that the solar cells have slow temperature drifting in real working ambient. It implies that the PSC operating at 358 K could be dominantly triggered by accumulated charge or deep defects. It has been documented that the fresh PSC comprises shallower defect states such as iodine-related defects such as I_i, V_I, and I_{Pb}.[35,36] The THPC in fresh devices could be triggered by pseudo-charge accumulation and meta-stable defect dynamics under thermal stress. Conversely, the TSC for degraded PSC is active under a wider temperature range compared to the fresh device as shown in Fig. 3c,d and Table S2. The charge distribution profile differs significantly suggesting a deleterious effect over a broader temperature range in the degraded device compared to the fresh one. Unlike the fresh device, the thermally triggered defect states or interfacial charge accumulation are energetically active and contribute to capturing the photogenerated carrier via non-radiative recombination under fast (20 K/min) and slow (2 K/min) thermal drifting. These photoactive defects and charge accumulation formed in the PSC with aging have a dominant effect on the loss of photocurrent. It suggests the importance of the passivation of deep defects and controlling the extent of charge accumulation to decelerate the device degradation under light, electric, and thermal stress.[6,10] Therefore, it is imperative to passivate the intrinsic instability of perovskite by material engineering coupled with defect resistive interface to improve the operational stability of PSCs.

2.2. Capacitance and device degradation

To evaluate the interfacial deterioration of the PSCs, we investigated the capacitance spectra at different thermal stresses. The capacitance characteristics were analyzed by the Mott-Schottky (*M-S*) (Eq. 3) and the carrier distribution (N_{CV}) (Eq. 4) given by the relation.[20]

$$\left(\frac{1}{C(V)}\right)^2 = \frac{2}{q\varepsilon_0\varepsilon_s N_A(x)}\,(V + V_D) \qquad [3]$$

$$N_{CV} = -\frac{2}{q\varepsilon_0\varepsilon_s}\left[\frac{d}{dV}\left(\frac{1}{C^2}\right)\right]^{-1} \qquad [4]$$

where C - capacitance, ε_0-permittivity of free space, ε_s - dielectric constant of the HP layer, and V_D is diffusion potential.

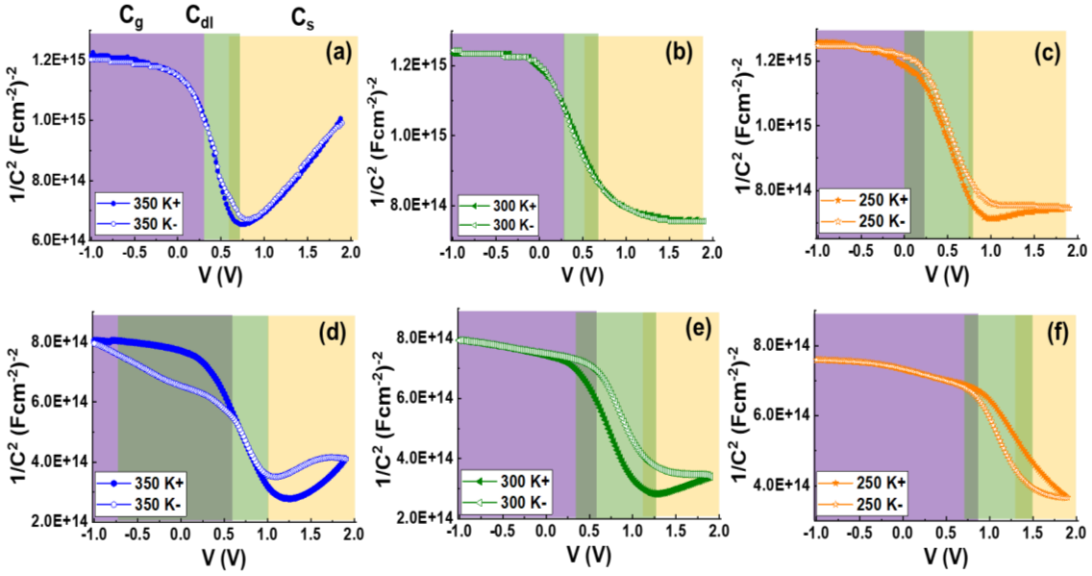

Figure 4. Capacitance spectra. *M-S* plots of fresh (a-c) and aged (d-f) PSCs at different temperatures (350, 300, 250 K), respectively. Here, +/- stands for forward and reverse scans. C_g, C_{dl}, *a*nd C_s represent characteristics capacitance in the device. - geometrical capacitance, Cdl- depletion layer capacitance, and *Cs*- saturation capacitance at the vicinity of diffusion potential and beyond.

Figure 4 depicts the *M-S* plots of fresh and aged devices measured at different temperatures. It is to be noted that capacitance comprises the ionic charge, defect, and free carriers, its hysteresis primarily stems from ionic accumulation, ionic defect, or trap state dynamics.[37,38] Despite a notable difference in the THPC of fresh device, there is comparatively lower capacitance hysteresis in the reverse and forward scan of *C-V* curves (Fig. 4a-c). The *M-S* curves for fresh PSC reveal a low degree of *C-V* hysteresis at room temperature compared to thermal stress. This observation implies the minimal lagging of interfacial ionic motion during *C-V* scans that is attributed to lower interfacial defective surface. On the other hand, *M-S* curves for aged PSC (Fig. 4d-f) demonstrated significantly pronounced capacitance hysteresis under thermal stress. These variations in characteristic capacitance are attributed to the formation of deleterious interfaces in the aged devices that lead to capacitance hysteresis and contribute to photocurrent loss. Similarly, the characteristic capacitances as noted in Mott-Schottky (*M-S*) plots (C_g - geometrical capacitance, C_{dl} - depletion layer capacitance, and C_s - saturation capacitance at the vicinity of diffusion potential and beyond) have negligible variation for the fresh device. While those

for the degraded device are significantly changed under thermal stress. This consolidates that the aged device degrades with interfacial deterioration and the dominance of accumulation of ions at device interfaces as interfacial surface defect resulting in voltage-dependent capacitance driven by thermal drifting.[10] This supports the significant photocurrent loss under the thermal drifting cycle of the aged device.

Furthermore, to evaluate the carrier distribution, we calculated the carrier profile (N_{CV}) using (Eq. 4) from respective *C-V* curves as depicted in Fig. S5. The N_{CV} profile comprises the free charge carriers and defect density.[10] The changes in N_{CV} distribution are be assigned to defect profile in the bulk and interface in fresh and aged PSCs under thermal stress. Although the N_{CV} profile density of degraded PSCs (~9-20 × 10^{15} cm^{-3}) in the bulk is almost in range of the fresh devices (~5-15 × 10^{15} cm^{-3}), the carrier profile widens its distribution which is attributed to the formation of defective interfacial in the aged device. Importantly, the interfacial carrier profile of fresh device (4.6 ~23.8 ×10^{16} cm^{-3}) increased by one order in aged PSC (44.6 ~146.8 ~10^{16} cm^{-3}). One can see almost similar profile density in fresh device while that for the aged device is stark distribution profile. It is attributed to deterioration of interfaces in device with accumulation of deleterious charges or ion migration under light and thermal stress.

These *C-V* analysis results corroborate that the loss in photocurrent under device operation is primarily associated with the worsening of interface quality due to the continuous drifting of mobile ions or photoactive meta defects toward the device interfaces or electrodes. There could be the formation of interfacial defective layers with different carrier trapping and de-trapping characteristics in the aged device.

2.3. Device simulation and degradation mechanism

To explore the degradation mechanism, we analyzed THPC and capacitance results with photophysics, employing device simulation using SCAPS (ver. 3.3.10) [24,39] a solar cell capacitance simulator. The PSC device structure, illustrated in Fig. 5a (with detailed layer and interface structures in Fig. S6, supporting information), and the layer properties (refer to Table S3, supporting information) were adopted from our earlier reports.[8,20,40,41] Recognizing the active generation of multiple defects and interfacial charge accumulation induced by thermal and light stress in PSCs, resulting in interfacial deterioration and the formation of an interface surface defect (ISD) layer, we conducted device simulations considering key optoelectronic properties. These properties include interfacial defect density (N_{ISD}), defect nature (neutral/acceptor/donor), and the characteristic response of each defect, i.e., capture cross-section (CC) for electrons and holes in the ISD layer.

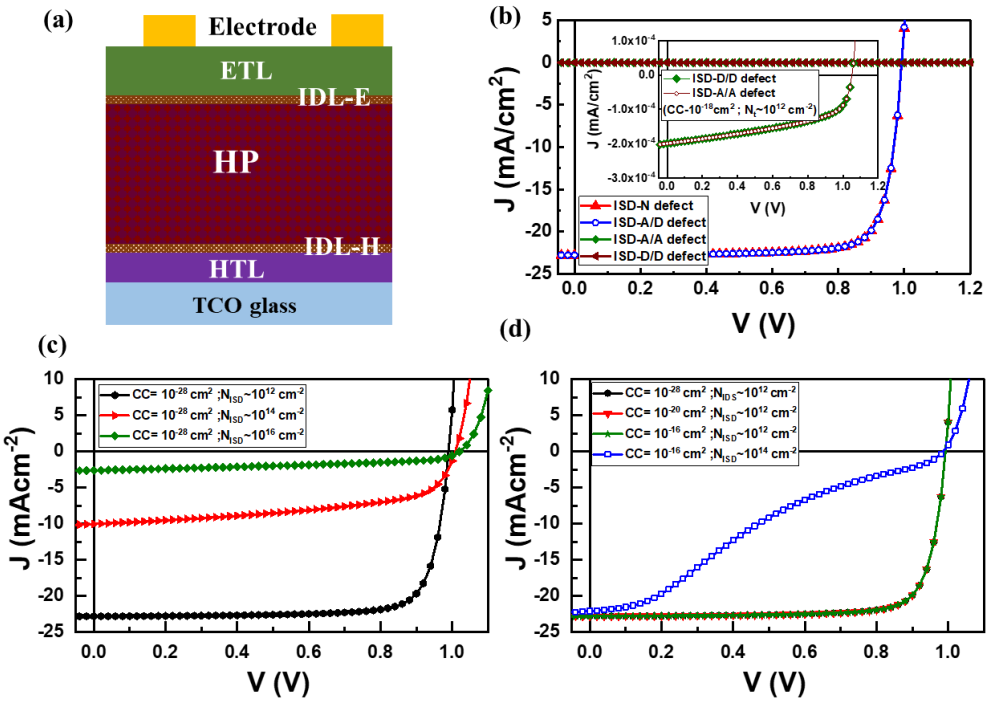

Figure 5. Device simulation results. (a) Schematic of device structure adopted for device simulation. Simulated J-V characteristics account for; (b) different types of defects, (c) activeness of defect- CC of electron and hole, and (d) CC and defect density (N_{ISD}) on the ISD layer. The corresponding device parameters are summarized in Tables S4 and S5.

Our simulation underscores the predominant role of defect characteristics within the ISD layer in PSC for device degradation. Active defects characterized by higher CC value (>10^{-18} cm^2) (Fig. S7) and higher N_{ISD} (Fig. S8) on the IDL (interfacial defect layer) significantly impact device parameters. Furthermore, the CC and N_{ISD} values, along with the nature of defects in the ISD layer, are found to have a significant role in the degradation of device performance. Figure 5b (Table S4) illustrates that neutral (N), acceptor (A) defects on the ISD of HTL side ISD, as well as donor (D) defects on the ETL side ISD, are not detrimental when CC and N_{ISD} are low. However, a notable reduction in photocurrent occurs when D and A defects manifest on the HTL and ETL sides of the ISD, respectively. This observation implies that the formation of a D-type defect on the ISD of HTL and an A-type defect on the ISD of ETL side are prone to the stability of PSCs. This means the formation of a D/A-type defect on the hole/electron collection side could act as a sink for the photogenerated hole/electron carrier transport. This could be a case of completely degraded PSC. Additionally, we explored the simultaneous variation of CC and N_{ISD}. Figure 5c reveals that even if the surface defect induced by charge accumulation is less active (CC= 10^{-28} cm^2), a surface defect-rich IDL layer (with N_{ISD} comparable or higher than HP bulk) could lead to significant photocurrent loss, aligning with our experimental observation. Similarly, with N_{ISD} much lower than the carrier density of the HP bulk, the impact on device parameters is negligible effect even for more active defects with higher CC values (Fig. 5d, Table S5).

Moreover, we also evaluated M-S plots (Fig. S9) from the simulation to see the effect of interfacial deterioration ($N_{t\text{-}ISD}$) and IDL quality (IDL-thickness layer and its mobilities). It reveals that the IDL deterioration accounted with $N_{t\text{-}IDL}$ and thickness (t) predominantly affects the M-S curves (Fig. 5a,b) at the vicinity of saturation capacitance (C_s) and geometrical capacitance (C_g). This means that the IDL layers widen, and defect densities increase with device aging under operation, the voltage-dependent capacitance prevails which is attributed to the accumulation of deleterious ions or thermal sensitive ionic defects. Similarly, as the interfacial layer is more defective, it affects carrier mobility resulting in deterioration in conductivity. The simulated M-S plots (Fig. S9c) show that there is a notable effect on device capacitance. The hindrance in carrier mobility due to interfacial deterioration could be correlated to *C-V* hysteresis and hence in THPC in the device. This could affect carrier injection and loss of photocurrent during device operation. As we compared with the experimental results of the M-S plots, the thermal gradient stress could affect the device with a higher degree of HTL or ETL/HP interface deterioration due to the widening of the defective layer regime by altering the conductivity and carrier dynamics.

Thus, these simulation results partly explain the characteristics of degradation, accounting for the deterioration of device layers and the interface. It suggests that the interface surface defect density and defective thickness are more prone to degradation of PSC. The degradation of the PSC is attributed to the cumulative consequence of both bulk and interface quality deterioration. Therefore, meticulous control of surface defect density and deleterious interfacial formation during device operation under light or heat stress is imperative for enhancing PSC stability.

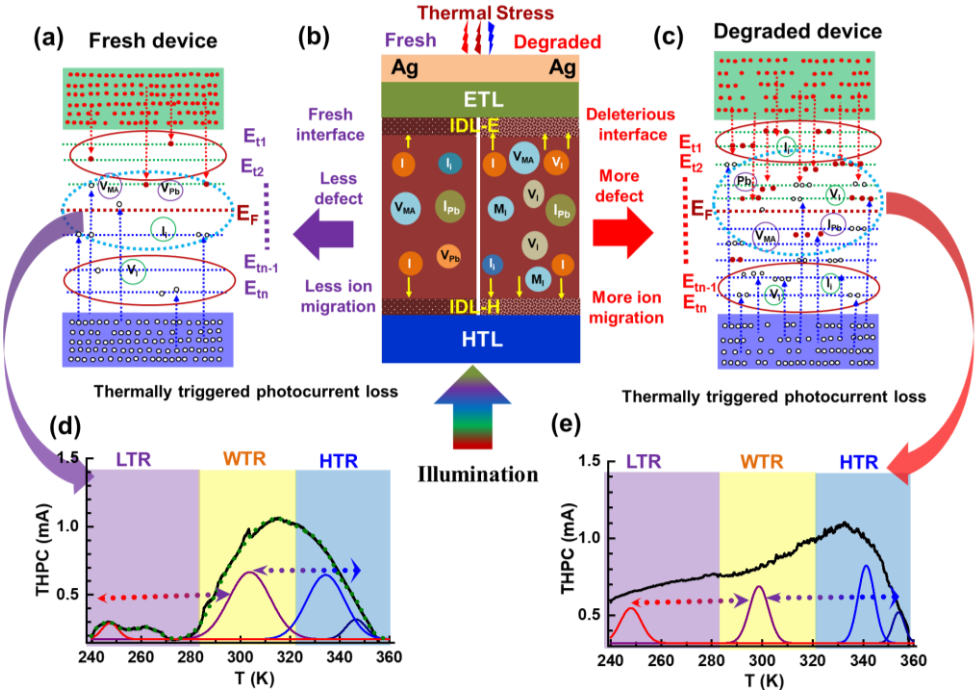

Figure 6. Schematic illustration of the degradation phenomena of the PSCs driven by photocurrent loss: (a, d) fresh, (b) perovskite bulk defect density and interfacial defective layer at interfaces (white line at

center separates the case of the fresh and aged device and yellow arrow at interface indicates the ion migration), and (c, e) degraded PSCs. Here, E_F is the Fermi level in the energy band of perovskite. E_{t1}…. E_{tn} represents the non-radiative recombination states within the perovskite absorber induced in the fresh and degraded device. The fill and unfilled symbols stand for the different types of non-radiative recombination centers in the perovskite layers. The dot arrow lines in (a, c) represent electron and hole capture. The dotted arrows in (d, e) indicate arbitrary multiple peaks fitting of THPC spectra.

In the schematic diagrams (Fig. 6), we propose a mechanism for the device degradation leading to photocurrent loss in PSCs with aging accounting for the THPC spectra and device simulation. It has been documented that the ions migration induces iodine vacancies and other iodine-related defects in perovskite bulk leading to more defective perovskite bulk.[42] Moreover, ion migration could trigger ionic accumulation that accelerates the deterioration of the interfacial quality.[43] During the operational lifespan of PSC, photogenerated carriers are entrapped by thermally activated non-radiative defects, primarily due to thermal drifting. It is supposed to have intrinsic defects (I_i, V_{Pb}, V_I, V_{MA}) [42,44] and ionic migration which is less active in the fresh PSCs (Fig. 6a,b). Hence it is less prone to capturing electrons and holes by non-radiative traps generated under illumination. The aged device degrades with more defects and deteriorates interface due to complex interface chemistries accelerated by ion migration as illustrated in Fig. 6b,c. Simulation results suggest that these defects become spatially active at interfaces, manifesting as interfacial surface defects. As PSCs age, internal dynamics increase, leading to the accumulation of ions at the interfaces, along with the emergence of various point defects. For the aged PSC, the grain distortion and iodine migration are accelerated under light and heat stress.[45] This process results in the formation of detrimental antisite defects within the perovskite bulk or at interfaces. The aging perovskite induces a quasi-continuous distribution of states (Fig. 6c,d) at the interfaces. This broadens the spectrum, facilitating the capture of more photo-generated carriers within the perovskite bulk, ultimately causing a decline in photocurrent and a subsequent drop in device efficiency.

These findings underscore the critical need for enhancing the inherent resilience of the perovskite layer to counter ion migration and stress-induced formation of defects at the interface surface. While progress has been made in achieving stability milestones by manipulating the bulk or interface quality of the perovskite layer through the incorporation of various functional additives,[19,46–49] there remains considerable potential for further advancements. It is essential to focus on passivating intrinsic defect formation and preventing the deterioration of interfacial surfaces in PSCs during ambient operation.

3. Conclusions

We have investigated the degradation of PSC by THPC analysis and device simulation. This work delves into the deterioration of PSC by probing THPC and thermally active ionic dynamics. THPC

response reveals alterations influenced by interfacial ionic or charge accumulation and complex energy level landscape assigned to multiple defects. The capacitance analysis demonstrates the thermally triggered charge accumulation is more pronounced in aged PSC. This plays a detrimental role in the loss of photo-current in the degraded PSC. These degradation phenomena were further examined by device simulation taking into account the interface surface defective layer and its associated defect characteristics. This work highlights a direct link between PSC device degradation and thermally activated traps induced due to the intrinsic instability of the perovskite layer and interfacial deterioration. This report underlines the importance of passivating defects in perovskite through material engineering and enhancing defect-resistive interfaces via carrier transport engineering to improve the operational stability of PSCs.

Supporting Information

The Supporting Information is available on the website. Experimental details, Theoretical models, equations, device simulation models, and device simulation results.

Conflicts of interest

There are no conflicts to declare.

Acknowledgments

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