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High-power-density hybrid planar-type silicon thermoelectric generator with phononic nanostructures

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ABSTRACT

Energy harvesting is essential for the internet-of-things networks where a tremendous number of sensors require power. Thermoelectric generators (TEGs), especially those based on silicon (Si), are a promising source of clean and sustainable energy for these sensors. Although large thermoelectric figure of merit has been reported for nanostructured Si material, however, nanostructuring has not been effectively used in device applications, and the reported performance of hybrid planar-type Si TEGs never exceeded normalized powers of $\mathbf{0.1\ \mu W cm^{-2} K^{-2}}$ due to the poor thermoelectric performance of Si and the suboptimal design of the devices. Here, we report a hybrid planar-type Si TEG with a normalized power of $\mathbf{1.3\ \mu W cm^{-2} K^{-2}}$ around room temperature. The increase in thermoelectric performance of Si by nanostructuring based on the phonon-glass electron-crystal concept and optimized three-dimensional heat-guiding structures resulted in a record-high power density. The improvement of power generation by a factor of 10 makes the once-a-day sensing applications realistic in a practical environment for the first time. In-field testing demonstrated that our Si TEG functions as a sufficient energy harvester. This demonstration paves the way for energy harvesting with a low-environmental load and cost-effective material with high throughput, a necessary condition for energy-autonomous sensor nodes for the trillion sensors universe.

1. Introduction

Improvements in computing speed and low power consumption of electronic components have led to the use of numerous sensors around us, enriching human life. In the internet of things society, where smart devices are connected through networks, energy-autonomous sensors are essential elements. Energy harvesting technology uses ambient energy sources such as mechanical vibration, heat, friction, and light [1] [–] [3]. These technologies can also contribute to carbon neutrality by leveraging their respective strengths. Thermoelectric (TE) conversion, one of the most promising energy harvesting technologies, generates electricity from thermal gradients [4,5]. Thermoelectric generators (TEGs) are known for their robustness because they are all solid-state devices with no moving parts. Since heat sources exist in various locations, sensor nodes with TE harvesters are practical if their power generation is sufficient.

The figure of merit ZT of TE materials is expressed by the Seebeck coefficient S, electrical conductivity σ, thermal conductivity κ, and temperature T as $ZT = S^2 \sigma T/\kappa$. High values of $ZT > 1$ have been reported for Bi, Te, Sb, and Pb compounds [6] [–] [10]. The compound Bi_2Te_3 is widely used in practical applications [11] [–] [13]. In some complex compounds of heavy metals, high Seebeck coefficients due to the large effective mass of electrons and low thermal conductivities due to phonon scattering have resulted in high ZT values. For energy

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harvesting applications, it is further advantageous that the materials are readily available, inexpensive, have a low environmental impact, and can be supplied in large quantities [14,15].

Silicon (Si) is the most widely used material in electronics and meets the above conditions [16,17]. However due to its high thermal conductivity $\kappa > 130\ \mathrm{Wm^{-1}K^{-1}}$, its ZT value is as low as 0.001 in bulk material at room temperature [18]. Therefore, it has been considered unsuitable as a TE material. However, researchers have reduced the thermal conductivity by using nanostructures [19,20], and achieved $ZT > 0.1$ at room temperature, such as 0.6 in nanowires (NWs) [21,22], 0.4 in porous thin-films [23], 0.3 in and 0.2 in alloys with germanium [24,25]. While improvements in material performance have been reported, there have not been as many studies on planar device structures fabricated on Si wafers, which is necessary to move to a practical stage using mass-producible Si technology.

Planar-type TEGs fabricated on Si wafers can be vertical or hybrid, depending on the orientation of the TE material [26,27]. Vertical devices can utilize the large heat flux to obtain high power densities, with reported normalized powers of $29\ \mu\mathrm{Wcm^{-2}K^{-2}}$ using Si and $84\ \mu\mathrm{Wcm^{-2}K^{-2}}$ using SiGe material [28,29]. In the hybrid type, TEGs generate power by extracting the temperature difference ΔT_{TE} in the in-plane direction of the TE material from the temperature difference ΔT in the out-of-plane direction of the wafer. In thin-film thermoelectric materials, the ratio of cross-sectional area to heat flux is small compared to the device's footprint area, enabling efficient power generation even when heat flux through the device is limited. The performance of planar-type TEG is evaluated by the area density of power generation per temperature difference (the normalized power of the device in a unit of $\mathrm{Wm^{-2}K^{-2}}$). Applying a ΔT_{TE} with an efficiency ratio $\eta_{\Delta T} = \Delta T_{TE}/\Delta T$ is essential in forming a suspension bridge structure. ΔT_{TE} can be increased by making the bridges longer and the material thinner. However, there is a trade-off in that the internal electrical resistance of the device increases, and an optimization of the device structure, both thermal and electrical, is required. In previous reports, there was a limit to the performance improvement by optimizing the dimensions of the poly-Si film, and the normalized power of the hybrid device has been limited to about $0.1\ \mu\mathrm{Wcm^{-2}K^{-2}}$ due to the significant electrical resistance of poly-Si film with few hundreds nanometer of film thickness [26,27,30–32]. There are reports of about $0.25\ \mu\mathrm{Wcm^{-2}K^{-2}}$ in devices using SiGe instead of poly-Si [33,34], and $0.3\ \mu\mathrm{Wcm^{-2}K^{-2}}$ in devices using bundles of Si NWs as bridges [35]. However, material cost and compatibility with wafer processes have been an issue.

This study demonstrates a hybrid planar-type Si TEG that achieves the normalized power of $1.3\ \mu\mathrm{Wcm^{-2}K^{-2}}$ using poly-Si thin films as the TE material. This is more than ten times higher power density than previously reported achieved by enhancing the thermoelectric performance through the fabrication of phononic nanostructures in the thermoelectric material and a structural design that optimizes electrical and thermal resistance. In particular, the three-dimensional structure for directing the heat flow from the cross-plane to the in-plane direction enables $\eta_{\Delta T} \geq 30\%$, contributing significantly to performance improvement. We then demonstrate that our Si TEG produces an

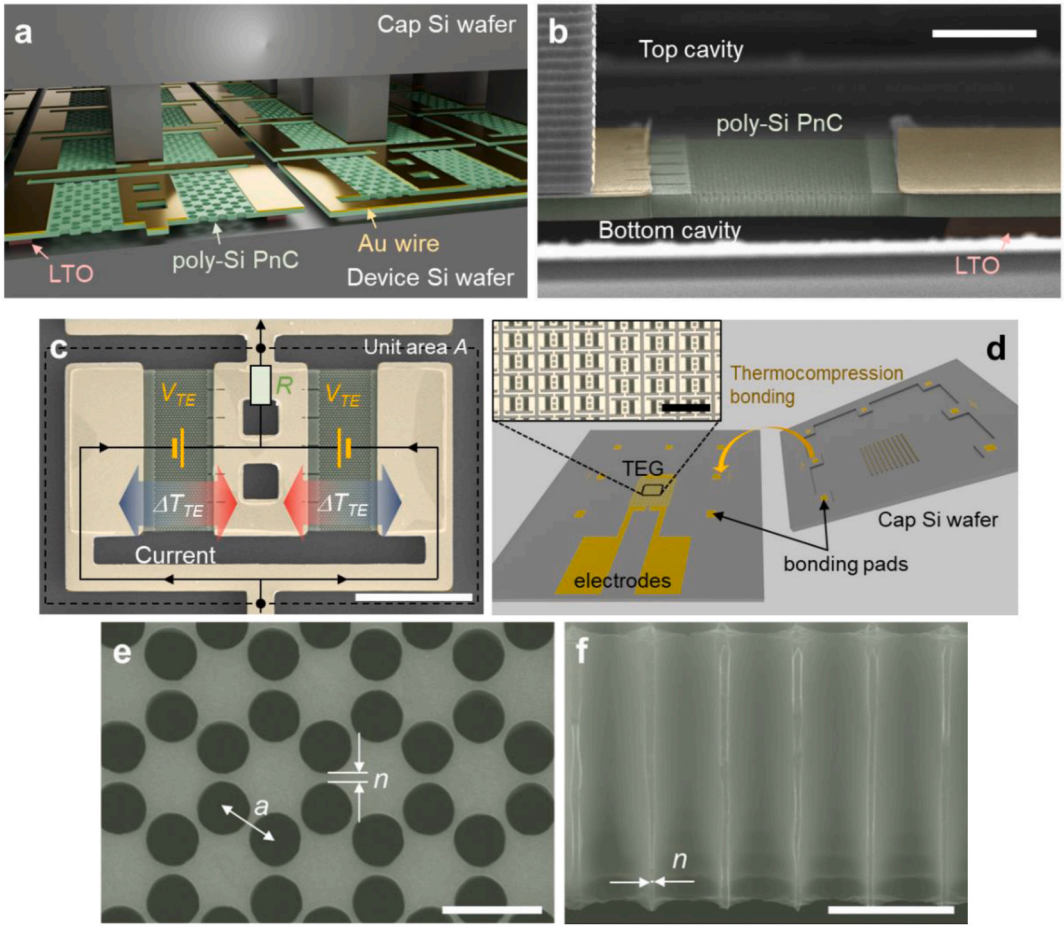

Fig. 1. Planar-type nano phononic Si thermoelectric generator. (a) Schematic 3D picture of TEGs composed of a device and cap wafer. (b) Side-view SEM images of TEG after cap wafer bonding. Scale bar, 5 μm. (c) SEM image of a unit cell of TEG. Scale bar, 20 μm. (d) Schematic 3D picture of fabricated device and cap wafers before bonding. The inset shows an optical microscope image of connected TEG cells. Scale bar, 100 μm. (e,f) SEM images of PnC nanostructures from the top and side view. Scale bars, 500 nm.

average power of 100 μW in an in-field measurement over four days.

2. Experimental design

In a hybrid planar-type TEG, the TE material parts that generate electricity have a thin film shape in the in-plane direction, with a double-cavity structure above and below the thin film (Fig. 1a and b). This structure allows the thermoelectric thin film to be suspended in mid-air to achieve a large temperature difference in the in-plane direction, thereby increasing the power generation density. Fig. 1c shows a scanning electron microscope (SEM) image of a unit cell of TEG with an electric circuit when a temperature difference ΔT_{TE} is induced in the thin film. The design of unileg modules is unique in that, unlike typical π-type modules, it uses only n-type materials, resulting in low electrical resistance and simplifying the fabrication process. The performance of the TEG is evaluated by the power density P, expressed by the TE voltage V_{TE}, electrical resistance R, and device area A as $P = {V_{TE}}^2/(4RA)$. Ideally, the power density does not depend on the number of devices integrated. However, the design of the TEG should not be based on the device alone but rather on the configuration of the number of devices in series and in parallels, which are optimized by considering the circuit design of the energy harvesting module. Therefore, based on an optimization calculation for 2400 units, we fabricated the device as a parallel arrangement of 20 lines, each with 120 units in series (Fig. 1d). The details of the fabrication and structure of the TEG are given in the Supplementary material.

In this study, two essential factors enabled the enormous increase achieved in power density: the enhancement of ZT and efficiency by nanostructuring and the three-dimensional heat flow control of the device. Poly-Si thin film thermoelectric materials have nanostructures based on phonon engineering for ZT enhancement. The phononic crystal (PnC) nanostructure is designed considering the mean free path of charge and heat carriers, known as the concept of PGEC (phonon-glass electron-crystal) proposed by Slack in 1995 [36]. In this structure, the phonon transport is significantly reduced while the electron transport is minimally disturbed. In porous structures, such as PnCs, the distance between the sidewalls of the pores (neck size n) is an essential structural parameter (Fig. 1e). The film thickness is also a critical structural parameter in hybrid planar-type TEG. If the film is too thick, the temperature difference will not be achieved, resulting in low power density, while nanofabrication will be difficult. On the other hand, if it is too thin, the electrical resistance becomes too high, and furthermore the mechanical strength, which is essential for practical use, cannot be ensured. In this study, we have formed PnC nanostructures with circular through-holes in a 1.1-μm-thick poly-Si film with a periodicity of 300 nm in a honeycomb lattice. The neck sizes range from 8 nm to 116 nm (e.g., Fig. 1f shows a PnC with $n = 8$ nm). Taking mechanical strength into consideration, PnC nanostructures are fabricated on silicon films that are more than three times thicker than conventional films and the dependence of thermal conductivity, electrical conductivity, and power generation were investigated.

The other important factor, the heat flow control in the device, is the optimization of the structural parameters in the thin film and the optimization of the structure perpendicular to the thin film. The former was optimized using the finite element method with the thermal and electrical parameters of the material and boundary resistances obtained by our measurements or database [37] (Supplementary material). Here, we describe a double-cavity structure that increases the power density by applying as large a temperature difference as possible to the thermoelectric material. In addition, we have developed a fabrication technique for heat-guiding structures by cap wafer bonding. Creating a heat flow path from the hot to the cold side through solid-solid interfaces is essential. The power generation efficiency at a given temperature difference can be calculated as the ratio of the total thermal resistance along the temperature gradient path to the thermal resistance of the thin film thermoelectric material. The three-dimensional heat-guiding structure reduces the total thermal resistance, while the nanostructures increase the thermal resistance of the thin film, resulting in high efficiency.

3. Results and discussion

3.1. Nanostructured polycrystalline Si TE material

Although various structural parameters can be approximately optimized by the finite element method, the dynamics of charge and heat carriers in nanostructures below 100 nm and systems with strong surface scattering are not straightforward. Therefore, it is necessary to experimentally investigate the structures that maximize the power density, starting from those found in simulations under conditions where mechanical stability is ensured. We have performed thermal and electrical conductivity measurements on several n-type nanostructured poly-Si films with different neck sizes to evaluate ZT (Supplementary material). We first measured the carrier concentration, Seebeck coefficient, and electrical conductivity of the poly-Si film before nanostructuring. We found that the carrier concentration was 2.2×10^{20} cm^{-3}, the Seebeck coefficient was $-100\,\mu$VK^{-1}, the electrical conductivity was 166 kSm^{-1} and the material power factor was 1.66 mWm^{-1}K^{-2}. Fig. 2a shows the measured thermal conductivity as a function of the neck size. The dashed line shows the thermal conductivity of the film with no nanostructure (31 Wm^{-1}K^{-1}). It is reduced to less than a quarter of that of single-crystal bulk Si due to the surface scattering in a thin film and polycrystalline grain boundary scattering. As the neck size decreases, the thermal conductivity decreases, with a thermal conductivity of 9 Wm^{-1}K^{-1} for a sample with a neck width of 36 nm. Surface phonon scattering reduces the thermal conductivity of the material, for practical thermal design, the effective thermal conductivity of the porous film is reduced to 4 Wm^{-1}K^{-1} by taking porosity into account. We fabricated structures with a neck size n of about 8 nm or less and obtained further reduced thermal conductivities, but the mechanical strength was insufficient for device fabrication. Thermal phonons are the main heat carriers in this sample, and phonon scattering is the sum of boundary scattering, Umklapp scattering, and impurity scattering as described by the Matthiessen rule. At around room temperature, the Umklapp scattering has a larger influence on the bulk material, while the boundary scattering becomes larger and dominant in the nanostructures. We also note that coherent phonon scattering is negligible in our phononic nanostructures at room temperature. Unless the periodic structure is a few nanometers, it is only observed at very low temperatures [38,39].

Fig. 2b shows the electrical conductivity versus the neck width of the PnC nanostructures. The electrical conductivity is also reduced, more strongly than expected, by fabricating the circular holes, especially in the neck size below 60 nm. Hall measurement result shows 17 % reduction in electron mobility and 25 % reduction in carrier concentration for nanostructured poly-Si membrane with the neck size of 44 nm. Possible reasons for the reduction in electrical conductivity include a reduction in mobility due to electron scattering at the neck and a decrease in carrier concentration due to a decrease in effective neck size caused by surface oxidation. In line with the PGEC concept, the fabrication of PnC nanostructures, although smaller than expected results in a larger σ/κ ratio. However, there is room to further increase the ZT by analyzing and improving the surface conditions. A plot of the ZT versus neck width is shown in Fig. 2c. In highly doped silicon, the MFP of the electrons is about 1–10 nm and the power factor is not affected even in nanowires and porous membranes, we assumed that the Seebeck coefficient is constant regardless of the nanostructure size [22,23]. Nanostructured poly-Si shows a ZT of 2.0×10^{-2} at 300 K, which is 20 times better than bulk Si. Fig. 2d shows the grain size distribution estimated by the transmission electron microscope (TEM) observation. The grain size of poly-Si is dominated by sizes around 50–100 nm, and some grain

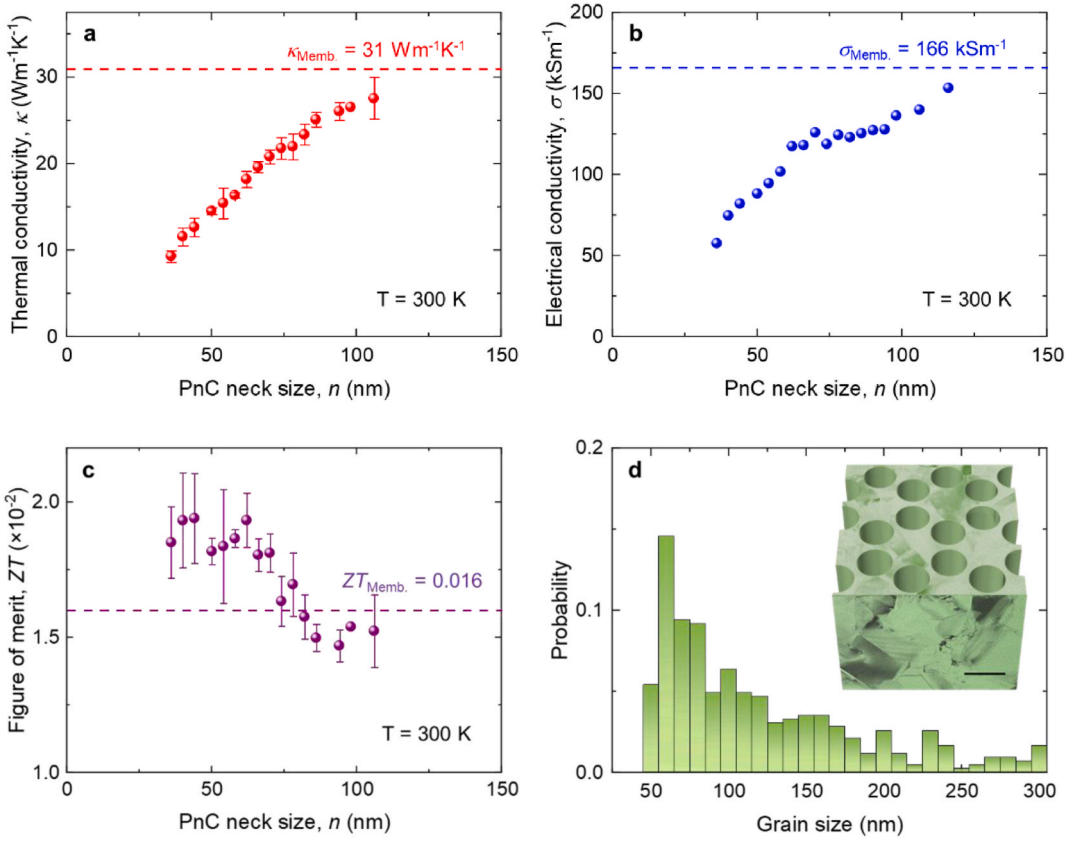

Fig. 2. (a–c) Measured thermoelectric properties of the nanostructured poly-Si membrane as a function of PnC neck size: thermal conductivity (a), electrical conductivity (b), and thermoelectric figure of merit (c). (d) Histogram of the grain size measured by surface and cross-sectional TEM observations. The inset shows two TEM images overlaid with a PnC pattern. Scale bar, 300 nm.

boundaries are in the necks causing the reduction of σ too. Making the smaller PnCs in the poly-Si with larger grain size might improve σ/κ more efficiently [40,41] (Supplementary material).

3.2. Characterization of planar-type Si TEG

We evaluated the performance of the fabricated 120 series × 20 parallel TEG at room temperature. The details of the measurement setup are described in the Supplementary material. The area of the 2400 units is 0.077 cm^2, including the wiring between the units. The internal electrical resistance of the TEG was 38.8 Ω, designed to be less than 50 Ω for a boost circuit in the latter stage of the energy harvesting module. Next, the TEG voltage was measured when an external temperature difference ΔT was applied: an open circuit voltage of 3.9 mV was measured at ΔT = 1 K, yielding a voltage factor of 50.6 mVcm^{-2}K^{-1} (Fig. 3a). The TEG voltage is proportional to the applied temperature difference in the range of about 15 K near room temperature. This fact indicates that the temperature dependence of the physical properties is negligible in this range. The estimated ratio $\eta_{\Delta T} = \Delta T_{TE}/\Delta T$ is as high as 32.4 %, a 160-fold improvement from 0.2 % in our previous TEG without a cap wafer [42]. While the total heat flow path length is 1 mm, consisting mainly of the Si substrate and a cap wafer (525 μm-thick,

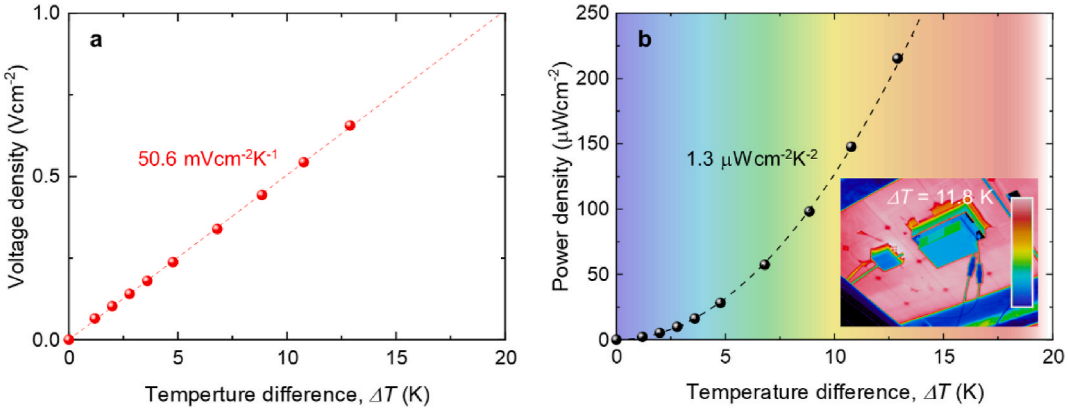

Fig. 3. Output voltage (a) and power density (b) of TEG as a function of applied temperature difference ΔT. The inset shows an IR camera image of the temperature map around the TEG module. Color bar, from 20 to 40 °C. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

respectively), the PnC poly-Si with a length of only 9 μm concentrates a temperature difference of up to 32 %. The fact that the amount of power generated is proportional to the square of ΔT_{TE} shows that our double-cavity structure is highly effective in increasing the power density.

From the measured TEG voltage and the internal electrical resistance, we evaluated the power density P, which is proportional to the square of the temperature difference ΔT, and obtained a normalized power of the TEG of 1.3 μWcm^{-2}K^{-2} (Fig. 3b). To our knowledge, this is the highest performance for a hybrid planar-type Si thermoelectric device. A power generation density of 100 μWcm^{-2} can be obtained from a temperature difference of less than 10 K, which is common in the everyday environment. In the inset of Fig. 3b, we show the IR camera image to characterize the ΔT in the environment. We fixed the test case body with planar-type TEG and Al heat-sink on the backside of the solar cell panel and observed $\Delta T = 11.8$ K while the panel was irradiated by the sun. Although some ΔT is lost at the interfaces between the TEG and the heat-sink, we expect the TE energy harvester to be applicable.

3.3. Benchmark of hybrid planar-type Si TEG for energy harvesting

To clarify the characteristics and performance of our device, we will discuss it in comparison with previously reported devices in the past two decades in terms of device power density (Fig. 4). Due to the practical superiority of Si, TEGs based on poly-Si films have been studied to improve the power density and to develop fabrication methods. Recently, a normalized power of 0.1 μWcm^{-2}K^{-2} has been reported for devices fabricated using only processes compatible with the BiCMOS process [32]. There have also been reports of devices based on single-crystalline Si NWs, with a normalized power of 0.5 μWcm^{-2}K^{-2} using short NWs of less than 1 μm in length on the SiO_2 layer [43]. To increase the power density by utilizing large ΔT, making a bridge structure with bottom and top cavities is essential. Using bundles of Si or SiGe NWs, devices have been reported with a normalized power of about 0.3 μWcm^{-2}K^{-2} [35]. Devices using poly-SiGe films, which have a higher bulk performance than Si, have also been reported at 0.25 μWcm^{-2}K^{-2} due to their low thermal conductivity. However, the high material cost of germanium and the low performance of n-type films have remained challenging.

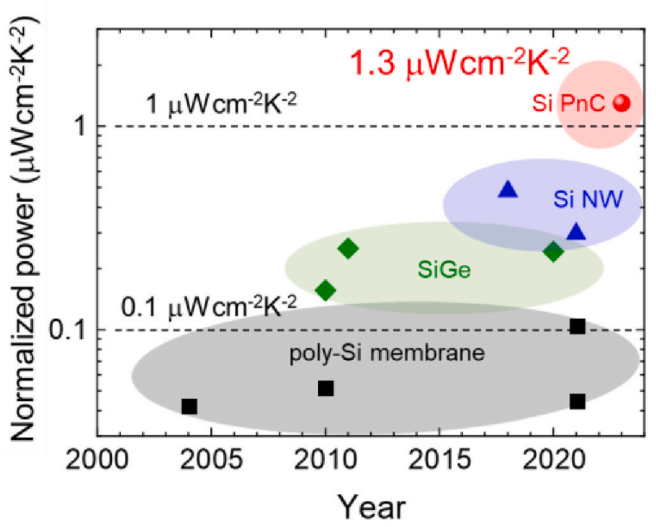

Fig. 4. Comparison of TEG normalized powers among hybrid planar-type Si devices reported in the last decades. Colors represent the different material groups. Black, poly-Si membrane [32,44] [–] [46]; green, SiGe [33,34,47]; blue, Si NW [35,43]; red Si PnC (this work). (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

Generally, both n- and p-type materials are used in TEGs. In contrast, our TEG is an uni-leg type, so the fabrication process is simplified and less costly. In addition, n-type material has relatively higher electrical conductivity and lower contact resistance to metals than p-type material, which reduces electrical resistance for better circuit compatibility. Furthermore, optimization of the through-hole with a small neck size and three-dimensional heat-guiding structures enabled a normalized power of 1.3 μWcm^{-2}K^{-2}, which is more than ten times higher than similar poly-Si films. Finite element simulations show that 30 % improvement of output power is obtained for devices with fabricated nanostructures (Supplementary material), and an overall performance improvement of more than 10 times is achieved by the combination of nanostructures, 3-dimensional heat-guiding structures and unileg design optimization. The presence of unexpected reduction in electrical conductivity in the nanostructures implies that further optimization is possible to enhance device performance.

3.4. In-field characterization of energy harvest module

Considering the application of TEG to wireless sensing systems, a simple sensor with low data volume and low-power communication consumes about 5 J for one sensing and data transmission in the case of Bluetooth Low Energy (BLE), which can communicate over several hundred meters. We performed in-field measurements to demonstrate power generation over a long period by an actual ΔT in the environment. The solar cell panel was used for the power generation measurement. As shown in Fig. 5a and b, two thermocouples and a Si TEG module were installed on the backside of the solar panel. The two thermocouples measure the temperature difference ΔT between the surface of the panel and the atmosphere 5 cm away from the panel, as shown in Fig. 5c. The output voltage of the TEG was also measured. Careful thermal design of the module is essential for an efficient thermoelectric power generation. A plastic resin ($\kappa \sim 0.18$ Wm^{-1}K^{-1}) was used for the case body for better thermal isolation, and two Al blocks and an Al heat sink were used for efficient heat dissipation on the cold side [48]. The transition of ΔT was recorded over four consecutive days, as shown in Fig. 5d, and the TEG voltage, which is proportional to ΔT was also recorded. Fig. 5e shows the calculated accumulated energy assuming the device normalized power of 1.3 μWcm^{-2}K^{-2} and an enlarged area of 10 cm^2. The details of the calculation are given in the Methods section. As expected, the amount of generated power depends on the weather. Interestingly, a negative value of ΔT is observed by radiative cooling. Therefore, we have a chance to harvest more energy by installing an inverter if the energy loss is less than the harvested power at night. The average generated power is 98 μW (721 μW at the peak in a sunny day), and the total energy generated is about 34 J within four days. A single measurement and data transmission via BLE requires about 5 J and 70 J for small data (temperature, humidity, etc.) and large data (10 KB image), respectively. Therefore, data can be collected about twice a day for the former application and 14 times per month for the latter. This in-field measurement shows that Si TEGs have reached a level where they can be used as a power source for self-powered sensing systems.

4. Conclusions

We demonstrate a hybrid planar-type poly-Si TEG with a normalized power of 1.3 μWcm^{-2}K^{-2}. According to the PGEC concept, the material performance was enhanced by forming through-holes with neck sizes of 8–100 nm in a 1.1-μm-thick poly-Si film. In addition, a three-dimensional heat-guiding structure fabricated by bonding the Si cap wafer increases $\eta_{\Delta T}$, and results in high power generation. The device performs ten times better than conventional hybrid planar-type Si TEGs and generates more than 100 μWcm^{-2}. The four days of in-field power generation demonstrated that the TEG generates an average of close to

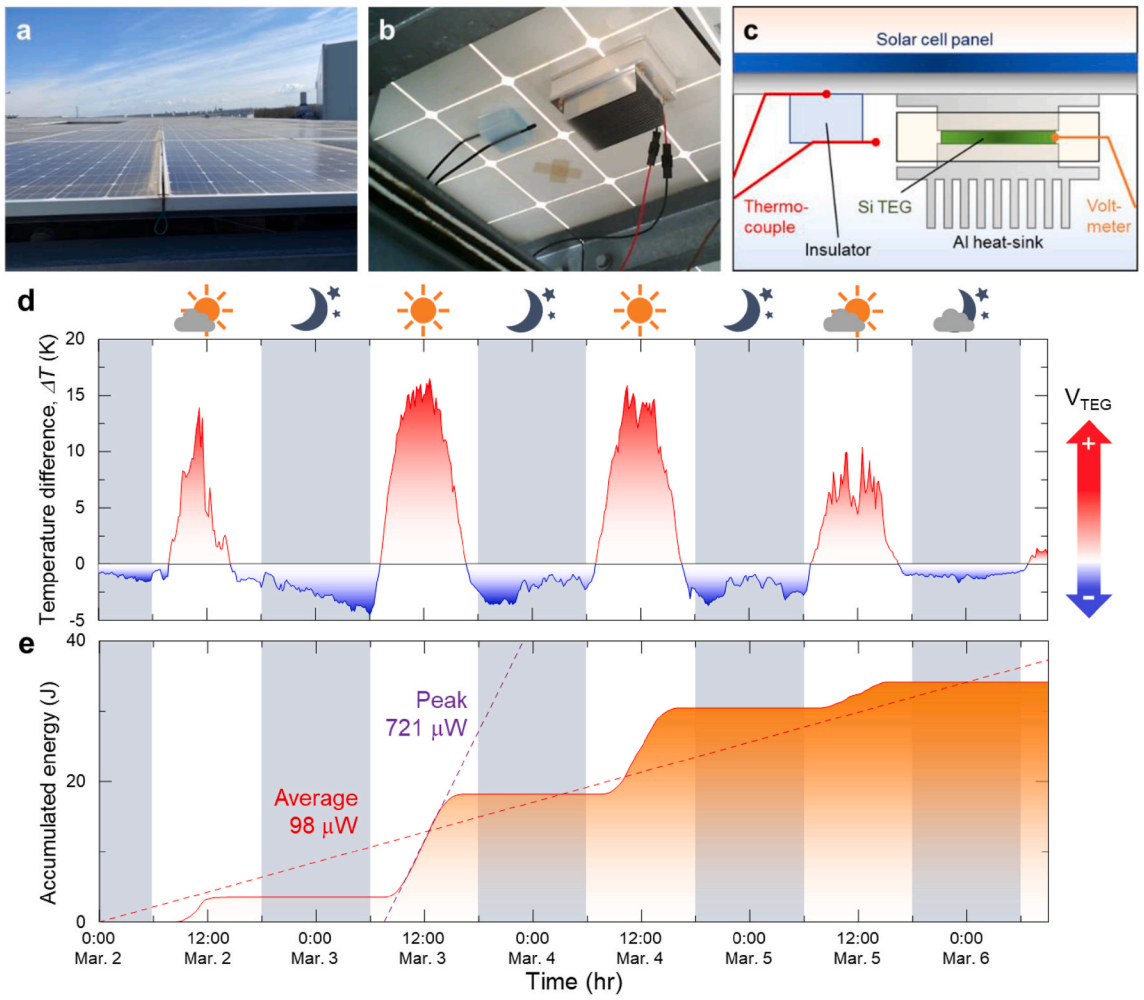

Fig. 5. (a,b) Solar cell panels used in the experiment on the front side (a) and the back side with the measurement systems for environmental temperature and TEG voltage (b). (c) Schematic of the measurement system. (d,e) Measured temperature difference between the backside surface of solar cell panel and air (d) and estimated accumulated energy (e) over four continuous days in Ibaraki, Japan (35°54′40"N, 140°3′15"E, from 2 to March 6, 2023).

100 μW (0.72 mW at the peak) and can be used as an energy-autonomous sensing system even at small temperature differences, such as those obtained from a near-room-temperature environment. The Si device is an uni-leg type that can be mass-produced at a low cost due to its greatly simplified process, which is advantageous for its widespread use. This work can contribute to accelerate the realization of the internet of things society, which requires an enormous number of sensors.

CRediT authorship contribution statement

Ryoto Yanagisawa: Writing – review & editing, Writing – original draft, Visualization, Validation, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Sota Koike:** Writing – review & editing, Methodology, Data curation. **Tomoki Nawae:** Writing – review & editing, Methodology, Data curation. **Naohito Tsujii:** Writing – review & editing, Methodology, Data curation. **Yanan Wang:** Writing – review & editing, Methodology, Data curation. **Takao Mori:** Writing – review & editing, Validation, Supervision. **Patrick Ruther:** Writing – review & editing, Resources, Methodology. **Oliver Paul:** Writing – review & editing, Supervision, Resources. **Yoshifumi Yoshida:** Writing – review & editing, Resources. **Junichi Harashima:** Writing – review & editing, Resources. **Takashi Kinumura:** Writing – review & editing, Resources. **Yuta Inada:** Writing – review & editing, Resources. **Masahiro Nomura:** Writing – review & editing, Writing – original draft, Validation, Supervision, Resources, Project administration, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mtphys.2024.101452.

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