Hydrogen-Terminated Diamond MOS Capacitors, MOSFETs, and MOSFET Logic Circuits

Jiangwei Liu[1, a)] and Yasuo Koide[1]

[1]Next-generation Semiconductor Group, Research Center for Electronic and Optical Materials, National Institute for Materials Science, 1-1 Namiki, Tsukuba, Ibaraki 305-0044, Japan
[a)]Electronic mail:liu.jiangwei@nims.go.jp

Abstract. Wide-bandgap semiconductor diamond has been studied to develop high-power, high-frequency, and high-temperature electronic devices. However, their development has been limited by the low free carrier density that occurs in diamond at room temperature because of the high activation energies of *p*-type boron and *n*-type phosphorus dopants. Fortunately, hydrogen-terminated diamond (H-diamond) can accumulate two-dimensional hole gases on its surface with a high free carrier density. In this chapter, we review our recent progress in the fabrication of H-diamond metal-oxide-semiconductor (MOS) capacitors, MOS field-effect transistors (MOSFETs), and MOSFET logic circuits. Specifically, the leakage current densities for different oxide insulators on H-diamond and the capacitance-voltage properties for the Al_2O_3/H-diamond MOS capacitors are discussed. Planar-type, T-type, and triple-gate fin-type H-diamond MOSFETs are reviewed, and the fabrication and performance of depletion- and enhancement-mode H-diamond MOSFETs and logic circuits are summarized.

Keywords: Diamond, MOS capacitors, MOSFETs, Logic Circuits.

1. Introduction

Semiconductor diamond has long been studied for applications in high-power, high-frequency, and high-temperature electronic devices because it exhibits a wide bandgap, high breakdown field, high carrier mobility, and high thermal conductivity [1, 2]. However, the development of diamond electronic devices has been limited by the low free carrier density that occurs in diamond at room temperature because of the high activation energies of the boron acceptor (370 meV) and phosphorus donor (570 meV) [3]. Fortunately, hydrogen-terminated diamond (H-diamond) can accumulate two-dimensional hole gases on its surface with a sheet hole density of 10^{12}–10^{13} cm^{-2}. Notably, after the H-diamond is exposed to NO_2 or $NH_3 + H_2$, the hole density can increase to as high as 10^{14} cm^{-2} [4, 5]. H-diamond is therefore considered to be a promising channel layer for fabricating high-performance diamond electronic devices such as metal-oxide-semiconductor (MOS) capacitors [6-9], MOS field-effect transistors (MOSFETs) [10-21], and MOSFET logic circuits [21-23].

Recently, the electrical properties of H-diamond-based MOSFETs have been significantly improved. Owing to the increase in hole density after treating the H-diamond surface with NO_2 gas, the maximum drain current ($I_{D,max}$) of the H-diamond-based MOSFET can be enhanced up to 1.35 A mm^{-1} [10]. The output power density of Al_2O_3/H-diamond-based MOSFET is approximately 3.8 W mm^{-1} [11]. The maxi-

mum cut-off frequency and maximum extrinsic transconductance ($g_{m,max}$) are also reported to be as large as 70 GHz and 206 mS mm^{-1}, respectively [12]. H-diamond MOSFETs can also operate well after annealing at a high temperature of 500 °C [13] and at a high breakdown voltage of 3326 V [14]. Furthermore, enhancement-mode H-diamond MOSFETs [6, 16, 20] and MOSFET logic circuits [21-23] have also been achieved. H-diamond-based MOSFETs are believed to be comparable to devices using other wide-bandgap semiconductors.

In this chapter, we review our recent progress in the fabrication of H-diamond MOS capacitors, MOSFETs, and MOSFET logic circuits. Specifically, the leakage current density (*J*) for different oxide insulators on H-diamond and the capacitance-voltage (*C-V*) properties for the Al_2O_3/H-diamond MOS capacitors are discussed. The fabrication processes and electrical properties for the planar-type, T-type, and triple-gate fin-type H-diamond MOSFETs are reviewed. Additionally, the depletion- and enhancement-mode H-diamond MOSFETs are summarized, and logic circuits composed of enhancement- and depletion-mode MOSFETs are demonstrated. Notably, other excellent works for vertical-type H-diamond MOSFETs [24], inversion channel diamond MOSFETs [25, 26], and boron-doped oxygen-terminated diamond MOSFETs [27, 28] are not included in this chapter.

2. H-diamond MOS capacitors

2.1 Fabrication process for H-diamond MOS capacitors

Figure 1 shows the fabrication process for the H-diamond MOS capacitors. A single crystalline diamond (001) substrate with dimensions of 3.0 × 3.0 × 1.0 mm is cleaned in a mixed acid solution of H_2SO_4 + HNO_3 for 3 hours at 300 °C [Fig. 1(a)]. Before growing the H-diamond epitaxial layer using a microwave plasma-assisted chemical vapor deposition (MPCVD) system (AX5200S, Seki Technotron Corp., Tokyo, Japan) [Fig. 1(b)], the diamond substrate is treated in the chamber at 1000 °C for 20 min to clean off surface contamination. The growth temperature, time, and chamber pressure for the H-diamond epitaxial layer are 900–940 °C, 1.5–2.0 hours, and 80 Torr, respectively. The H_2 and CH_4 flow rates are 500 and 0.5 sccm, respectively. Thicknesses of the H-diamond epitaxial layers are in the range of 150–200 nm. After growing the H-diamond by MPCVD, two different routes are used for the fabrication of H-diamond MOS capacitors. The choice of the fabrication route is based on the deposition temperatures of the oxide insulators. For fabricating the H-diamond MOS electronic devices, LOR 5A and AZ 5214E photoresists are used. Because the temperature limitation for the photoresist (AZ 5214E) is 140 °C, when the deposition temperature for the oxide insulator is lower than this temperature, the photoresists can be used as the mask to form the gate oxide and metal contacts first [Fig. 1(c)-1]. When the deposition temperature for the oxide insulator is higher than 140 °C, the Ohmic contacts are formed first [Fig. 1(c)-2], and then the oxide insulator is deposited to cover the entire surface of the sample.

For the fabrication route with the gate oxide and metal contacts deposited first, a maskless laser lithography system (DL-1000, Nanosystem Solutions, Inc., Tokyo,

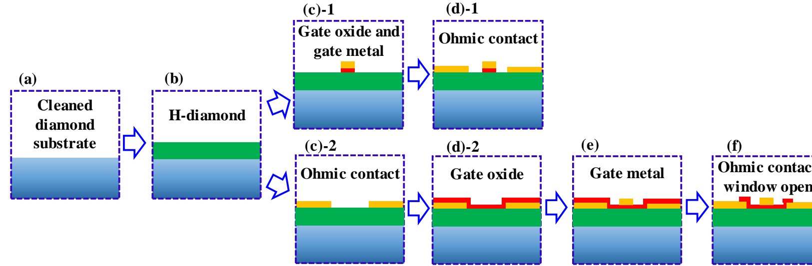

Fig. 1. Fabrication process for the H-diamond MOS capacitors

Japan) is employed to form the patterns. The LOR 5A and AZ 5214E photoresists are sequentially coated to cover the entire H-diamond surface. After baking at 180 and 110 °C for 5.0 and 2.0 min, respectively, the sample is exposed using the laser lithography system and developed in tetramethylammonium hydroxide (TMAH) solution for 2.0–2.5 min. The oxide insulators that have formation temperatures lower than 150 °C are then deposited by atomic layer deposition (ALD, SUNALE R-100B, Picosun Altech Corp., Ltd., Tokyo, Japan), radio-frequency sputtering deposition (RF-SD, handmade), and electron-gun evaporation (EV, RDEB-1206K, R-DEC Co. Ltd., Ibaraki, Japan) systems [Fig. 1(c)-1]. The gate metal layers of Ti/Au are formed using the EV system. Finally, the Ohmic contacts made of Pd/Ti/Au layers are formed on the H-diamond [Fig. 1(d)-1]. Here, the Pd metal is in direct contact with the H-diamond surface with a low contact resistivity [29]. The photoresists are lifted off in the N-methylpyrrolidone (NMP) solution at room temperature for 3.0 h.

Alternatively, the Ohmic contacts can be deposited first. After coating, exposing, and developing the photoresists, the Ohmic contact layers (Pd/Ti/Au) are evaporated on the photoresist-free area using the EV system [Fig. 1(c)-2]. The oxide insulators are formed at a deposition temperature higher than 150 °C and cover the entire surface of the sample [Fig. 1(d)-2]. Then, the gate metals (Ti/Au) are formed on the oxide insulators [Fig. 1(e)]. Finally, the windows for accessing the Ohmic contact electrodes are opened in the oxide insulator by capacitively coupled plasma reactive-ion etching system (CCP-RIE, SAMCO International Inc., Kyoto, Japan) using CHF_3 + Ar [Fig. 1(f)]. The plasma power, CHF_3 flow rate, and Ar flow rate are 100 W, 10 sccm, and 40 sccm, respectively. The electrical properties are measured using an MX-200/B prober (Vector Semiconductor Corp., Ltd., Tokyo, Japan) and a B1500A parameter analyzer (Agilent Technologies Inc., Tokyo, Japan) at room temperature (RT).

2.2 Leakage current densities for H-diamond MOS capacitors

Figures 2(a) and 2(b) show a scanning electron microscopy (SEM) image and schematic structure of the H-diamond MOS capacitor, respectively. The diameter of the circular gate electrode and interspacing between the gate and Ohmic electrodes are 200 and 10 µm, respectively. Figure 2(c) shows J as a function of the electric field for the H-diamond MOS capacitors with different oxide insulators as dielectric layers

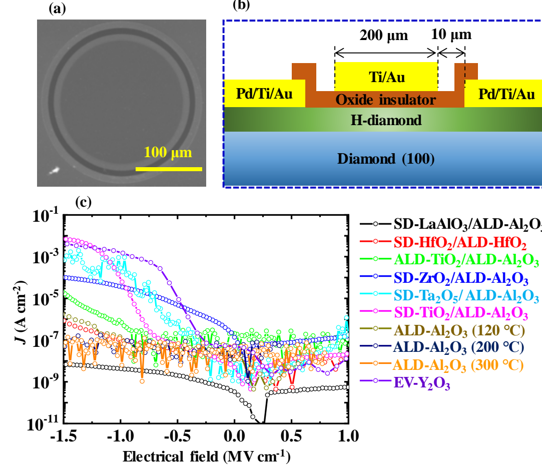

Fig. 2. (a) and (b) The SEM image and schematic structure of the H-diamond MOS capacitor, respectively. (c) J as a function of the electric field for the H-diamond MOS capacitors with different oxide insulators as dielectric layers.

Table 1. Summary of the J values at –1.5 MV cm^{-1} for the H-diamond MOS capacitors with the different oxide insulators as dielectric layers [8, 9, 20].

Oxide insulator	Formation technique	Formation temperature	Thickness (nm)	J (A cm^{-2})
$LaAlO_3/Al_2O_3$	SD/ALD	RT/120 °C	26.8/4.3	6.9×10^{-9}
HfO_2/HfO_2	SD/ALD	RT/120 °C	30.1/4.0	8.4×10^{-7}
TiO_2/Al_2O_3	ALD/ALD	120 °C/120 °C	25.0/4.0	2.1×10^{-5}
ZrO_2/Al_2O_3	SD/ALD	RT/120 °C	32.5/4.0	1.0×10^{-4}
Ta_2O_5/Al_2O_3	SD/ALD	RT/120 °C	24.5/4.0	7.6×10^{-4}
TiO_2/Al_2O_3	SD/ALD	RT/120 °C	24.4/4.0	7.3×10^{-3}
Al_2O_3	ALD	120 °C	17.9	1.7×10^{-6}
		200 °C	25.5	4.9×10^{-8}
		300 °C	25.3	5.2×10^{-8}
Y_2O_3	EV	RT	24.5	4.4×10^{-3}

[8, 9, 20]. The electric field is determined by dividing the gate voltage by the thickness of the oxide insulator. The J values for the MOS capacitors at the electric field of −1.5 MV cm^{-1} are summarized in Table 1. For the SD-oxide/ALD-oxide/H-diamond and ALD-oxide/ALD-oxide/H-diamond MOS capacitors, the ALD-Al_2O_3 and ALD-HfO_2 with thicknesses of approximately 4 nm are deposited on the H-diamond as buffer layers to protect the hydrogen surface from damage caused by the plasma discharge during the SD-insulator deposition.

The SD-TiO_2/ALD-Al_2O_3/H-diamond and SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOS capacitors show the highest and lowest J values of 7.3×10^{-3} and 6.9×10^{-9} A cm^{-2}, respectively. Furthermore, J for the ALD-TiO_2/ALD-Al_2O_3/H-diamond MOS

capacitor is lower than that for the SD-TiO_2/ALD-Al_2O_3/H-diamond. This implies that the dielectric quality for the ALD-TiO_2 is higher than that of the SD-TiO_2. For the MOS capacitor with the single ALD or EV oxide insulator as the dielectric, the J value for the ALD-Al_2O_3/H-diamond MOS capacitor is lower than that for the EV-Y_2O_3/H-diamond MOS capacitor. The J value for the ALD-Al_2O_3 (120 °C)/H-diamond MOS capacitor is 1.7×10^{-6} A cm^{-2}, which is larger than that (4.9×10^{-8} A cm^{-2}) for the ALD-Al_2O_3 (200 °C)/H-diamond MOS capacitor. This is possibly due to the improved quality of the Al_2O_3 film deposited at a higher temperature. However, the J value changes to 5.2×10^{-8} A cm^{-2} for the ALD-Al_2O_3 (300 °C)/H-diamond MOS capacitor. Because the H-diamond channel is thermally sensitive [30], the high deposition temperature of the Al_2O_3 might damage the interface quality between the ALD-Al_2O_3 and H-diamond, resulting in the increase of J.

2.3 Capacitance-voltage properties for H-diamond MOS capacitors

Figures 3(a), 3(b), and 3(c) show frequency-dependent C-V characteristics of the H-diamond MOS capacitors with the ALD-Al_2O_3 deposited at 120, 200, and 300 °C, respectively [9]. The measurement frequency is varied in the range from 1 to 100 kHz. For the ALD-Al_2O_3 (120 °C)/H-diamond MOS capacitor, a slight decrease in the maximum capacitance (C_{OX}) is observed with increasing frequency (from 0.313 μF cm^{-2} at 1 kHz to 0.301 μF cm^{-2} at 100 kHz). However, for the Al_2O_3 (200 °C)/H-diamond and Al_2O_3 (300 °C)/H-diamond MOS capacitors, the C_{OX} values are stable at approximately 0.272 and 0.295 μF cm^{-2}, respectively. Based on the values of C_{OX} at 1 kHz and the film thicknesses, the dielectric constants of the ALD-Al_2O_3 films deposited at 120, 200, and 300 °C are calculated to be 6.3, 8.0, and 8.6, respectively. Increasing the deposition temperature significantly improves the dielectric property of

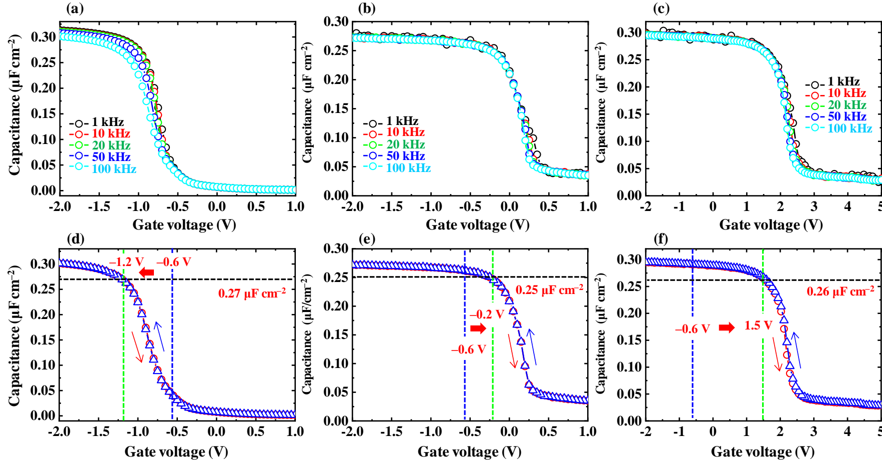

Fig. 3. (a), (b), and (c) Frequency-dependent C-V characteristics of the ALD-Al_2O_3/H-diamond MOS capacitors with Al_2O_3 films deposited at 120, 200, and 300 °C, respectively. (d), (e), and (f) Hysteresis characteristics of the C-V curves for the ALD-Al_2O_3/H-diamond MOS capacitors with Al_2O_3 films deposited at 120, 200, and 300 °C, respectively.

ALD-Al_2O_3.

Figures 3(d), 3(e), and 3(f) display the hysteresis characteristics of the *C-V* curves at 100 kHz for the ALD-Al_2O_3 (120 °C)/H-diamond, ALD-Al_2O_3 (200 °C)/H-diamond, and ALD-Al_2O_3 (300 °C)/H-diamond MOS capacitors, respectively. The red circles and blue triangles represent the responses to sweeping the gate voltage from negative to positive and from positive to negative, respectively. For all the MOS capacitors, no hysteresis voltage is observed. Therefore, the trapped charge densities in the ALD-Al_2O_3 films are considerably low [31, 32]. The flat band capacitances (C_{FB}) are calculated using equation (1) to be 0.27, 0.25, and 0.26 µF cm^{-2} for the ALD-Al_2O_3 (120 °C)/H-diamond, ALD-Al_2O_3 (200 °C)/H-diamond, and ALD-Al_2O_3 (300 °C)/H-diamond MOS capacitors, respectively [33].

$$C_{FB} = \frac{1}{\frac{1}{C_{OX}} + \frac{L_D}{\varepsilon_{diamond}\varepsilon_0}}, \qquad (1)$$

where $\varepsilon_{diamond}$ is the dielectric constant of diamond (5.7), ε_0 is the vacuum dielectric constant (8.85 × 10^{-12} F m^{-1}), and L_D is the Debye length of H-diamond, which is calculated to be 2.0 nm based on a hole concentration of 2 × 10^{18} cm^{-3} for the H-diamond channel layer [34]. The experimental flat band voltages for the ALD-Al_2O_3 (120 °C)/H-diamond, ALD-Al_2O_3 (200 °C)/H-diamond, and ALD-Al_2O_3 (300 °C)/H-diamond MOS capacitors are determined to be −1.2, −0.2, and 1.5 V, respectively.

Based on the work function difference between the Ti electrode (4.3 eV) and the H-diamond (4.9 eV) [35], the theoretical flat band voltage for an H-diamond MOS capacitor is –0.6 V. Therefore, the voltage shifts between the experimental and theoretical flat band voltages for the ALD-Al_2O_3 (120 °C)/H-diamond, ALD-Al_2O_3 (200 °C)/H-diamond, and ALD-Al_2O_3 (300 °C)/H-diamond MOS capacitors are –0.6, 0.4, and 2.1 V, respectively. These shifts are attributed to the presence of fixed charges in the ALD-Al_2O_3 films and at the ALD-Al_2O_3/H-diamond interfaces [31]. Based on these values and the C_{OX}, the fixed charge densities for the ALD-Al_2O_3 (120 °C)/H-diamond, ALD-Al_2O_3 (200 °C)/H-diamond, and ALD-Al_2O_3 (300 °C)/H-diamond MOS capacitors are calculated using equation (2) to be 1.1 × 10^{12}, –6.8 × 10^{11}, and –3.9 × 10^{12} cm^{-2}, respectively [33].

$$\frac{V_{FB} - \Delta W / q}{q} = \frac{Q}{C_{OX}}, \qquad (2)$$

where q is the elementary charge of 1.6×10^{-19} C.

3. H-diamond MOSFETs

3.1 Planar-type and T-type H-diamond MOSFETs

3.1.1 Fabrication process for the planar-type and T-type H-diamond MOSFETs

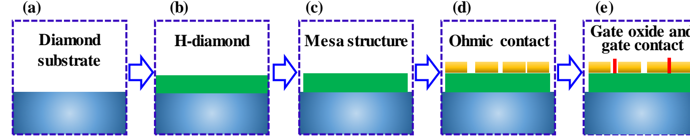

Fig. 4. Fabrication process for the planar-type and T-type H-diamond MOSFETs

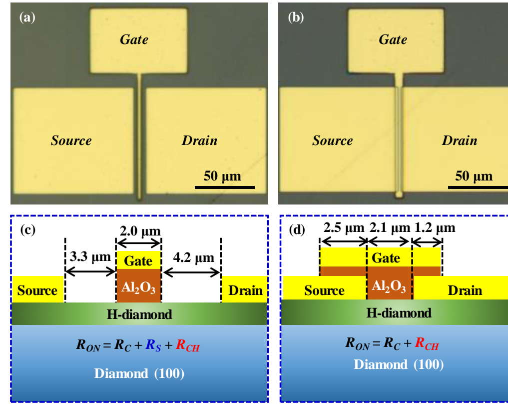

Fig. 5. (a) and (b) Surface morphologies of the planar-type and T-type H-diamond MOSFETs, respectively. (c) and (d) Schematic diagrams of the planar-type and T-type H-diamond MOSFETs, respectively.

Figure 4 shows the fabrication process for the planar-type and T-type ALD-Al_2O_3/H-diamond MOSFETs. They are fabricated on the same H-diamond epitaxial layer [Fig. 4(b)]. Mesa structures for the H-diamond MOSFETs are formed by CCP-RIE in an O_2 atmosphere [Fig. 4(c)]. The O_2 flow rate, chamber pressure, source power, and etching time are 100 sccm, 10 Pa, 50 W, and 90 s, respectively. The Pd/Ti/Au contacts are formed on the H-diamond using the EV system [Fig. 4(d)]. Finally, the Al_2O_3 gate oxide and Ti/Au gate contacts are formed by ALD at 120 °C and using the EV system, respectively [Fig. 4(e)]. The thickness of the Al_2O_3 layer is 32.3 nm.

Figures 5(a) and 5(b) show the surface morphologies of the planar-type and T-type H-diamond MOSFETs, respectively. Their schematic diagrams are shown in Figs. 5(c) and 5(d), respectively. The gate width (W_G) and area of the Ohmic contact electrodes for both MOSFETs are 100 μm and 10,000 μm^2, respectively. The gate length (L_G) values for the planar-type and T-type H-diamond MOSFETs are 2.0 and 2.1 μm, respectively. The interspace lengths of the source-to-gate ($L_{S\text{-}G}$) and drain-to-gate ($L_{D\text{-}G}$) electrodes for the planar-type H-diamond MOSFET are 3.3 and 4.5 μm, respectively. The Al_2O_3 gate oxide covers the source/drain electrodes for the T-type H-diamond MOSFET with distances of 2.5 and 1.2 μm, respectively. The on-resistance (R_{ON}) for the planar-type H-diamond MOSFET is composed of Ohmic contact resistance (R_C) for the metal/H-diamond interface, surface resistance (R_S) for the H-diamond epitaxial layer interspace between the source/drain and gate oxide electrodes, and channel resistance (R_{CH}) for the H-diamond epitaxial layer under the oxide insulator. Because

there is no interspace between the source/drain and gate oxide electrodes for the T-type H-diamond MOSFET, the R_S is zero [18].

3.1.2 Electrical properties for the planar-type and T-type H-diamond MOSFETs

Figure 6(a) shows J as a function of the gate-to-source voltage (V_{GS}) for the planar-type (black circles) and T-type (red circles) H-diamond MOSFETs. Despite the metal/oxide/metal structure in the T-type H-diamond MOSFET, its J is the same level as that for the planar-type MOSFET. As the V_{GS} changes from –10.0 to 8.0 V, the J values for both MOSFETs are lower than 3.0×10^{-7} A/cm^2. When the V_{GS} varies from –10.0 to –28.0 V, their J values gradually increase. The gate breakdown voltage is 24.8 V for the planar-type H-diamond MOSFET and 26.2 V for the T-type H-diamond MOSFET. The breakdown field values for the Al_2O_3 insulators are calculated as the V_{GS} divided by the Al_2O_3 film thickness (32.3 nm), resulting in 7.7 and 8.1 MV cm^{-1} for the planar-type and T-type H-diamond MOSFETs, respectively.

Figures 6(b) and 6(c) show the drain current (I_D) versus drain voltage (V_D) curves for the planar-type and T-type H-diamond MOSFETs, respectively. The I_D is normalized by the W_G of 100 μm. The V_{GS} is changed from −10.0 to 10.0 V in steps of 1.0 V. Both the planar-type and T-type MOSFETs show p-type characteristics and distinct pinch-off behaviors. The $I_{D,max}$ values for the planar-type and T-type MOSFETs are −80.0 and −160.0 mA mm^{-1}, respectively. At $V_{GS} = -10.0$ V, the R_{ON} values normalized by the W_G for the planar-type and T-type MOSFETs can be extracted as 119.6 and 35.6 Ω mm from the linear regions of their I_D-V_D characteristics, respectively. The larger R_{ON} for the planar-type H-diamond MOSFET is ascribed to the interspaces of the source/drain and gate electrode ($R_S \neq 0$). The I_D-V_{GS} characteristics for the MOSFETs are shown in Fig. 6(d) at $V_D = -10.0$ V. The on/off ratios for both

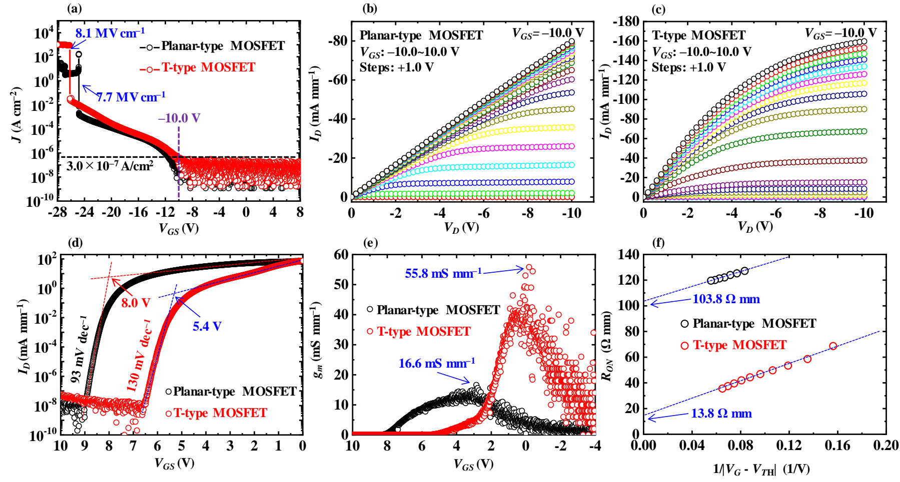

Fig. 6. (a) J as a function of V_{GS} for the planar-type and T-type H-diamond MOSFETs. (b) and (c) The I_D-V_D plots for the planar-type and T-type H-diamond MOSFETs, respectively. (d) and (e) The I_D-V_{GS} and g_m-V_{GS} characteristics for the planar-type and T-type H-diamond MOSFETs, respectively. (f) The R_{ON} as a function of $1/|V_{GS}–V_{TH}|$ for the planar-type and T-type H-diamond MOSFETs.

MOSFETs are larger than 10^{10}. Using a linear extrapolation method, the threshold voltage (V_{TH}) values for the planar-type and T-type H-diamond MOSFETs are determined to be 5.4 ± 0.1 and 8.0 ± 0.1 V, and their subthreshold swing (SS) values are deduced from the inverse slopes of the I_D-V_{GS} characteristics to be 93 and 130 mV/dec, respectively.

The interfacial trapped charge density (D_{it}) for the Al_2O_3/H-diamond can be calculated using equation (3) [36].

$$SS = \frac{kT}{q}\ln(10)(1+\frac{qD_{it}}{C_{OX}}), \tag{3}$$

where k and T are Boltzmann's constant (8.62×10^{-5} eV K^{-1}) and RT (298.15 K), respectively. The C_{OX} is the maximum capacitance density of Al_2O_3, which can be calculated as 0.173 μF/cm^2 using equation (4).

$$C_{OX} = \frac{\varepsilon_0\varepsilon_r}{d}, \tag{4}$$

where ε_r is the dielectric constant of Al_2O_3 (6.3 at a deposition temperature of 120 °C), and d is the thickness of the Al_2O_3 layer (32.3 nm). By inserting the C_{OX} into equation (3), the D_{it} values for the Al_2O_3/H-diamond interface in planar-type and T-type MOSFETs can be calculated as 6.2×10^{11} and 1.3×10^{12} eV^{-1} cm^{-2}, respectively.

In addition to the Al_2O_3/H-diamond interface, there are vertical edge contacts between Al_2O_3 and the source/drain Ohmic contacts for the T-type H-diamond MOSFET, which may lead to the formation of interfacial defects and an increase in D_{it}. The g_m values as a function of V_{GS} for the planar-type and T-type H-diamond MOSFETs are shown in Fig. 6(e). They are determined based on the slopes of the linear portions of the I_D-V_{GS} curves. The $g_{m,max}$ values for the planar-type and T-type H-diamond MOSFETs are 16.6 and 58.8 mS/mm, respectively.

For an ideal H-diamond MOSFET, the R_C and R_S are considered negligible in the R_{ON}. The ideal drain current (I_D^0) is expressed with the ideal drain voltage (V_D^0) using equation (5) [31].

$$I_D^0 = \frac{\mu_{eff}C_{OX}\left\{(V_{GS}-V_{TH})-\frac{V_D^0}{2}\right\}V_D^0}{L_G}, \tag{5}$$

where μ_{eff} is the effective mobility of the H-diamond epitaxial layer. Thus, the R_{CH} can be calculated using equation (6).

$$R_{CH} = \left[\frac{\partial I_D^0}{\partial V_D^0}\right]^{-1}_{V_D^0=0} = \frac{L_G}{\mu_{eff}C_{OX}\left|V_{GS}-V_{TH}\right|}, \tag{6}$$

For a real H-diamond MOSFET, the R_{CH} under the Al_2O_3 film can be considered ideal. The relationships for the R_{ON} with R_C, R_S, and R_{CH} can be obtained using equation (7).

$$R_{ON} = R_C + R_S + R_{CH} = R_C + R_S + \frac{L_G}{\mu_{eff}C_{OX}\left|V_{GS}-V_{TH}\right|}, \tag{7}$$

The R_{ON} as a function of $1/|V_{GS}–V_{TH}|$ for the planar-type and T-type H-diamond MOSFETs are shown in Fig. 6(f). By fitting the red circles for the T-type H-diamond MOSFET, the R_C is 13.8 Ω mm (the y-axis intercept). By fitting the black circles for the planar-type H-diamond MOSFET, the ($R_C + R_S$) is observed to be 103.8 Ω mm.

Because the R_C for both MOSFETs is the same, the R_S for the planar-type H-diamond MOSFET can be calculated to be 90.0 Ω mm. By considering the R_{ON} values for the planar-type and T-type H-diamond MOSFETs (119.6 and 35.6 Ω mm, respectively) at $V_{GS} = −10.0$ V, the R_{CH} can be computed as 15.8 and 21.8 Ω mm, respectively. Based on the slopes of the fitting lines in Fig. 6(f), the μ_{eff} values for the H-diamond channel layer are 41.3 and 35.5 cm^2 V^{-1}s^{-1} in the planar-type and T-type MOSFETs, respectively.

3.2 Triple-gate fin-type H-diamond MOSFETs

3.2.1 Fabrication process for fin patterns and triple-gate H-diamond MOSFETs

Figures 7(a) and 7(b) show the fabrication processes for fin patterns and triple-gate H-diamond MOSFETs on a diamond substrate with dimensions of 5.0 × 5.0 × 0.3 mm, respectively [19]. To form the fin patterns on the diamond (001) substrate, a tungsten (W) metal layer is first sputtered using an automatic sputtering system to cover the entire substrate surface [Fig. 7(a)-i]. The positive photoresist FEP-171 is then coated on the sample and exposed using an electron beam lithography system (ELS-F125, Elionix Inc., Tokyo, Japan) [Fig. 7(a)-ii]. After the photoresist is developed [Fig. 7(a)-iii], the W metal and the diamond substrate at the photoresist-free area

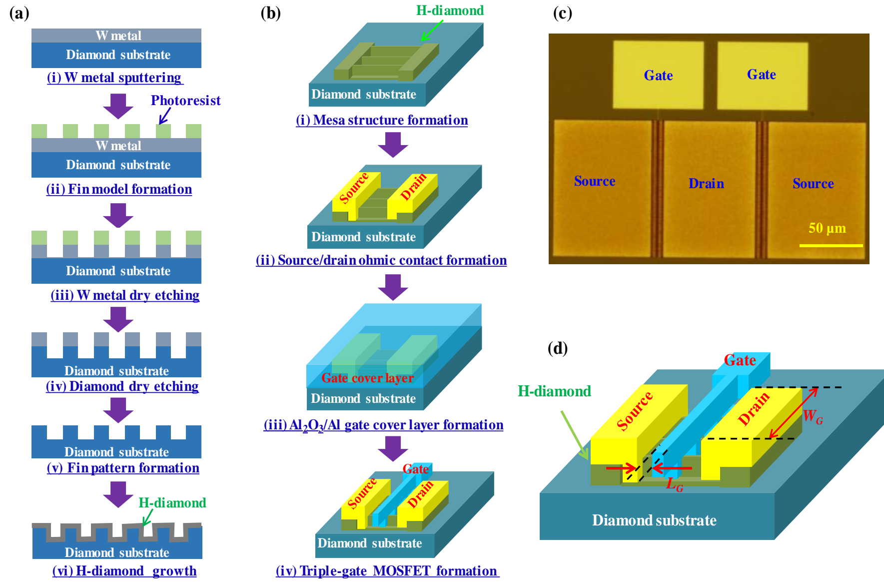

Fig. 7. (a) and (b) Fabrication processes for the fin-patterned H-diamond and triple-gate MOSFETs, respectively. (c) Top view of two triple-gate H-diamond MOSFETs. (d) Schematic diagram of the triple-gate H-diamond MOSFET.

are dry-etched in SF_6 and O_2 atmospheres, respectively, using an inductively coupled plasma reactive-ion etching system (RIE-101iPH, Samco Inc. Kyoto, Japan) [Fig. 7(a)-iv]. The residual W metal is cleaned again using SF_6 to form fin patterns on the diamond surface [Fig. 7(a)-v]. Then, the H-diamond epitaxial layer is grown on the substrate by MPCVD to form fin-patterned H-diamond [Fig. 7(a)-vi].

After the formation of fin-patterned H-diamond, the triple-gate MOSFETs are then fabricated [Fig. 7(b)]. The fin-patterned H-diamond is first etched in an O_2 atmosphere using the CCP-RIE system to form a mesa structure [Fig. 7(b)-i]. The Pd/Ti/Au Ohmic contacts are then evaporated on the fin-patterned H-diamond to form the source/drain electrodes using the electron-gun evaporation system [Fig. 7(b)-ii]. The Al_2O_3 gate insulator layer that has been used for the fabrication of high-performance diamond MOS devices and the Al gate electrode are then deposited to cover the entire sample surface by ALD and sputtering, respectively [Fig. 7(b)-iii]. Then, the sample is coated with PMGI-SF6S/FEP-171 bilayer photoresists and exposed using the electron beam lithography system. After developing the photoresists, the Al and Al_2O_3 layers on the photoresist-free areas are wet-etched using Al etchant and TMAH solutions, respectively. Finally, the photoresists are lifted off in NMP solution, and the fabrication of the triple-gate H-diamond MOSFETs is complete [Fig. 7(b)-iv]. The top view and schematic diagram of the triple-gate H-diamond MOSFETs are shown in Figs. 7(c) and 7(d), respectively. The L_G, $L_{S\text{-}G}/L_{D\text{-}G}$, and W_G for these devices are 500 nm, 500/500 nm, and 100.5 μm, respectively.

3.2.2 Morphologies for the fin-patterned diamond and triple-gate MOSFETs

Figures 8 shows SEM images of the fin-patterned diamond substrate [Figs. 8(a), 8(b), and 8(c)] and triple-gate MOSFET, and transmission electron microscopy

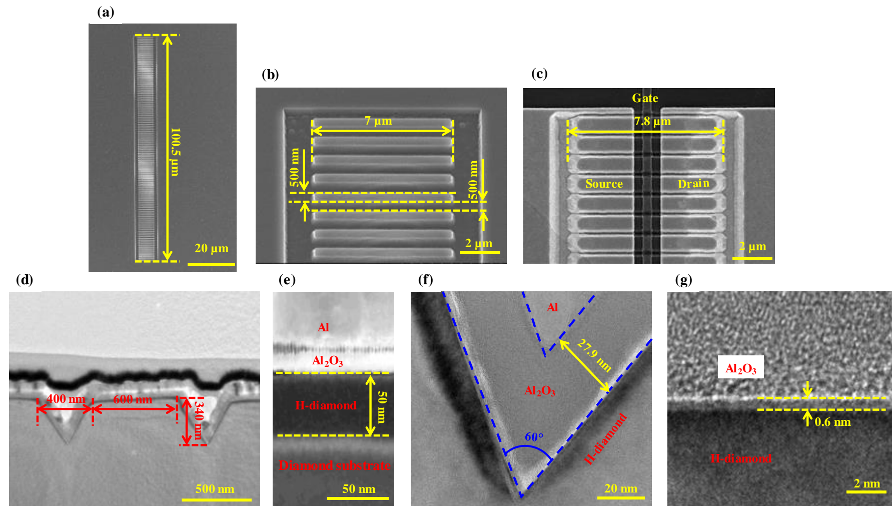

Fig. 8. (a) and (b) SEM images of the fin-patterned diamond substrate. (c) SEM image of the triple-gate MOSFET. (d), (e), (f), and (g) Interfacial TEM images of the triple-gate H-diamond MOSFET.

(TEM) images of interfaces in the triple-gate H-diamond MOSFET [Figs. 8(d), 8(e), 8(f), and 8(g)]. As shown in the SEM images [Figs. 8(a) and 8(b)], the total width of the diamond fin pattern and the fin length are 100.5 and 7 µm, respectively. Both the fin width and the interspacing between fins are 500 nm. The fin height was confirmed to be 500 nm using a 3D-measurement laser microscope. The gate, source, and drain contacts for the H-diamond triple-gate MOSFET can be seen in Fig. 8(c). After growing the H-diamond epitaxial layer by MPCVD, the fin length and width increased to 7.8 µm and 600 nm, respectively. The interspacing between fins and the fin height decreased to 400 and 340 nm, respectively [Fig. 8(d)]. The H-diamond epitaxial layer thickness is approximately 50 nm [Fig. 8(e)].

Figure 8(f) shows a high-resolution TEM image for the magnification of the left adjacent fins in Fig. 8(d). The angle between two adjacent fins is 60°. The two inclined active planes of each fin in the triple-gate MOSFETs are the $(\pm\frac{\sqrt{3}}{3}01)$ sides. The equivalent W_G for the triple-gate MOSFET can be calculated as 139.6 µm. The ALD-Al_2O_3 layer thickness is approximately 27.9 nm, which agrees well with the measurement results obtained using the ellipsometer. An interfacial layer with a thickness of approximately 0.6 nm exists between H-diamond and Al_2O_3 [Fig. 8(g)]. This layer may result from reactions between the oxides or nitrides and the surface adsorbates on the H-diamond epitaxial layer [37, 38].

3.2.3 Electrical properties for the triple-gate H-diamond MOSFETs

To compare the electrical properties of triple-gate H-diamond MOSFETs with the common planar-type devices, the planar-type MOSFETs are also fabricated simultaneously with the triple-gate devices on the same diamond substrate. Both triple-gate and planar-type MOSFETs have the same L_G, W_G, and $L_{S\text{-}G}/L_{D\text{-}G}$. The difference between them is the existence of fin patterns on the diamond substrate for the triple-gate MOSFET. Figure 9(a) shows the gate leakage current for the triple-gate and planar-type MOSFETs. The gate leakage current curves for the MOSFETs are measured for a V_{GS} from 30.0 to −10.0 V. At the V_{GS} of −10.0 V, the holes are accumulated at the Al_2O_3/H-diamond interface and the MOSFETs are in the on state. The leakage current of the triple-gate MOSFET is 1.4×10^{-10} A, which is higher than that of the planar-type device, 2.3×10^{-12} A. This is possibly ascribed to the longer equivalent W_G and rougher etching surface for the triple-gate MOSFET than those for the planar-type device. The J for the planar-type MOSFET can be calculated to be 4.6×10^{-6} A cm^{-2} using the gate leakage current divided by the area of the gate electrode (5.025×10^{-7} cm^2). This J is one order higher than that of the Al_2O_3/H-diamond MOS capacitor [9]. Because the fabrication process for MOSFETs is more complicated than that for MOS capacitors, the potential device damage during fabrication for the former is more serious than that for the latter, which may lead to a higher leakage current for the MOSFET.

Figures 9(b) and 9(c) show the I_D-V_D characteristics for the triple-gate and planar-type MOSFETs, respectively. The V_{GS} is varied from −10.0 to 20.0 V in steps of 1.0 V. The I_D for the planar-type MOSFET is normalized using the W_G of 100.5 µm.

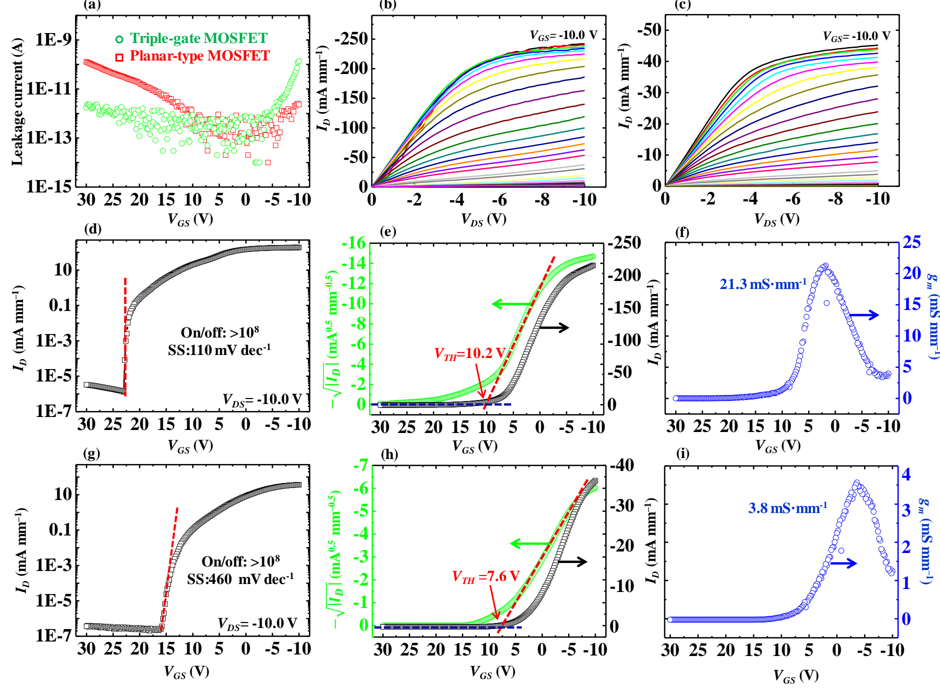

Fig. 9. (a) The gate leakage currents for the triple-gate and planar-type MOSFETs. (b) and (c) I_D-V_D characteristics for the triple-gate and planar-type MOSFETs, respectively. (d), (e), and (f) The log $|I_D|$-V_{GS}, $-\sqrt{|I_D|}$-V_{GS}, and g_m-V_{GS} characteristics of the triple-gate MOSFET, respectively. (g), (h), and (i) The log $|I_D|$-V_{GS}, $-\sqrt{|I_D|}$-V_{GS}, and g_m-V_{GS} characteristics of the planar-type MOSFET, respectively.

That for the triple-gate MOSFET is normalized using its equivalent W_G of 139.6 μm. Both MOSFETs show *p*-type channel and pinch-off characteristics. There are also clear linear relationships between I_D and low V_D for both devices, which indicate effective Ohmic contact between the Pd/Ti/Au and H-diamond channel layers. The absolute $I_{D,max}$ for the triple-gate MOSFET is 174.2 mA mm^{-1}, which is much higher than the value of 45.2 mA mm^{-1} obtained for the planar-type device. The value of R_{ON} can be extracted from the linear region of the I_D-V_D characteristics, which is 31.9 and 98.0 Ω mm for the triple-gate and planar-type MOSFETs, respectively.

While the equivalent W_G of the triple-gate MOSFET is only 1.4 times longer than that for the planar-type device, the absolute $I_{D,max}$ for the former (174.2 mA mm^{-1}) is approximately four times larger than the corresponding value for the latter (45.2 mA mm^{-1}). It was previously reported that the inclined H-diamond (111) plane has a higher hole density than the planar H-diamond (001) plane [39]. In the current study, because each fin of the triple-gate MOSFET has two inclined ($\pm\frac{\sqrt{3}}{3}$ 01) planes, it is natural to believe that the hole density of the fin-type H-diamond channel layer

must be higher than that of the planar H-diamond (001) layer. This may be the reason for the higher $I_{D,max}$ and lower R_{ON} obtained for the triple-gate MOSFET compared with the theoretical values.

The on/off ratio of the triple-gate MOSFET is higher than 10^8 [Fig. 9(d)], similar to that of the planar-type device [Fig. 9(g)]. The SS is 110 mV dec^{-1} for the triple-gate MOSFET at a V_{DS} of −10.0 V. This value is much lower than that of the planar-type device, 460 mV dec^{-1}. The threshold voltage (V_{TH}) values of the MOSFETs can be determined based on $-\sqrt{|I_D|}$ as a function of V_{GS}, which are 10.2 ± 0.1 and 7.6 ± 0.1 V for the triple-gate and planar-type MOSFETs, respectively [Figs. 9(e) and 9(h)]. The $g_{m,max}$ values for the triple-gate and planar-type MOSFETs are 15.3 ± 0.1 and 3.8 ± 0.1 mS mm^{-1}, respectively [Figs. 9(f) and 9(i)].

3.3 Enhancement-mode H-diamond MOSFETs

3.3.1 Enhancement-mode SD-oxide/ALD-oxide/H-diamond MOSFETs

In sections 3.1 and 3.2, the planar-type, T-type, and triple-gate fin-type H-diamond MOSFETs have been fabricated using the single ALD-Al_2O_3 layers as the oxide insulators. All of them demonstrate depletion-mode characteristics. In contrast, insulators with bilayer structure are also deposited by ALD and RF-SD on the H-diamond for the MOSFETs [6, 7, 40, 41]. ALD-Al_2O_3 and ALD-HfO_2 with thicknesses of approximately 4 nm are deposited on the H-diamond as the buffer layers. The SD-Ta_2O_5/ALD-Al_2O_3/H-diamond and SD-ZrO_2/ALD-Al_2O_3/H-diamond MOSFETs show depletion-mode characteristics [40, 41], but the SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond and SD-HfO_2/ALD-HfO_2/H-diamond MOSFETs show enhancement-mode characteristics [6, 7]. The depletion- and enhancement-mode characteristics for the SD-oxide/ALD-oxide/H-diamond-based MOSFETs are independent of the insulator materials and device structures and are reproducibly dependent on the fabrication processes. Because the fabrication processes for the SD-oxide/ALD-oxide/H-diamond-based MOSFETs are the same as those of the planar-type, T-type, and triple-gate H-diamond MOSFETs, they operate with depletion-mode characteristics.

For the fabrication processes of the depletion-mode H-diamond MOSFETs, mesa-structure formation is the first common step, and the source/drain Ohmic contacts are fabricated in the second step. Conversely, gate oxides and contacts fabricated in the second step produce the enhancement-mode MOSFETs [6, 7]. By comparing the experimental details between the two fabrication processes, the distinct difference is that the insulator/H-diamond interface for the enhancement-mode MOSFETs is annealed at 180 °C for 5 min during the photoresist baking step, and there is no annealing process for the depletion-mode MOSFETs. Because the enhancement-mode characteristic is ascribed to hole depletion in the H-diamond channel layer at zero gate voltage and hole accumulation in the H-diamond channel layer is thermo-sensitive [38], the annealing step may reduce the number of holes and promote the enhancement-mode characteristics. In this section, we demonstrate that annealing leads to the formation of enhancement-mode SD-oxide/ALD-oxide/H-diamond-based MOSFETs [30].

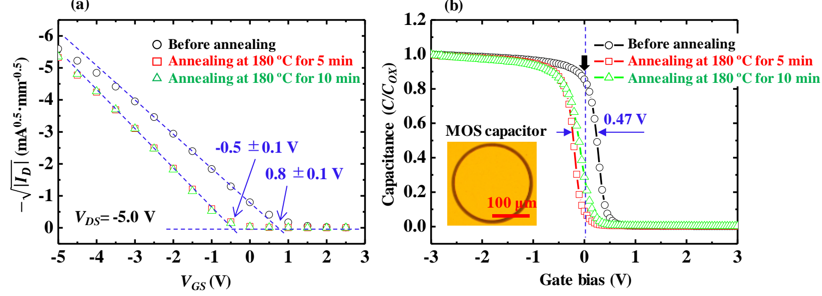

Fig. 10. (a) V_{TH} determination of SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOSFETs before and after annealing at 180 °C for 5 and 10 min. (b) *C-V* curves for SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOS capacitors before (black) and after annealing at 180 °C for 5 min (red) and 10 min (green). The inset shows the top view of the MOS capacitor.

The transfer characteristics of the SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOSFETs before and after annealing at 180 °C for 5 and 10 min are used to determine the V_{TH} values, as shown in Fig. 10(a). The V_{TH} before annealing is determined to be 0.8 ± 0.1 V with the depletion-mode characteristics. However, after annealing at 180 °C for 5 and 10 min, the V_{TH} value is changed to the constant value of –0.5 ± 0.1 V with the enhancement-mode characteristics. Annealing can change the MOSFET from the depletion-mode to the enhancement-mode. This indicates that the holes in the H-diamond channel layer at the equilibrium stage disappear after annealing at 180 °C.

Figure 10(b) shows the *C-V* characteristics for the SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOS capacitors. The black, red, and green lines represent the *C-V* curves before annealing and after annealing at 180 °C for 5 and 10 min, respectively. The inset figure is the top view of the MOS capacitor. All the *C-V* curves show distinct accumulation and depletion regions, which suggest that a high-quality SD-$LaAlO_3$/ALD-Al_2O_3 insulator is fabricated on the H-diamond. The *C-V* curves in the depletion regions before and after annealing at 180 °C for 5 min show sharp dependence on the gate bias, which indicates the low-density interfacial state at the SD-$LaAlO_3$/ALD-Al_2O_3 interface. For an annealing time of 10 min, the depletion *C-V* curve shows a slight stretch in the curve, which implies that the long annealing possibly degrades the quality of the SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond interface.

Figure 11 shows the schematic structures and band diagrams of the H-diamond epitaxial layer [Fig. 11(a)], and SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond before [Fig. 11(b)] and after [Figs. 11(c) and 11(d)] annealing, respectively. The VBM, CBM, and E_F in the figure represent the valence band maximum, conduction band minimum, and Fermi level, respectively. For the H-diamond epitaxial layer [Fig. 11(a)], there are negatively charged acceptors and C-H bonds close to the surface, and holes are generated in the H-diamond channel layer by transfer doping. The H-diamond shows upward band bending toward the surface, which indicates hole accumulation. After depositing the $LaAlO_3$/Al_2O_3 bilayer on the H-diamond, the negatively charged accep-

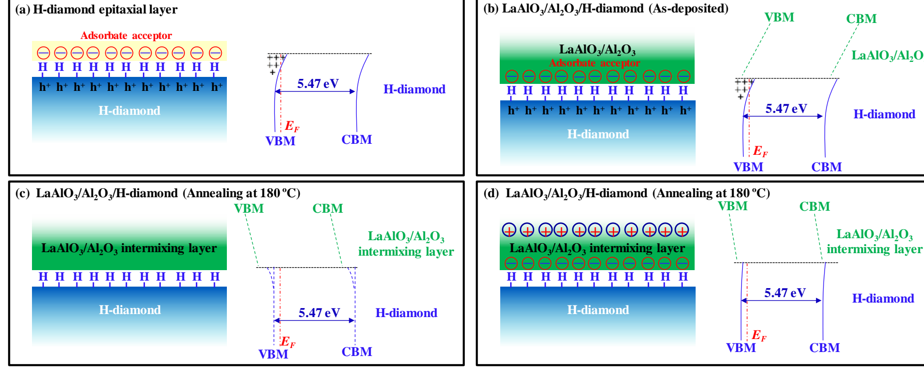

Fig. 11. Structures and band diagrams of (a) an H-diamond epitaxial layer and SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond (b) before and (c, d) after annealing. VBM, CBM, and E_F are the valence band maximum, conduction band minimum, and Fermi level, respectively.

tors are kept close to the insulator, and then the H-diamond shows upward band bending toward the ALD-Al_2O_3/H-diamond interface [Fig. 11(b)]. Because both the C-H bonds and the negatively charged acceptors are located at the interface, holes can be accumulated in the H-diamond channel layer, and therefore the MOSFET before annealing shows depletion-mode characteristics.

After annealing the MOSFET at 180 °C, there are two possible charge states at the interface. One contains no negatively charged acceptors at the interface. The energy band of the H-diamond shows flat or downward bending toward the interface [Fig. 11(c)]. The other state involves negatively charged acceptors at the interface, and the energy band of the H-diamond shows slight upward band bending toward the interface [Fig. 11(d)]. However, the negatively charged acceptors are compensated by the positive charges generated in the SD-$LaAlO_3$/ALD-Al_2O_3 intermixing layer after annealing. For both possible interfacial charge states, it is difficult to accumulate holes in the H-diamond channel layer at V_{GS} = 0 V. The annealed H-diamond MOSFET shows enhancement-mode characteristics. The origin of the enhancement-mode characteristics may be the reduction of the acceptor density close to the insulator/H-diamond interface after annealing. The possible negatively charged adsorbates that exist before and after deposition of the insulator layer are oxygen-based anions such as HCO_3^- and OH^- [33]. Annealing at 180 °C may provide the out-diffusion of the adsorbate acceptor or the generation of the positively charged compensator.

3.3.2 Enhancement-mode ALD-oxide/ALD-oxide/H-diamond MOSFETs

Not only the SD-oxide/ALD-oxide/H-diamond MOSFETs but also the ALD-oxide/ALD-oxide/H-diamond MOSFETs can operate with enhancement-mode characteristics [8]. Figure 12(a) shows the transfer characteristic of the I_D-V_D curve, which is used to determine the V_{TH} value for the planar-type ALD-TiO_2/ALD-Al_2O_3/H-

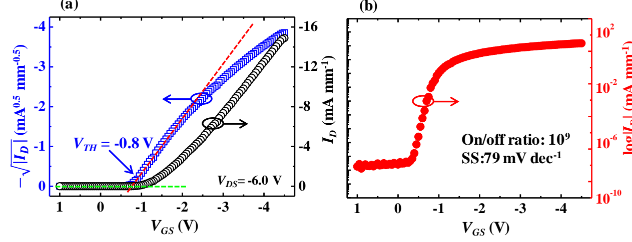

Fig. 12. Electrical properties of the ALD-TiO_2/ALD-Al_2O_3/H-diamond MOSFET. (a) Transfer characteristic of I_D-V_D used to determine V_{TH}. (c) The I_D-V_{GS} characteristic of the MOSFET used to determine the on/off ratio and *SS* value.

diamond MOSFET. The L_G and W_G of the MOSFET are 4 and 150 µm, respectively. The $L_{S\text{-}G}/L_{D\text{-}G}$ is 4/4 µm. The V_{TH} for the ALD-TiO_2/ALD-Al_2O_3/H-diamond is −0.8 ± 0.1 V. This indicates that the ALD-TiO_2/ALD-Al_2O_3/H-diamond MOSFET also operates with enhancement-mode characteristics. Notably, there is also an annealing process for the enhancement-mode ALD-TiO_2/ALD-Al_2O_3/H-diamond MOSFET.

An advantage of the ALD-TiO_2/ALD-Al_2O_3 bilayer over the SD-oxide/ALD-oxide bilayer on the H-diamond for the enhancement-mode MOSFETs is that during the formation of the SD-oxide/ALD-oxide bilayer, after depositing the ALD-oxide buffer layer in the ALD chamber, the sample is exposed to the air and moved into the SD chamber for the SD-oxide deposition. However, the ALD-TiO_2/ALD-Al_2O_3 bilayer can be formed in the same ALD chamber without exposure. Therefore, there is no effect of air contamination on the ALD-TiO_2/ALD-Al_2O_3 interface quality. The log $|I_D|$-V_{GS} characteristic of the MOSFET shown in Fig. 12(b) indicates that the on/off ratio of the device is as high as 8.3×10^8. The *SS* value of the ALD-TiO_2/ALD-Al_2O_3/H-diamond MOSFET is as low as 79 mV dec^{-1}.

3.3.3 Enhancement-mode EV-Y_2O_3/H-diamond MOSFETs

Because there is no plasma discharge damage for the hydrogen surface of the H-diamond under evaporation, the EV-Y_2O_3 film can be formed directly on the H-diamond [20]. Figures 13(a) and 13(b) show schematic cross-sectional structures of the T-type and planar-type Y_2O_3/H-diamond MOSFETs, respectively. For the T-type MOSFET, the gate electrode has top and bottom lengths of 9.3 and 2.4 µm, respectively. For the planar-type H-diamond MOSFETs, the L_G increases from 3.3 to 15.4 µm. The $L_{S\text{-}G}$ and $L_{D\text{-}G}$ for all planar-type H-diamond MOSFETs are 3 and 1.9 µm, respectively. The W_G for all the MOSFETs is kept at 100 µm.

Figures 13(c) and 13(d) show the $-\sqrt{|I_D|}$ -V_{GS} characteristics for the T-type and planar-type H-diamond MOSFETs, respectively. The V_{TH} value is determined to be −0.1 ± 0.1 for the T-type MOSFET. That is −1.8 ± 0.1 V for the planar-type Y_2O_3/H-diamond MOSFET at L_G = 3.3 µm. The V_{TH} values for all the MOSFETs are summarized in Fig. 13(e) as a function of L_G. With the increase of L_G from 3.3 ± 0.1 to 15.4 ± 0.1 µm, the V_{TH} for the MOSFETs changes in the range of −0.3 ± 0.1 to −2.0 ± 0.1 V. The variation of the V_{TH} is possibly attributed to the non-uniform hole density on

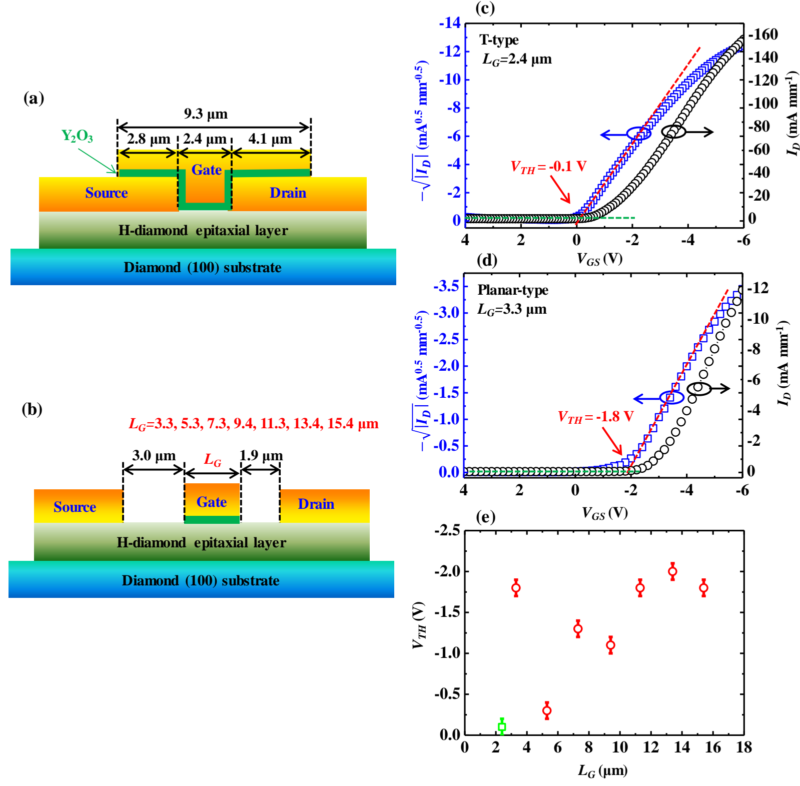

Fig. 13. (a) and (b) Schematic cross-sectional structures of T-type and planar-type Y_2O_3/H-diamond MOSFETs, respectively. (c) and (d) The $-\sqrt{|I_D|}$ -V_{GS} characteristics for the T-type and planar-type H-diamond MOSFETs, respectively. (e) The V_{TH}-L_G characteristics for the planar-type H-diamond MOSFETs.

the H-diamond channel layer. Furthermore, all the V_{TH} values are negative, implying enhancement-mode characteristics for all the EV-Y_2O_3/H-diamond MOSFETs.

The enhancement-mode characteristics for the Y_2O_3/H-diamond MOSFETs are also believed to be caused by the variation of negatively charged acceptors on the H-diamond. Compared with that of the previous enhancement-mode SD-oxide/ALD-oxide/H-diamond and ALD-oxide/ALD-oxide/H-diamond MOSFETs [6-8], the fabrication process of the enhancement-mode Y_2O_3/H-diamond MOSFETs is simpler. It is not necessary to deposit the oxide insulators in two steps. Additionally, because the gate contacts (Ti/Au) can be formed in the same chamber after evaporating the Y_2O_3 on the H-diamond, there is no undesirable surface contamination on the oxide insulator from the air.

Table 2 summarizes the effect of annealing on the depletion- and enhancement-mode characteristics of the H-diamond-based MOSFETs with different oxide insulators and device structures. If there is no annealing step in the fabrication process, the V_{TH} values are positive for the SD-oxide/ALD-oxide/H-diamond MOSFETs, corre-

sponding to the depletion-mode characteristics. Alternatively, if there is an annealing step in the process, the V_{TH} values are negative for the SD-oxide/ALD-oxide/H-diamond MOSFETs, corresponding to the enhancement-mode characteristics. Even though there is no annealing step for the EV-Y_2O_3/H-diamond MOSFETs, they operate with enhancement-mode characteristics, and although there is an annealing step for the ALD-Al_2O_3/H-diamond MOSFETs, they operate with depletion-mode characteristics.

Table 2. Effect of annealing on the depletion-/enhancement-mode (D-/E-mode) characteristics of the H-diamond-based MOSFETs with the different oxide insulators and device structures [6-8, 20, 40, 41].

	Oxide insulators	L_G (μm)	$L_{S\text{-}G}/L_{D\text{-}G}$ (μm)	V_{TH} (V)	D-/E-mode
No annealing	SD-$LaAlO_3$/ALD-Al_2O_3	4	5/5	0.8	D-mode
	SD-Ta_2O_5/ALD-Al_2O_3	4	0/0	1.3	D-mode
	SD-ZrO_2/ALD-Al_2O_3	4	0/0	1.3	D-mode
		4	5/5	1.4	D-mode
	EV-Y_2O_3	2.4	0/0	–0.1	E-mode
		3.3	3/1.9	–1.8	E-mode
	ALD-Al_2O_3	4	5/5	3.8	D-mode
Annealing	ALD-Al_2O_3	4	5/5	3.0	D-mode
	SD-$LaAlO_3$/ALD-Al_2O_3	4	5/5	–0.5	E-mode
		10	5/5	–3.6	E-mode
		20	5/5	–4.7	E-mode
		30	5/5	–5.0	E-mode
	SD-HfO_2/ALD-HfO_2	4	10/10	–1.3	E-mode
	ALD-TiO_2/ALD-Al_2O_3	4	4/4	–0.8	E-mode
	SD-TiO_2/ALD-Al_2O_3	4	4/4	–0.9	E-mode

4. H-diamond MOSFET logic circuits

4.1 Enhancement-mode MOSFET/load resistor NOT logic circuits

The development of the enhancement-mode H-diamond MOSFETs enables the fabrication of H-diamond MOSFET logic circuits [21-23]. Figure 14(a) shows the top view of the NOT logic circuits with various load resistors [21]. The load resistance is controlled by the distance between the output voltage (V_{out}) and power supply (V_{DD}) electrodes using the defined surface conductive layer, where the load resistors are denoted by *R1*, *R2*, *R3*, *R4*, and *R5.* The width of all the load resistors is 10 μm, and the lengths of the *R1*, *R2*, *R3*, *R4*, and *R5* resistors are 10, 20, 40, 80, and 160 μm, respectively. The $L_{S\text{-}G}/L_{D\text{-}G}$ of the enhancement-mode SD-$LaAlO_3$/ALD-Al_2O_3/H-

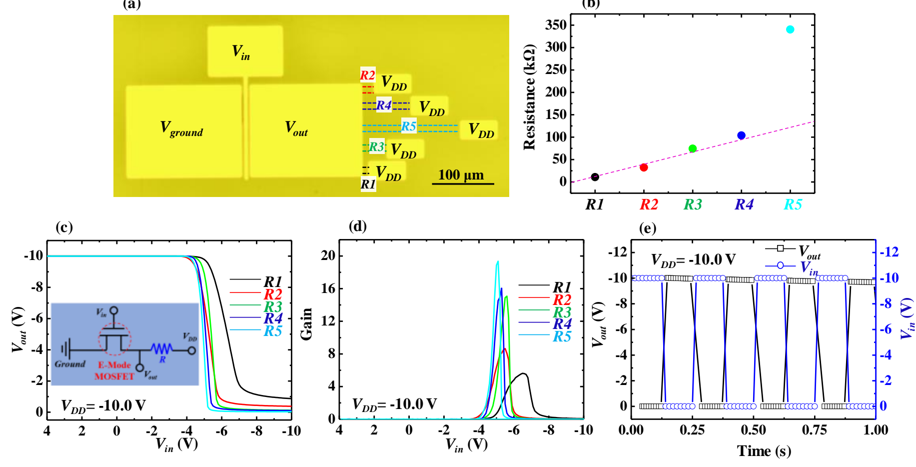

Fig. 14. (a) Top view of the NOT logic circuits with various load resistors, (b) resistance values for the *R1*, *R2*, *R3*, *R4*, and *R5* resistors, (c) the VTCs of the NOT logic circuits with the various load resistors, (d) the gain derived from the VTCs, and (e) the pulse response characteristic of the NOT logic ciruits with the load resistor of *R5* (340.2 kΩ). Inset figure in Fig. 14(c) is schematic diagram of the logic circuit.

diamond MOSFET is 5/5 µm. The L_G and W_G are kept at 4 and 150 µm, respectively. The resistance values for the resistors are shown in Fig. 14(b). With a linearly increasing length from *R1* to *R5*, the resistance increases linearly from 10.8 to 103.8 kΩ, except for the value of 340.2 kΩ for *R5*. The deviation may be attributed to the inhomogeneous conductivity in the H-diamond surface over the wide area.

Figure 14(c) shows the voltage transfer characteristics (VTCs) of the H-diamond MOSFET logic circuits with various load resistors, where the inset in the figure is the schematic of the logic circuit. The V_{DD} is kept at –10.0 V. Note that the NOT logical properties are observed for all H-diamond MOSFET logic circuits with the V_{in} ranging from 4.0 to –10.0 V. If the V_{in} is more positive than V_{TH}, the MOSFET is in the off state and no I_{DS} flows through the load resistor, resulting in $V_{out} = V_{DD}$. Likewise, if the V_{in} is more negative than the V_{TH}, the MOSFET turns on and I_{DS} flows, producing the voltage drop across the load resistor, which connects the V_{out} to the ground level. Thus, when V_{in} is “high” the V_{out} is “low”, and when V_{in} is “low” the V_{out} is “high”, which provides the inversion of the input signal.

The minimum V_{out} in the VTC curve with the large load resistance (for example, *R5*) is larger than that with the small load resistance (for example, *R1*). In addition, for the increasing load resistances from *R1* to *R5*, the slope of the transition regions in the VTC curve increases. The gain defined by $-dV_{out}/dV_{in}$ in the VTCs can be evaluated, as shown in Fig. 14(d). The gain increases from 5.6 to 19.4 with increasing load resistance from *R1* (10.8 kΩ) to *R5* (340.2 kΩ). To examine the switching property of the H-diamond logic circuits, the pulse response characteristics are investigated, and the result is shown in Fig. 14(e). When the input signal is kept at a high level of –10.0 V, the output response signal is measured to be 0 V. However, when the input signal

is kept at a low level of 0 V, the output response signal is close to the V_{DD} value of –10.0 V. Thus, the pulse response signal provides the inversion property between V_{in} and V_{out}.

4.2 Enhancement-mode MOSFET/load resistor NOR logic circuit

Figures 15(a) and 15(b) show the top view and schematic diagram of the H-diamond MOSFET NOR logic circuit, respectively [23]. The circuit is composed of two enhancement-mode SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOSFETs and a load resistor. The V_{in1} and V_{in2} represent two input voltages. The W_G and L_G for the enhancement-mode SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOSFETs are kept at 100 and 2 µm, respectively. Interspaces between the different electrodes for V_{in}-to-ground, V_{in}-to-V_{out}, and V_{in}-to-V_{DD} are 1.5, 2, and 26 µm, respectively.

Figure 15(c) shows V_{out} as functions of V_{in1} and V_{in2} for the H-diamond MOSFET NOR logic circuit. There are four logic states for the input voltages: (1, 1), (1, 0), (0, 1), and (0, 0). For each input voltage, the measurement time is 60 s. If both V_{in1} and V_{in2} are −10.0 V, the input voltages are in the logical (1, 1) state, and the two enhancement-mode MOSFETs operate in the on state. There is a large current across the load resistor, leading to a significant decrease in V_{DD}. The V_{out} responds close to 0 V and at the logical 0 state. If one V_{in} is −10.0 V and the other is 0 V, the input voltage is in the logical (1, 0) or (0, 1) state. In this case, only one enhancement-mode MOSFET operates in the on state. The V_{out} responds close to 0 V and at the logical 0 state. If both V_{in1} and V_{in2} are 0 V, the input voltages are at a logical (0, 0) state. Two enhancement-mode MOSFETs operate in the off state, and there is no current across the load resistor. The V_{out} responds close to V_{DD} of −10.0 V and at the logical 1 state. Therefore, when one or both input voltages are "high" signals, the output voltages respond with "low" signals. When both input voltages are "low" signals, the output voltage responds with a "high" signal. These results indicate that our logic circuits operate with NOR characteristics.

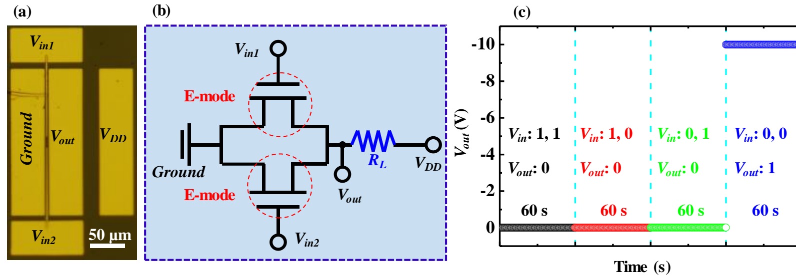

Fig. 15. (a) and (b) Top view and schematic diagram of the H-diamond MOSFET NOR logic circuit, respectively. The circuit is composed of two E-mode MOSFETs and a load resistor, R_L. (c) V_{out} as functions of four logic states of V_{in}: (1, 1), (1, 0), (0, 1), and (0, 0).

4.3 Enhancement-/depletion-mode H-diamond MOSFET NOT logic circuits

Figures 16(a) and 16(c) show the top view and schematic diagram of the enhancement-/depletion-mode H-diamond MOSFET NOT logic circuit, respectively. The circuit is composed of a depletion-mode MOSFET and an enhancement-mode MOSFET [22]. The depletion- and enhancement-mode MOSFETs for the NOT logic circuits act as load and driver devices, respectively. The distance between source and drain electrodes for both Al_2O_3/H-diamond and SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOSFETs is the same, 5.5 μm; however, their gate lengths are 3 and 2 μm, respectively. The gate-to-source and gate-to-drain interspaces for the Al_2O_3/H-diamond MOSFET are 1.2 and 1.3 μm, and those for the $LaAlO_3$/Al_2O_3/H-diamond MOSFET are 1.5 and 2 μm, respectively. Although both MOSFETs have the same device structures, the L_G and interspaces of gate-to-source/drain are different. This is possibly attributed to the positioning accuracy for the laser lithography system, ± 1.0 μm.

Figure 16(c) shows the VTCs of the H-diamond NOT logic circuit with the V_{DD} changing from −5.0 to −25.0 V. There are distinct inversion characteristics for the NOT logic circuit. If the V_{in} is 0 V, the enhancement-mode SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOSFET operates in the off state, resulting in a V_{out} close to V_{DD}. If the V_{in} is −10.0 V, the enhancement-mode MOSFET turns on, resulting in a V_{out} close to the ground level. Thus, when the V_{in} operates with a low signal and at the logical 0 state, the V_{out} responds with a high signal and at the logical 1 state. Likewise, when the V_{in} operates with a high signal and logical 1 state, the V_{out} responds with a low signal and logical 0 state. The gain curve defined by $-dV_{out}/dV_{in}$ can be determined, as shown in Fig. 16(d). The maximum gain value increases from 1.2 to 26.1 with the V_{DD} changing from −5.0 to −25.0 V.

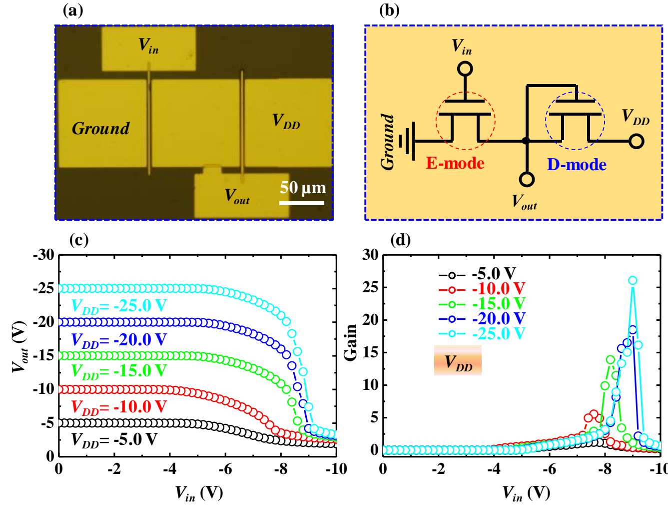

Fig. 16. (a) and (b) Top view and schematic diagram for the enhancement-/depletion-mode H-diamond MOSFET NOT logic circuit. (c) VTCs of the H-diamond MOSFET NOT logic circuit with the V_{DD} changing from −5.0 to −25.0 V, and (d) the gain curve ($-dV_{out}/V_{in}$) derived from the VTCs.

4.4 Enhancement-/depletion-mode MOSFET NOR logic circuit

Figures 17(a) and 17(b) show the top view and schematic diagram of the H-diamond MOSFET NOR logic circuit, respectively [22]. The structures for the MOSFETs are the same as those for the NOT logic circuit. V_{in1} and V_{in2} represent two input voltages for the NOR logic circuit, which is composed of a depletion-mode MOSFET and two enhancement-mode devices.

Figure 17(c) shows the V_{out} signal of the H-diamond MOSFET NOR logic circuit for four different V_{in} signals at $V_{DD} = -10.0$ V. For each signal, the measurement time is 60 s. If both V_{in1} and V_{in2} are −10.0 V [logical (1, 1) state], both enhancement-mode MOSFETs work in the on states. The current across the depletion-mode MOSFET equals the total I_{DS} for the two enhancement-mode MOSFETs, which leads to a significant decrease in V_{DD} and a V_{out} of -0.9 ± 0.1 V.

If the V_{in1} and V_{in2} are −10.0 and 0 V [logical (1, 0) state], respectively, only one enhancement-mode MOSFET works in the on state. The current across the depletion-mode MOSFET is lower than that for the logical (1, 1) state, resulting in a higher absolute V_{out} of -1.9 ± 0.1 V. If the V_{in1} and V_{in2} are 0 and −10.0 V [logical (0, 1) state], respectively, the V_{out} is also -1.9 ± 0.1 V, indicating that the electrical properties for both enhancement-mode MOSFETs are consistent. If both V_{in1} and V_{in2} are 0 V [logical (0, 0) state], both the enhancement-mode MOSFETs work in the off states. Then, no current flows across the depletion-mode MOSFET, and the V_{out} is close to the V_{DD} of −10.0 V. Thus, when one or both input voltages operate with a high signal and logical 1 state, the V_{out} responds with a low signal and logical 0 state. Likewise, when both input voltages operate with low signals and logical 0 state, the V_{out} responds with a high signal and logical 1 state. These results indicate that our logic circuit acts with the NOR gate characteristics.

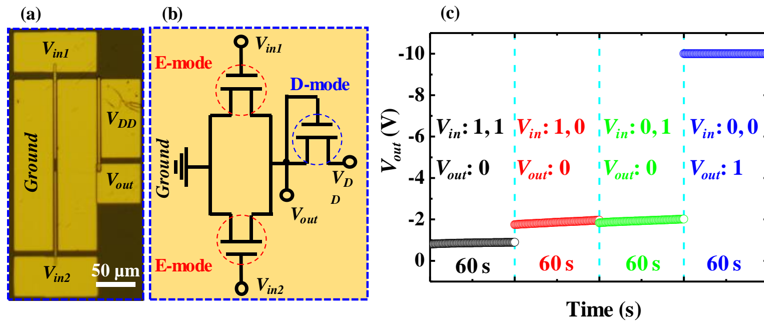

Fig. 17. (a) and (b) Top view and schematic diagram of the enhancement-/depletion-mode H-diamond MOSFET NOR logic circuit, respectively. (c) V_{out} as functions of four logic states of V_{in}: (1, 1), (1, 0), (0, 1), and (0, 0).

5. Conclusion

In this chapter, we review our recent progress in the fabrication and characterization of the H-diamond MOS capacitors, MOSFETs, and MOSFET logic circuits. Investigations for the *J* and *C-V* properties of the H-diamond MOS capacitors are necessary to help determine the optimal oxide insulator for H-diamond-based MOS devices. Studies for the planar-type, T-type, and triple-gate fin-type H-diamond MOSFETs help reveal the underlying defects in the device structures and assist with their improvement. The fabrication of depletion- and enhancement-mode H-diamond MOSFETs and the H-diamond MOSFET logic circuits may help promote the development of diamond complementary MOS integrated circuit chips.

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