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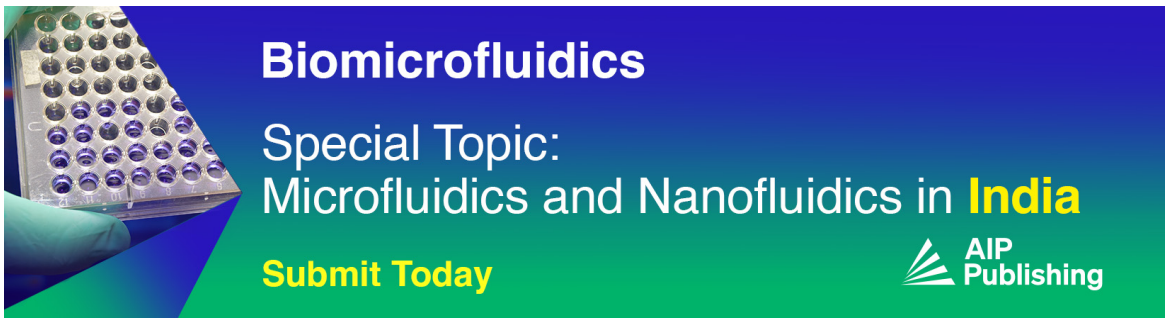

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Progress and challenges in the development of ultra-wide bandgap semiconductor α-Ga_2O_3 toward realizing power device applications

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ABSTRACT

Ultra-wide-bandgap (UWBG) semiconductors, such as Ga_2O_3 and diamond, have been attracting increasing attention owing to their potential to realize high-performance power devices with high breakdown voltage and low on-resistance beyond those of SiC and GaN. Among numerous UWBG semiconductors, this work focuses on the corundum-structured α-Ga_2O_3, which is a metastable polymorph of Ga_2O_3. The large bandgap energy of 5.3 eV, a large degree of freedom in band engineering, and availability of isomorphic p-type oxides to form a hetero p–n junction make α-Ga_2O_3 an attractive candidate for power device applications. Promising preliminary prototype device structures have been demonstrated without advanced edge termination despite the high dislocation density in the epilayers owing to the absence of native substrates and lattice-matched foreign substrates. In this Perspective, we present an overview of the research and development of α-Ga_2O_3 for power device applications and discuss future research directions.

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I. INTRODUCTION

Given the strong demand to suppress CO_2 emissions and save energy, it is urgent to promote efficient energy consumption along with the use of reusable energy sources. It is essential to reduce energy loss in power converters to efficiently utilize electrical energy. Power converters are used in virtually all electrical equipment. Currently, most power converters employ power devices based on Si semiconductors. However, their efficiency is close to the material limit. The use of wide bandgap semiconductors is a promising method to exceed the Si limit. This is because the on-resistance (R_{on}) of a drift layer in a power semiconductor device is inversely proportional to the cube of the critical field for breakdown (E_C), and E_C tends to increase with the increase in bandgap energy E_g, as shown in Fig. 1.[1] Accordingly, R_{on} of a drift layer is expressed as

$$R_{on} = \frac{4V_B^2}{\varepsilon\mu E_c^3}, \quad (1)$$

where V_B indicates the break down voltage, ε symbolizes relative dielectric constant, and μ corresponds to electron mobility. The denominator $\varepsilon\mu E_c^3$ is referred to as Baliga's figure of merit (BFOM).[2] The BFOM indicates how small R_{on} can be in principle. Table I summarizes the material properties and BFOM of the selected semiconductors. For instance, the BFOM of 4H–SiC is 340, which implies that R_{on} of a 4H–SiC device can be 1/340 of that of Si. It is worth mentioning that intrinsic experimental values of ε, μ, and E_c for α-Ga_2O_3 are unavailable at the moment. Among existing wide bandgap semiconductors, 4H–SiC and GaN are the most well-developed materials for power device applications, and these devices have gradually penetrated the market.

α-Ga_2O_3, the target material of this study, has a larger E_g than those of 4H–SiC and GaN, and as a result, a higher E_c can be expected. The first-principles calculations indicate that the energy gap should be indirect.[6,7] Moreover, α-Ga_2O_3 can be grown on isomorphic sapphire (α-Al_2O_3), of which large-scale wafers are commercially available at a reasonable price. Moreover, α-Ga_2O_3 has a large degree of freedom in band engineering and conductivity control owing to an abundance of corundum-structured oxides, and it is relatively easy to create solid solutions with them. Additionally, α-Ga_2O_3 is a potential candidate for solar-blind UV detectors because $E_g = 5.3$ eV corresponds to $\lambda = 238$ nm, which is shorter than the shortest wavelength of the solar spectrum on the surface of the Earth. Herein, we present an overview

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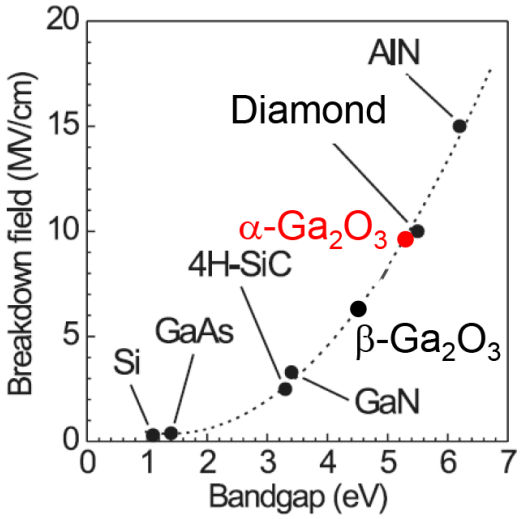

FIG. 1. Bandgap dependence of E_c. Reproduced with permission from Higashiwaki *et al.*, Appl. Phys. Lett. **100**, 013504 (2012). Copyright 2012 AIP Publishing.[1]

of the α-Ga_2O_3-related technologies and discuss future perspectives by focusing on power device applications. Regarding UV applications, a comprehensive review was conducted by Biswas and Nishinaka.[8]

II. MATERIAL PROPERTIES AND POTENTIAL FOR POWER DEVICE APPLICATIONS OF α-Ga_2O_3

Ga_2O_3 crystalizes into five different structures.[9,10] Among the Ga_2O_3 polymorphs, the corundum-structured α-phase is the second most well developed material for semiconductor device applications, next to the most thermally stable β-phase. In addition to the largest E_g among the Ga_2O_3 polymorphs, α-Ga_2O_3 exhibits several advantages. First, there are many corundum-structured oxides, as illustrated in Fig. 2, and α-Ga_2O_3 can be used to create solid solutions.[11] Therefore, α-Ga_2O_3 has a higher degree of freedom for band engineering, and it may even be possible to provide multi functionality. For instance, α-$(Al_xGa_{1-x})_2O_3$ can be grown without a compositional limitation[12–14] compared to the case of β-Ga_2O_3, and E_g can be controlled over a wide range (Fig. 3). As depicted in Fig. 3, the E_g of α-$(Al_xGa_{1-x})_2O_3$ can be increased to 8.8 eV, which cannot be reached by

TABLE I. Material properties and BFOM of semiconductors. The values are from Ref. 3 except those for α-Ga_2O_3.

	Si	4H–SiC	GaN	β-Ga_2O_3	α-Ga_2O_3	Diamond
Eg (eV)	1.1	3.3	3.4	4.5	5.3	5.5
ε	11.8	9.7	9	10	12.8[a]	5.5
μ (cm^2/V s)	1400	1000	1200	200	200[b]	2000
EC (MV/cm)	0.3	2.5	3.3	6.5	9.5[c]	10
BFOM (vs Si)	1	340	870	1231	4921	24 661

[a]Theoretical value obtained via first-principles calculations.[4]
[b]Assumed to be the same as that for β-Ga_2O_3. The highest reported value for α-Ga_2O_3 is 65 cm^2/V s.[5]
[c]Expected value from the empirical curve shown in Fig. 1.

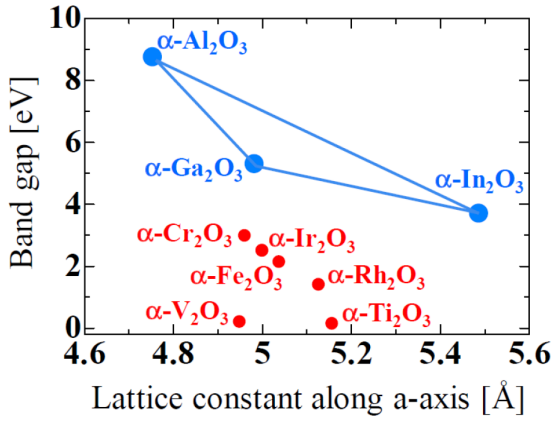

FIG. 2. Relationship between the bandgap and lattice constant along the *a*-axis of corundum-structured oxides. Reproduced with permission from Kaneko *et al.*, Jpn. J. Appl. Phys., Part 1 **57**, 02CB18 (2018). Copyright 2018 The Japan Society of Applied Physics.[11]

β-$(Al_xGa_{1-x})_2O_3$, indicating a possibility for the realization of further high-performance power devices beyond α-Ga_2O_3. In particular, nearly defect-free devices can be fabricated when the Al content is sufficiently high to enable the growth of coherently strained α-$(Al_xGa_{1-x})_2O_3$ on sapphire. Ferromagnetism can be formed by alloying with α-Fe_2O_3.[15] Second, isomorphic p-type oxides with relatively small lattice mismatch (<0.3%), such as α-$(Ga_xIr_{1-x})_2O_3$ and α-$(Ga_xRh_{1-x})_2O_3$,[11] can be

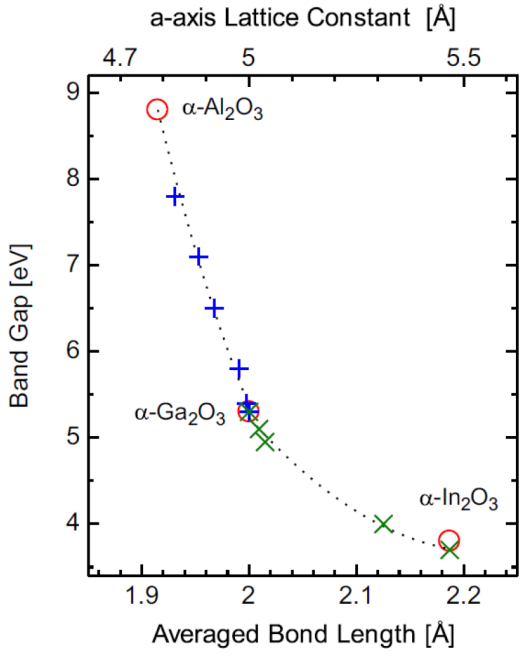

FIG. 3. Bandgap energy in terms of averaged bond length/lattice constant along the *a*-axis of α-$(Al_xGa_{1-x})_2O_3$ and α-$(In_xGa_{1-x})_2O_3$. Reprinted with permission from S. Fujita and K. Kaneko, J. Cryst. Growth **401**, 588–592 (2014). Copyright 2014 Elsevier.[12]

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utilized to create a hetero-p–n junction[16–18] unlike the case of β-Ga_2O_3. Recently, Zhang *et al.* reported a β-Ga_2O_3 hetero-p–n-junction diode using NiO as the p-type layer, and the performance surpassed the material limits of SiC and GaN despite the crystal structure difference between β-Ga_2O_3 and NiO.[19] This fact may mean that the necessity for matching the crystal structure and lattice parameters is debatable. Another advantage is that a single-crystalline α-Ga_2O_3 film can be grown on a large-scale using cost-effective sapphire substrates. However, the dislocation density in the epilayer is extremely high if countermeasures are not taken. The crystal plane of the epilayer can be controlled by the choice of the crystal plane of sapphire. In the case of β-Ga_2O_3, a β-Ga_2O_3 film can also be grown heteroepitaxially. However, the crystal plane is virtually limited to $(\bar{2}01)$, on which stacking faults are readily formed, and the epilayer includes in-plane rotational domains[20] although such domains can be suppressed to a certain degree by growing films on off-angled substrates.[21] Therefore, an expensive singe crystal β-Ga_2O_3 substrate needs to be used even if the epilayer does not have to be of ultra-high quality.

The major drawbacks of α-Ga_2O_3 are as follows. First, the dislocation density in an epilayer is extremely high because of the absence of native α-Ga_2O_3 and lattice-matched foreign substrates. Moreover, the use of foreign substrates (sapphire in most cases) results in the bowing and cracking of the epi-wafer caused by thermal stress owing to the difference in the thermal expansion coefficients. Additionally, α-Ga_2O_3 epilayers grown on insulating sapphire substrates require a complicated fabrication process to produce vertical-structured devices. Second, α-Ga_2O_3 is a metastable phase, which turns to the β-phase at high temperatures of approximately 550 °C or higher.[22] Therefore, damage recovery by thermal annealing would be difficult even if ion implantation is performed. Fortunately, thermal annealing of electrodes should not be problematic, because optimal contact performance can be achieved below the transition temperature, and thermal treatment at higher temperatures degrades contact performance, similar to that of β-Ga_2O_3.[23,24] Interestingly, the transition temperature tends to increase as the film thickness decreases, as shown in Fig. 4.[25] Moreover, it has been reported that the transition initiates from the film surface.[25] Under ultra-high pressure, α-Ga_2O_3 is thermodynamically the most stable among the Ga_2O_3 polymorphs.[26] The increased thermal stability of thin α-Ga_2O_3 films is most likely caused by the compressive strain owing to the lattice mismatch, which effectively stabilizes the α-phase. Formation of a capping layer on the surface of an α-Ga_2O_3 film effectively increases the thermal stability.[27] McCandless reported that the transition temperature of a 57-nm-thick α-Ga_2O_3 with a capping layer of SiO_2 or Mo increased to ~800 °C while that of the control sample without a capping layer was ~600 °C.[27] Capping with a crystalline Al_2O_3 layer further increased the transition temperature to ~900 °C, which can be attributed to the thermal diffusion of Al into the underlying α-Ga_2O_3 layer. Thus, alloying with α-Al_2O_3 dramatically increases the thermal stability. Jinno *et al.* clarified the Al composition dependence of thermal stability of *c*-plane α-$(A_xGa_{1-x})_2O_3$ films.[28] As displayed in Fig. 5, the transition temperature is 650 °C when $x = 0$, which increases to 950 °C when $x = 0.45$. No transition was observed when $x > 0.6$, even after annealing at 1100 °C. Hence, ion implantation and the following thermal annealing for damage recovery may be possible in high-Al-composition films. Third, thermal conductivity of α-Ga_2O_3 should be low, which in principle would have an adverse impact on heat dissipation from power

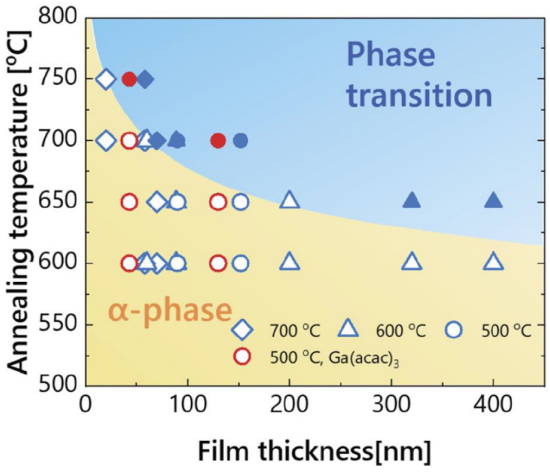

FIG. 4. Thermal stability of α-Ga_2O_3 films as a function of the film thickness. Open symbols indicate samples that maintained the α-phase. The solid symbols indicate samples that completely converted to the β-phase. Samples drawn in red and blue colors were grown using $Ga(acac)_3$ and $GaCl_3$ as a Ga precursor. The circular, triangular, and rhomboid symbols illustrate the growth temperature of 500, 600, and 700 °C, respectively. Reproduced with permission from Jinno *et al.*, AIP Adv. **10**, 115013 (2020). Copyright 2020 AIP Publishing.[25]

devices. Although experimental thermal conductivities of α-Ga_2O_3 have not been reported, Yang *et al.* theoretically estimated the thermal conductivities up to 800 K, as displayed in Fig. 6, by combining the first principles calculation and iteratively solving the Boltzmann transport equation.[29] Based on their calculation, the thermal conductivities should be 11.61 W/mK along [100], 9.38 W/mK along [010], and 8.04 W/mK along [001], which are considerably lower than those of GaN (210 W/mK[30]) and 4H–SiC (347 W/mK[31]). Note that the experimental thermal conductivity of β-Ga_2O_3 is the highest along [010]

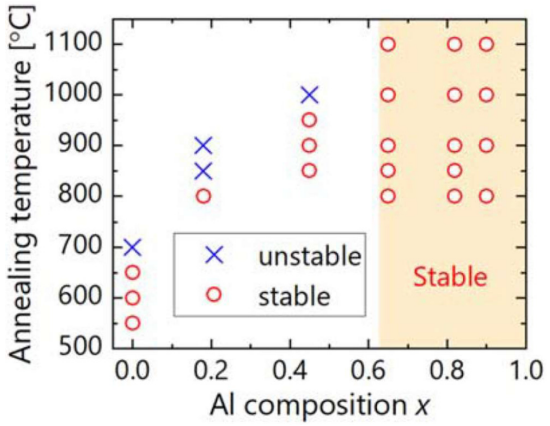

FIG. 5. Thermal stability of the *c*-plane α-$(A_xGa_{1-x})_2O_3$ films as a function of the Al composition. The blue crosses illustrate the samples that converted to the β-phase while the red circles represent the samples that maintained the α-phase. Reproduced with permission from Jinno *et al.*, Jpn. J. Appl. Phys., Part 1 **60**, SBBD13 (2021). Copyright 2021 The Japan Society of Applied Physics.[28]

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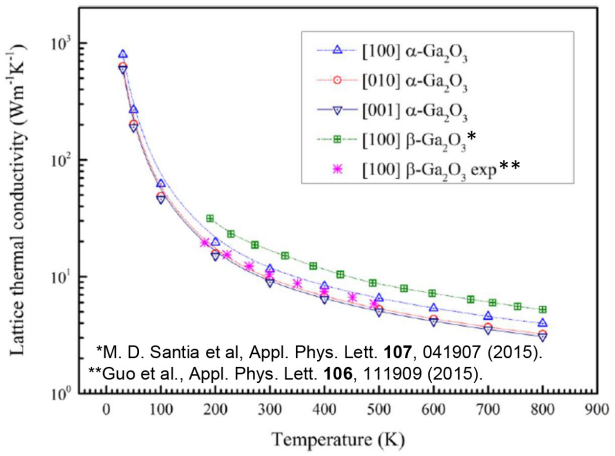

FIG. 6. Calculated lattice thermal conductivity of α-Ga_2O_3 as a function of the temperature. Calculated and experimental values for β-Ga_2O_3 are also shown for comparison. Reproduced with permission from Yang *et al.*, J. Vac. Sci. Technol. A **40**, 052801 (2022). Copyright 2022 The American Vacuum Society (AVS).[29]

(27 W/mK) and lowest along [010] (10.9 W/mK).[32] The low thermal conductivity is a common problem associated with Ga_2O_3.

III. EPITAXY

The development of epitaxial growth methods is essential for realizing high-performance α-Ga_2O_3 power devices. Epitaxial growth of α-Ga_2O_3 has been primarily investigated via mist chemical vapor deposition (mist CVD), halide vapor phase epitaxy (HVPE), molecular beam epitaxy (MBE), and metalorganic vapor phase epitaxy (MOVPE). A wide range of growth temperatures (350–880 °C) have been reported because the thermal stability of α-$(Al_xGa_{1-x})_2O_3$ depends on the film thickness and Al composition, as described in Sec. II. In this section, we present an overview of the current situation of these growth methods and then discuss detailed technical aspects such as substrates, conductivity control, and defect control.

A. Growth methods

1. Mist CVD

In this method, an aqueous solution containing a gallium source, such as gallium (III) acetyl acetonate or $GaCl_3$, is atomized via ultrasonic vibration.[34,35] Subsequently, the mist is transferred to the reactor together with a carrier gas, such as N_2 or O_2, and α-Ga_2O_3 is grown on a substrate by exploiting the chemical reaction between the gallium source and H_2O or O_2. The method realized the first epitaxial growth of α-Ga_2O_3.[34] The growth conditions have been well established to grow phase-pure α-Ga_2O_3 epilayers. Moreover, μm-order-thick films can be grown at a typical growth rate of approximately 1 μm/h. Additionally, it is possible to grow solid solutions such as α-$(Al_xGa_{1-x})_2O_3$,[12] and the growth of α-$(Al_xGa_{1-x})_2O_3$/α-$(Al_yGa_{1-y})_2O_3$ super lattice was demonstrated.[36]

Residual impurity concentrations in mist-CVD-grown α-Ga_2O_3 tend to be high. For instance, Uno *et al.* reported that their UID film included H, C, and Si at following concentrations: $[H] = 2 \times 10^{19}\,cm^{-3}$, $[C] = 7 \times 10^{17}\,cm^{-3}$, and $[Si] = 3 \times 10^{18}\,cm^{-3}$.[37] Plausible sources of H, C, and Si include H_2O, quartz (SiO_2), and acetylacetone, respectively. SiO_2 and a high concentration of H_2O could react with each other at high temperatures to release Si-included species as contaminants. Therefore, it is essential to establish a technique to suppress the residual impurities to grow a drift layer for a high- V_B device. Note that it is occasionally stated that the mist-CVD growth apparatus is cost-effective than those of metalorganic chemical vapor deposition (MOCVD) or halide vapor phase epitaxy (HVPE). However, this is probably based on the lab-level simple structure of the mist-CVD apparatus. If an industry-level apparatus with gas lines for multiple growth precursors and dopants is fully equipped with appropriate components, such as an optimized laminar flow channel, mass-flow controllers, air-operated valves, programmable logic controllers, and an exhaust system, the machine cost would be comparable to those of MOCVD or HVPE.

2. HVPE

In this method, α-Ga_2O_3 is grown using $GaCl_x$ and O_2 as precursors.[38–40] $GaCl_x$ ($x = 1$ or 3) is produced upstream in the reactor in the chemical reaction involving Ga and HCl/Cl_2 (hereinafter denoted as HCl-HVPE[38,39] and Cl_2-HVPE,[40] respectively). Rapid growth is one of the most attractive points of HVPE. In the case of HCl-HVPE, the growth rate exceeds 100 μm/h when $GaCl_3$ and O_2 are used as the precursors, as illustrated in Fig. 7.[39] Such a high growth rate is beneficial for growing a thick α-Ga_2O_3 film for a drift a layer or freestanding α-Ga_2O_3 wafer. To date, there have been no reports on the HVPE of α-$(Al_xIn_yGa_{1-x-y})_2O_3$ solid solutions. However, it should be possible because the HVPE of In_2O_3 has already been demonstrated,[41] and the supply of $AlCl_3$ is a well-established technique in the HVPE of AlN.[42]

The most major impurities in HCl-HVPE-grown UID α-Ga_2O_3 include H and Cl, and the concentrations tend to increase at high growth rates. For instance, in our case, [H] is below the detection limit of SIMS measurement ($5 \times 10^{16}\,cm^{-3}$), and [Cl] is typically $5 \times 10^{16}\,cm^{-3}$ at a growth rate of 15 μm/h. When the growth rate was increased to 100 μm/h, [H] and [Cl] increased to 2.8×10^{17} and $1.4 \times 10^{18}\,cm^{-3}$, respectively.[39] In β-Ga_2O_3, Cl is theoretically

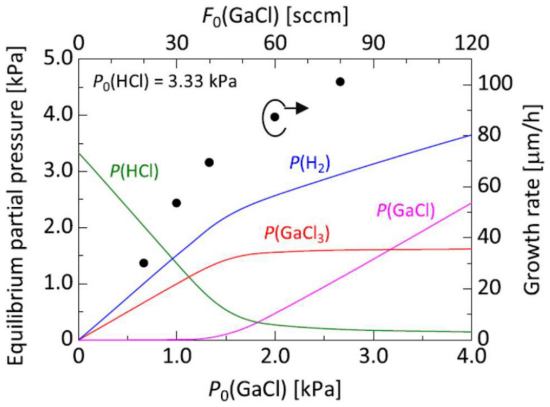

FIG. 7. HVPE growth rate of α-Ga_2O_3 as a function of the GaCl supply vapor pressure under an additional HCl supply to convert GaCl–$GaCl_3$. The O_2 supply was fixed at 3.125 kPa. The calculated equilibrium vapor pressures of H_2, HCl, GaCl, and $GaCl_3$ are also displayed. The calculated results reveal that GaCl should be effectively converted to $GaCl_3$. Reproduced with permission from Oshima *et al.*, Semicond. Sci. Technol. **35**, 055022 (2020). Copyright 2020 IOP Science.[39]

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predicted to be a shallow donor.[43] It is likely that Cl is a shallow donor in α-Ga_2O_3 despite the lack of theoretical calculations. In reality, HVPE-grown UID α-Ga_2O_3 films are highly resistive, and n-type conduction owing to Cl impurity has not been reported yet. Extended research is required to clarify whether Cl in α-Ga_2O_3 is inactive or just compensated. The background Si concentration is below the detection limit of SIMS measurement ($\leq 10^{15}$ cm^{-3}), even at a growth rate of 100 μm/h, despite the existence of H_2 (by-produced by the reaction of Ga and HCl) in the quartz reactor tube probably owing to the low growth temperature.

3. MBE

In this method, α-Ga_2O_3 is grown using gallium vapor flux and plasma-activated oxygen (presumably atomic oxygen) as precursors. α-$(Al_xGa_{1-x})_2O_3$ can be grown across the entire compositional range.[13] In the case of MBE, there is a critical thickness beyond which the film is contaminated by the β-phase. There have been no previous reports on such critical thickness in the cases of mist CVD or HVPE. The critical thickness depends on the crystal plane. Reported maximum thicknesses for phase-pure MBE-grown α-Ga_2O_3 films are 3.3 nm for (0001),[44] 14.3 nm for $(11\bar{2}0)$,[44] 51 nm for $(10\bar{1}0)$,[13] and 217 nm for $(10\bar{1}2)$.[45]

Moreover, residual impurity concentrations in MBE-grown α-Ga_2O_3 have not been reported yet. In the case of β-Ga_2O_3, the primary residual donor is Si, which is believed to be originated from quartz parts used in the plasma cell.[46] It is likely that MBE-grown α-Ga_2O_3 exhibit a similar tendency.

4. MOVPE

MOVPE is a commonly utilized growth method in the III–V semiconductor industry. MOVPE has been applied to R&D of β-Ga_2O_3, and high-quality epilayers and promising device prototypes have been demonstrated.[47,48] More recently, MOVPE of phase-pure α-Ga_2O_3 was reported by Bhuiyan *et al.*[14] They grew a α-Ga_2O_3 film on $(10\bar{1}0)$ sapphire using trimethylgallium and O_2 as the precursors.[14] Moreover, they reported the growth of α-$(Al_xGa_{1-x})_2O_3$ in a full Al composition range using trimethylaluminum as the Al source.[14]

Residual impurities in MOVPE-grown α-Ga_2O_3 have not been reported yet. Generally, MOVPE-grown films tend to include carbon as a residual impurity, which originates from the metalorganic precursors. For example, the carbon concentration in MOVPE-grown UID GaN exhibits a tendency to increase as the growth temperature or V/III ratio decreases.[49] Depending on the growth condition, MOVPE-grown β-Ga_2O_3 includes carbon impurities. For example, Ikenaga *et al.* reported that the carbon concentration in their MOVPE-grown β-Ga_2O_3 film was below the detection limit (3×10^{16} cm^{-3}) when the growth temperature was 1000 °C; however, it increased to $\sim 1.5 \times 10^{18}$ cm^{-3} at 800 °C.[50] In the case of α-Ga_2O_3, the growth temperature is even lower (650 °C,[14] for instance). The low growth temperature can suppress the combustion of hydrocarbon and enhance the incorporation efficiency of carbon impurity, resulting in a higher carbon concentration in the crystal.

B. Substrates

Sapphire, synthetic mica[51] $LiNbO_3$, and $LiTaO_3$[52] have been reported as potential substrates for α-Ga_2O_3. Among them, sapphire is the only realistic choice for industrial use at present owing to its isomorphic structure and availability of large-diameter and high-quality wafers at a reasonable price. Moreover, α-Ga_2O_3 can be grown on various crystal planes of sapphire such as (0001), $(11\bar{2}0)$, and $(10\bar{1}0)$. Higher electron mobility has been reported in *m*-plane films than in *c*-plane films[5] although it is unclear whether the difference is intrinsic or because of the crystal-orientation-dependent defect character/distribution.

C. Conductivity control

Group-IV elements, such as Si, Ge, and Sn, which substitute Ga sites, are used as shallow donors in α-Ga_2O_3, and the related doping techniques are well established. In the case of mist CVD, a dopant material, such as $SnCl_2$ or $ClSi(CH_3)_2((CH_2)_2CN)$, is dissolved in the aqueous solution of the growth precursors.[53,54] A previous study reported on n-type conductivity control via F doping.[55] In the case of HVPE, dopant gas sources, such as SiH_4 and $GeCl_4$, have been reported.[56,57] Moreover, electron mobility decreases at low carrier concentrations probably because of the scattering by dislocations.[5,56] Son *et al.* experimentally demonstrated that electron mobility increased as the dislocation density decreased (reflected to the FWHM of the x-ray rocking curve), as illustrated in Fig. 8.[56] Based on a theoretical estimation, the scattering by dislocations should be negligible even in the non-degenerated region when the dislocation density is less than 10^7–10^8 cm^{-2}.[59] Moreover, p-type conductivity control of α-Ga_2O_3 would be virtually impossible besides the case of β-Ga_2O_3, in which the causes of the difficulty are believed to be the absence of shallow acceptors, large effective hole mass, and formation of small polarons.[60] Fortunately, as mentioned in Sec. II, corundum-structured p-type oxides, such as α-$(Ga_xIr_{1-x})_2O_3$, with relatively small lattice mismatch are available to form a hetero-p–n junction.

IV. DEFECT CONTROL

A. Dislocations

In a conventional α-Ga_2O_3 film, the dislocation density is as high as 10^{10} cm^{-2} because of the lattice mismatch between α-Ga_2O_3 and

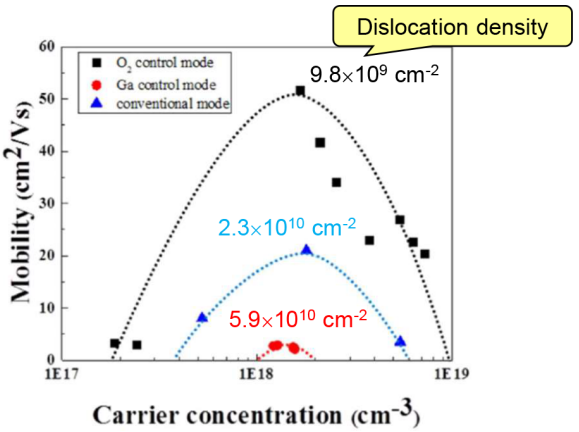

FIG. 8. Electron mobility as a function of the free electron density in HVPE-grown α-Ga_2O_3 films with different dislocation densities, reproduced with permission from of Son *et al.*, ECS J. Solid State Sci. Technol. **9**, 055005 (2020). Copyright 2020 IOP Science.[56] The dislocation densities were calculated based on the x-ray rocking curve widths by using a method described in Ref. 58.

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sapphire ($\Delta a/a$ ~4.5%, $\Delta c/c$ ~3.3%).[61,62] Among the dislocations, edge dislocations comprise the vast majority in many cases for *c*-plane α-Ga_2O_3 on sapphire. It is reflected to the broad FWHM of an x-ray rocking curve measured in skew-symmetric geometry while the FWHM is extremely narrow when measured in symmetric geometry, as depicted in Fig. 9. Accordingly, XRC measurements must be performed in both geometries to accurately estimate the mosaicity of the film. As mentioned in Sec. III, dislocations with such high density scatter electrons significantly to reduce the mobility. Accordingly, the dislocation density should be decreased to 10^7–10^8 cm^{-3} or less.[59] Note that the properties of crystal defects, including dislocations, grain boundaries, and stacking faults, are at the moment poorly understood for any phase of Ga_2O_3. Hence, the impact of dislocations on the electrical characteristics or device performance is probably not limited to the reduction in electron mobility. It is likely that dislocations in α-Ga_2O_3 also act as the current leak path or diffusion path for impurities.

Several techniques have been reported to decrease the dislocation density, including super lattice buffer layers,[36] use of patterned sapphire substrates (PSS),[63] and epitaxial lateral overgrowth technique (ELO).[35,62,64–66] Son *et al.* performed the HVPE of α-Ga_2O_3 on a PSS, and the dislocation density was reported to be 8.4×10^9 cm^{-2} while that in a control sample was 1.6×10^{10} cm^{-2}.[63] It is probably because of the lateral growth of α-Ga_2O_3 at the initial 3D-growth stage. However, the effect was limited because of the short period (~1 μm) of the pattern. Jinno *et al.* grew an α-Ga_2O_3 layer via mist CVD on a quasi-graded α-$(Al_xGa_{1-x})_2O_3$ super lattice buffer layer and obtained reduced screw and edge dislocation densities of 3×10^8 and 6×10^8 cm^{-2}, respectively.[36] Oshima *et al.* performed the ELO of α-Ga_2O_3 by HVPE and reported that the dislocation density was less than 5×10^6 cm^{-2} in the laterally over grown area on the mask (Fig. 10).[62] However, the dislocation density was still extremely high on the window areas because the dislocations in the seed layer propagated into the regrown α-Ga_2O_3 through the windows and reached the top surface. Additionally, a line of dislocations was newly formed at a coalesced boundary.[67] There are several strategies to solve the problem, which can be learned from the case of GaN. The modification of the mask pattern is one such method. The fraction of the defective area, i.e., window area and coalesced boundaries, can be decreased by making the mask width wider, and window width narrower. Thick film growth is another effective method.[68] During the thick film growth, dislocations with Burgers vectors of opposite signs attract each other to annihilate by making a dislocation loop, and dislocations with Burgers vectors of the same sign should disperse to uniformly distribute because of the repulsive interaction. Ma *et al.* demonstrated the reduction in the dislocation density by thick film growth in mist-CVD-grown α-Ga_2O_3, as illustrated in Fig. 11.[58] Combining the modification of the mask pattern and thick film growth will result in a better result. HVPE is a suitable growth method to shorten the time for thick film growth. Double ELO, in which the windows of the second mask are located to avoid the defective areas of the first ELO layer, is another plausible option;[65] however, it may not be cost effective because the process requires two cycles of photolithography and growth.

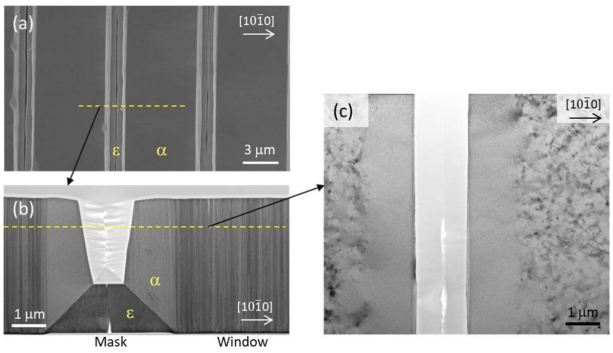

FIG. 10. SEM and TEM images of ELO-α-Ga_2O_3 stripes. (a) Plan-view SEM image, (b) cross-sectional TEM image, and (c) plan-view TEM image. Reproduced with permission from Oshima *et al.*, APL Mater. **7**, 022503 (2019). Copyright 2019 AIP Publishing.

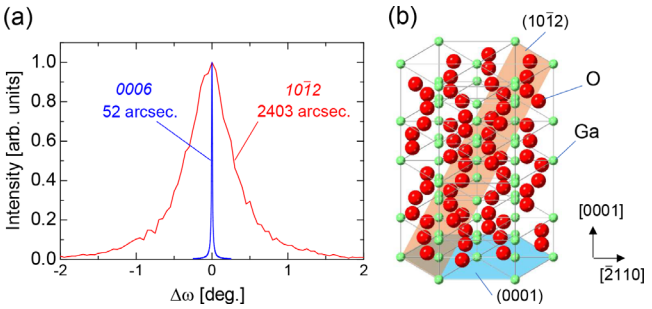

FIG. 9. (a) Typical x-ray rocking curves for 0006 and 10$\bar{1}$2 diffractions measured in symmetric and skew-symmetric geometries, respectively. Moreover, the FWHMs for 0006 and 10$\bar{1}$2 are illustrated. The sample was an HVPE-grown α-Ga_2O_3 film on (0001) sapphire. (b) Crystal structure of α-Ga_2O_3 showing (0001) and (10$\bar{1}$2) planes.

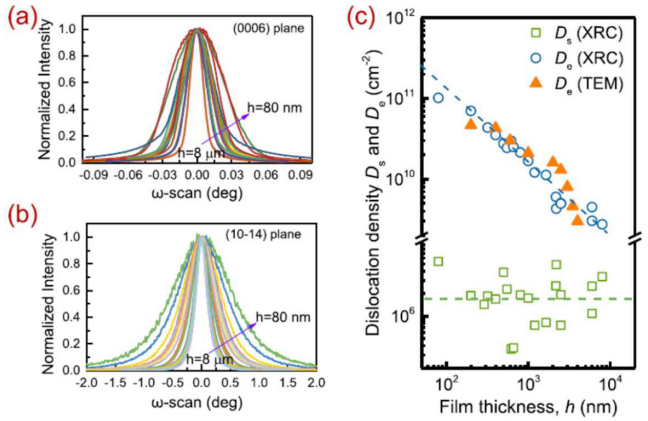

FIG. 11. (a) and (b) XRCs of 0006 and 10$\bar{1}$4 diffractions for α-Ga_2O_3 epilayers with different thicknesses, respectively, and (c) edge and screw dislocation densities (D_e and D_s, respectively), calculated based on XRCC-FWHMs as a function of the film thickness. The dashed line represents a least squares fit to the relationship of $D_e \propto 1/h$. Reproduced with permission from Ma *et al.*, Appl. Phys. Lett. **115**, 182101 (2019).Copyright 2019 AIP Publishing.[58]

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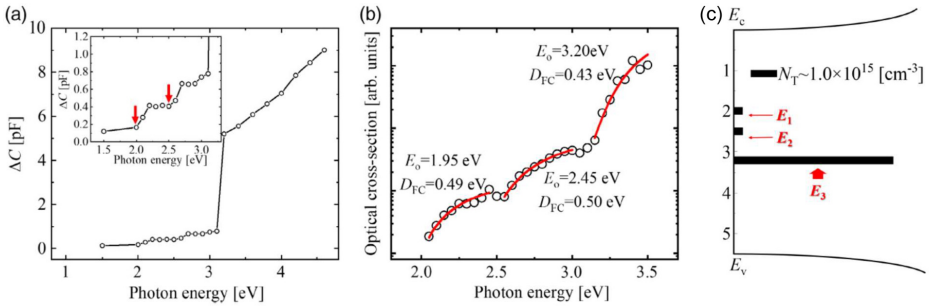

FIG. 12. (a) Relationship between ΔC and photon energy. The inset illustrates the enlarged view. (b) The optical cross section and the fitting results using the Pässler model (red lines). (c) Distribution of deep traps in the bandgap and their concentration. Reproduced with permission from Takane *et al.*, Phys. Status Solidi B **258**, 2000622 (2021). Copyright 2021 Wiley.

B. Deep levels

Deep levels significantly impact device performance through the trapping and releasing of carriers. Hence, it is essential to comprehend what type of traps exist, their origins, how they affect device performance, and how the density can be controlled. Some reports discuss the theoretical and experimental investigations of deep levels in α-Ga_2O_3, although the number of the reports is limited compared to that of β-Ga_2O_3. Koayashi *et al.* reported the formation energies of native point defects [vacancies (V_{Ga} and V_O), interstitials, and vacancy pairs] and charge transition levels of the native point defects in α-Ga_2O_3 based on first-principle calculations.[7] Experimental investigations have been conducted by means of deep-level transient spectroscopy (DLTS), deep-level optical spectroscopy (DLOS), photocapacitance, and photoinduced current.[69–71] For instance, Takane *et al.* investigated the deep levels in a mist-CVD-grown UID α-Ga_2O_3 film on $(10\bar{1}0)$ sapphire via DLOS and photocapacitance.[71] Consequently, three types of deep levels, namely, E_1 (CBM–2.0 eV, 3.5×10^{14} cm^{-3}), E_2 (CBM–2.5 eV, 3.6×10^{14} cm^{-3}), and E_3 (CBM–3.2 eV, 6.2×10^{15} cm^{-3}), were detected, as illustrated in Fig. 12, where CBM refers to conduction band minimum. Takane *et al.* compared their results with the theoretical calculations of Kobayashi *et al.*[7] and found that E_3 is likely to originate from V_{Ga} or V_{Ga}–V_O complex. Refer to the excellent review by Polyakov *et al.* for more details and other reports.[72]

V. DEVICES

A. SBDs

α-Ga_2O_3-based SBDs have been primarily reported by the groups of Kyoto University and FLOSFIA, Inc.[33,73–75] As depicted in Fig. 13, the research group fabricated vertical-structured SBDs (GaO™ SBD) by transferring a mist-CVD-grown α-Ga_2O_3 film on a metal substrate with high thermal conductivity.[73] Unfortunately, the details of the transfer process have not been disclosed. However, it should be noted that the mechanical bonding strength between an α-Ga_2O_3 film and a sapphire substrate is relatively weak, and the film can be easily separated from the substrate via thermal stress when the film is thicker than approximately 5 μm. It is likely that this feature is beneficial for the transfer process. The SBDs comprises a simple planar structure without guarding layers and passivation layers. The R_{on} and V_B were 0.1 mΩ cm^2 and 531 V for one of the SBDs (SBD1), and 0.4 mΩ cm^2 and 855 V for another SBD (SBD2), respectively. The R_{on} of SBD1 is approximately 1/7 of a commercially available SiC SBD and beyond the SiC limit (Fig. 14). The relatively small thickness of the α-Ga_2O_3 layer (~10 μm) and the use of a metal substrate contributed to minimize the R_{on} as well as maximizing the heat dissipation. Consequently, an extremely low heat resistance of 2.7 °C/W, which is as low as that of a commercial SiC device, was reported even for an ampere-class SBD mounted in a standard TO220 package.[33] The reverse recovery characteristics of an ampere-class SBD were reported to be equivalent or even faster than SiC devices, as illustrated in Fig. 15.[33] Remarkably, it has been reported that the forward and reverse I–V characteristics of the α-Ga_2O_3-based SBDs were comprehensively explained by thermoionic and thermoionic field emission models, respectively, from 294 to 423 K, despite the high dislocation density.[75] The ideality factor was 1.03, and it was independent of the temperature through 294–423 K.[75] FLOSIA has been shipping engineering samples of their SBDs ($V_B = 600$ V, $I_{max} = 10$ A[77]) and PFC power supply boards for evaluation. Table II lists the specifications of the PFC power supply board.[78] Figure 16 depicts the PFC power supply board combined with a DC–DC converter, in which α-Ga_2O_3-based SBDs are also used for driving an LED light.

B. PN diodes

Modulation doping based on a p–n junction is one of the most effective methods for improving V_B and R_{on}. Hence, it is necessary to clarify the characteristics of the α-$(Ir_xGa_{1-x})_2O_3$/α-Ga_2O_3 hetero p–n junction. Kan *et al.* fabricated a p–n junction diode using an

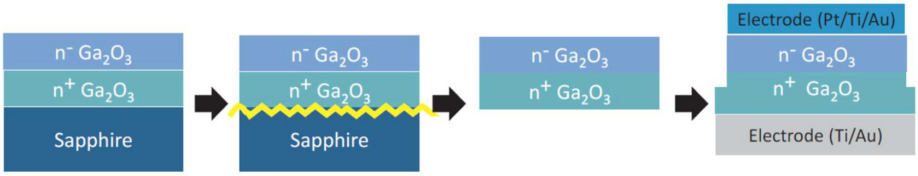

FIG. 13. Fabrication process of a GaO™ SBD. A thin α-Ga_2O_3 film is lifted off a sapphire substrate and transferred onto a supporting metal substrate. Reproduced with permission from Oda *et al.*, Appl. Phys. Express **9**, 021101 (2016). Copyright (2016) The Japan Society of Applied Physics.

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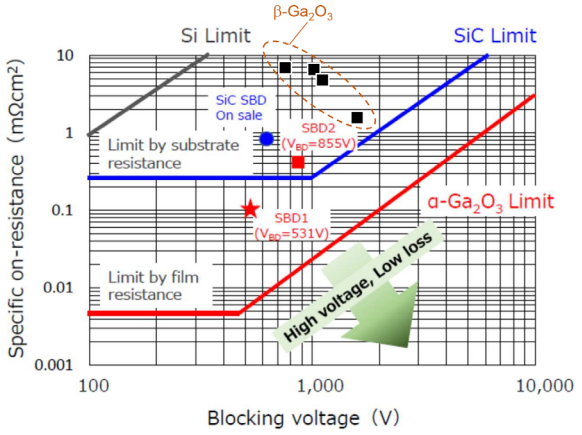

FIG. 14. Benchmarking of the GaO™ SBDs. Data for β-Ga_2O_3 vertical SBDs reported in Ref. 76 were added for comparison. Reproduced with permission from T. Shinohe, in *Proceedings of the International Power Electronics Conference (IPEC-Himeji 2022-ECCE Asia), Himeji, Japan* (IEEE, 2022), pp. 627–631. Copyright 2022 Institute of Electrical Engineers of Japan.[33]

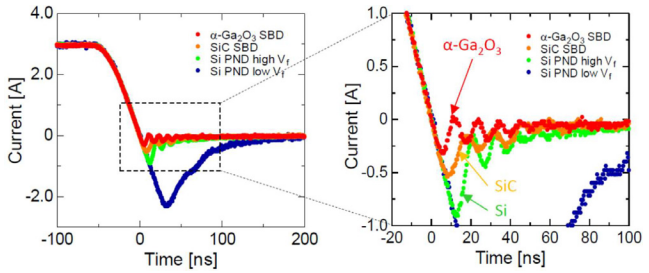

FIG. 15. Reverse recovery characteristics of an ampere-class GaO™ SBD. Reproduced with permission from T. Shinohe, in *Proceedings of the International Power Electronics Conference (IPEC-Himeji 2022-ECCE Asia), Himeji, Japan* (IEEE, 2022), pp. 627–631. Copyright 2022 Institute of Electrical Engineers of Japan.[33]

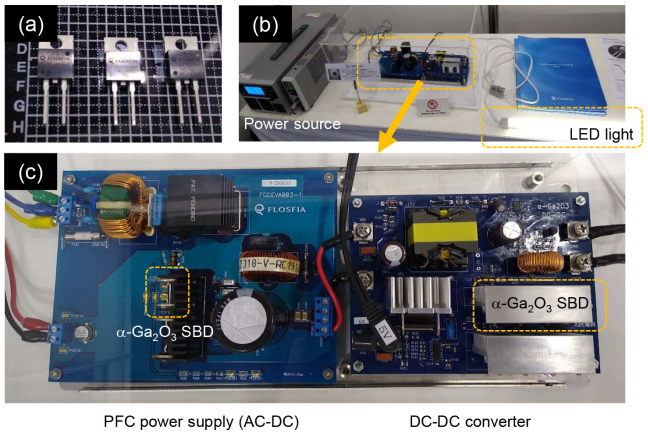

FIG. 16. Engineering samples displayed by FLOFIA at Techno-Frontier 2020 (July 20–22, 2022, Tokyo, Japan). (a) GaO™ SBDs mounted in standard TO-220 packages. (b) Evaluation boards driving an LED light. (c) Magnified image of the evaluation boards.

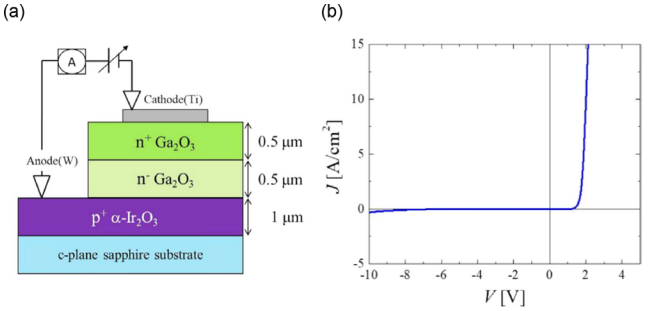

FIG. 17. (a) Schematic of the cross section of the α-Ir_2O_3/α-Ga_2O_3 hetero-p–n-junction diode. (b) *I–V* characteristics of the diode. Reproduced with permission of from Kan *et al.*, Appl. Phys. Lett. **113**, 212104 (2018). Copyright 2018 AIP Publishing.[16]

TABLE II. Specifications of the PFC power supply board.[78]

Item	Specification
Input voltage	AC 90–242 V (Max. 4 A@AC 100 V, 2 A@AC 200 V)
Input frequency	50–60 Hz
Bias voltage	DC 12 V
Output voltage	Typ. DC 390 V (Max. 0.9 A)
Output power	Max. 360 W (Max. 0.9 A)
Switching frequency	Variable (100–240 kHz, Typ. 120 kHz)

α-Ir_2O_3/α-Ga_2O_3 hetero structure and confirmed the rectifying *I–V* characteristics, as displayed in Fig. 17.[16] Moreover, they clarified the type-II band alignment of the junction by XPS, as shown in Fig. 18. The band offset for holes was as large as 4.7 eV.[16] Kaneko *et al.* investigated α-$(Ga_xIr_{1-x})_2O_3$ as a p-type layer to increase the bandgap and decrease the lattice mismatch and band offset.[18] When x was increased from 0 to 0.6, the bandgap increased from 3.0 to 4.2 eV, and the lattice mismatch decreased from 0.3% to 0.12%. Although the decrease in the band offset for holes has not been described in the report, it should decrease because the valence band maximum (VBM) decreased by ~1 eV, as illustrated in Fig. 19.[18] However, Mg doping was required to provide clear p-type conduction to the α-$(Ga_{0.6}Ir_{0.4})_2O_3$ layer despite the simultaneous increase in resistivity. The behavior was not straightforward. Further analysis is required to clarify the nature of α-$(Ga_xIr_{1-x})_2O_3$.

C. Field effect transistors (FETs)

The first report on a α-Ga_2O_3-based FET was by Dang *et al.* in 2015.[79] The MESFET was fabricated using a mist-CVD-grown Sn-doped (0001) α-Ga_2O_3 layer on sapphire with a AgO_x Schottky gate. The rectification ratio, V_B, and on-off ratio were 6×10^6, 19.6 V, and 2×10^7, respectively. More recently, an α-Ga_2O_3-based MOSFET with a V_B of 2.3 kV was reported.[80] The MOSFET with a HfO_2 gate was fabricated using an HVPE-grown Si-doped (0001) α-Ga_2O_3 layer on

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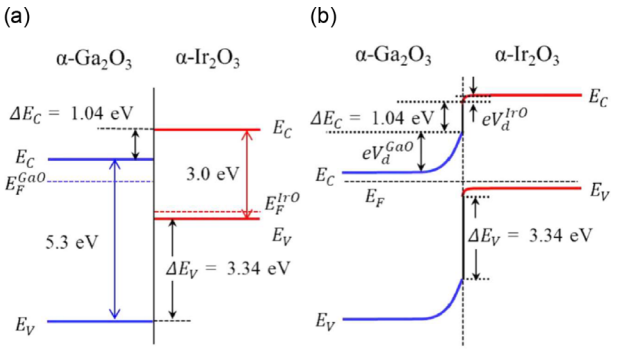

FIG. 18. Energy-band diagrams of (a) isolated α-Ir_2O_3 and α-Ga_2O_3. (b) α-Ir_2O_3/α-Ga_2O_3 hetero junction at thermal equilibrium. Reproduced with permission of from Kan *et al.*, Appl. Phys. Lett. **113**, 212104 (2018). Copyright 2018 AIP Publishing.[16]

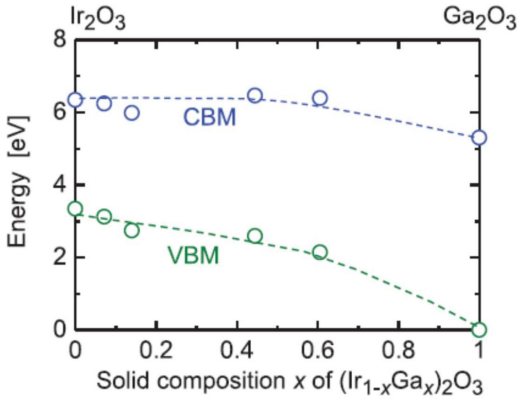

FIG. 19. CBM and VBM positions of α-$(Ga_xIr_{1-x})_2O_3$ in terms of Ga composition x. VBM of α-Ga_2O_3 is considered as the standard of energy ($E = 0$). Reproduced with permission from Kaneko *et al.*, Appl. Phys. Lett. **118**, 102104 (2021). Copyright 2021 AIP Publishing.[18]

sapphire. The epilayer comprised a 300-nm-thick Si-doped top layer and a 900-nm-thick UID buffer layer. Ti/Al/Ni/Au was used as source and drain electrodes instead of conventional Ti/Au, and as a result, the contact resistance was reduced by a factor of 10 or more. However, R_{on} was as high as 335 m Ω cm^2, and E_c was approximately 1 MV/cm, which was much lower than the expected material limit (~9.5 eV). Hence, there is still much room for improvement, as shown in Fig. 20. A vertical structure should be employed to fundamentally reduce R_{on}.

The FETs described above are normally on devices; however, normally off devices are desirable for safety. The research group of Kyoto University and FLOFIA demonstrated normally off operation of a preliminary MOSFET with a corundum-structured p-well layer (GaO™ MOSFET)[33] although the drain current was exceedingly small. The threshold gate voltage was as high as 7.9 V. The device structure and output characteristics are displayed in Figs. 21 and 22, respectively. The channel mobility of the MOSFET was as high as 72 cm^2/V s (Fig. 21),[33] which was superior to that of commercially available SiC devices.

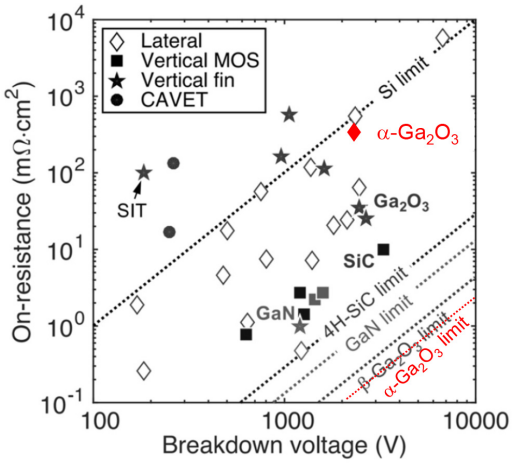

FIG. 20. Benchmarking of power transistors. Unlabeled data points are for β-Ga_2O_3. The α-Ga_2O_3 limit and the data for α-Ga_2O_3 MOSFET reported in Ref. 80 were added. Reproduced with permission from Green *et al.*, APL Mater. **10**, 029201 (2022). Copyright 2018 AIP Publishing.[81]

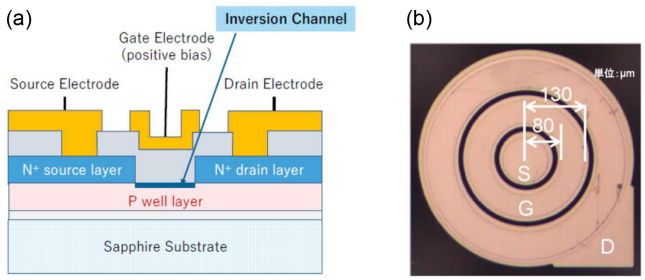

FIG. 21. (a) Schematic of the normally off GaO™ MOSFET. (b) Optical micrograph of the MOSFET. Reproduced with permission from https://flosfia.com/struct/wp-content/uploads/79cd9d2dfa54a771f642e008cc4f9cb0.pdf for "News Release From FLOSFIA and Kyoto University (2018)." Copyright 2018 FLOSFIA and Kyoto University.[82]

VI. SUMMARY AND FUTURE PERSPECTIVES

A. Growth methods

Currently, mist CVD and HCl-HVPE are the most matured growth methods for thin and thick α-Ga_2O_3 films, respectively. The primary reason is most likely the much wider growth windows to secure the phase purity than those in Cl_2-HVPE, MBE, and MOCVD. The existence of H_2 and/or H_2O in the growth atmosphere is a characteristic of mist CVD and HCl-HVPE. These facts indicate that H_2 and/or H_2O play an instrumental role in expanding the growth window. If the mechanism is clarified, and the MBE/MOVPE process is improved based on the mechanism, these methods could be considered mainstream to grow α-Ga_2O_3 thin films. From the perspectives of the high growth rate and residual impurity concentration, HVPE would be the best choice to grow a thick film, such as a drift layer for a high-V_B device, whose thickness can be several ten micrometers or more depending on the V_B. Multi-wafer planetary HVPE technology for GaN would be applicable to α-Ga_2O_3 for mass production.

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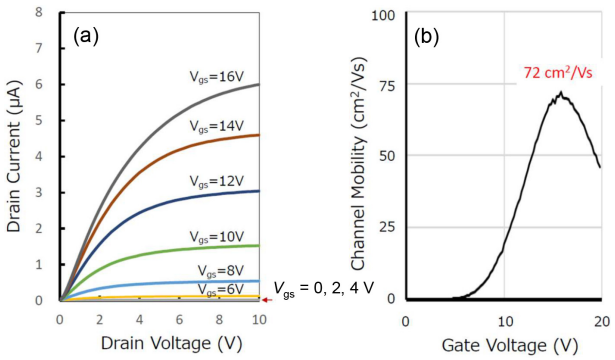

FIG. 22. (a) Output characteristics of the normally off GaO™ MOSFET. (b) Channel mobility of the MOSFET as a function of the gate voltage. Reproduced with permission from T. Shinohe, in Proceedings of the International Power Electronics *Conference (IPEC-Himeji 2022-ECCE Asia), Himeji, Japan* (IEEE, 2022), pp. 627–631. Copyright 2022 Institute of Electrical Engineers of Japan.[33]

B. Substrates

Currently, α-Ga_2O_3 has been grown heteroepitaxially on foreign substrates. However, freestanding α-Ga_2O_3 substrates are preferable. In the case of GaN, the melt growth requires ultra-high pressure. Consequently, it is virtually impossible to grow a practically useful bulk crystal for wafer fabrication, similar to the case of α-Ga_2O_3. Accordingly, freestanding GaN wafers are mass-produced by HVPE of a thick GaN layer on a foreign substrate and removal of the substrate following the growth.[83] It is likely that freestanding α-Ga_2O_3 wafers are developed in the future using the same methodology, as depicted in Fig. 23. It has been reported that α-Ga_2O_3 powder was grown via a flux method under a high pressure of 44 kbar.[84] If seeding and temperature gradient control under such ultra-high pressure are realized, a bulk α-Ga_2O_3 crystal could be grown to produce freestanding α-Ga_2O_3 wafers, although it would be a considerable challenge to accomplish it.

C. Defect control

At present, it is unclear how crystal defects in α-Ga_2O_3, including dislocations and point defects, affect device performance, what are the killer defects, and how low the concentrations should be. Such an investigation should be conducted in mutual feedback of the improvement of crystal growth technologies and the analysis of the device performance.

1. Dislocations

Although the dislocation density in heteroepitaxial α-Ga_2O_3 can be reduced by ELO, high-dislocation-density areas on window regions

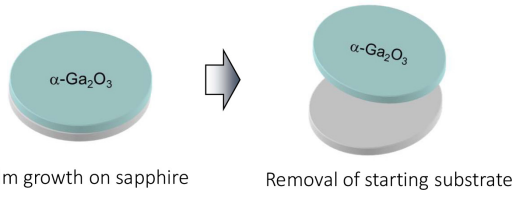

FIG. 23. Fabrication of a freestanding α-Ga_2O_3 wafer by HVPE thick film growth and removal of the starting substrate.

and formation of dislocations at the coalesced boundary remain problematic. However, we believe that such difficulties will eventually be overcome using the measures described in Sec. IV A. Indeed, the problem of production cost needs to be considered. Note that allowable dislocation density has not been experimentally clarified yet and needs to be explored in device development because the allowable dislocation density should be dependent on the device structure and operating conditions. There seems to be a tendency that wider bandgap semiconductors are more robust to crystal defects. For example, GaN-based laser diodes (LDs) with a dislocation density of 10^6 cm^{-3} efficiently operate while the dislocation density needs to be much lower in GaAs-based LDs. Despite the high dislocation density, the relatively high V_B and excellent ideality factor of current α-Ga_2O_3 SBDs may indicate that this tendency is applicable to α-Ga_2O_3.

2. Deep levels

Currently, the understanding of deep levels in α-Ga_2O_3 is insufficient despite the practical significance. Systematic investigation is required using samples grown by various growth methods under various growth conditions or with post-growth treatment such as thermal annealing and irradiation of particle beams. Furthermore, the origins of the deep levels need to be clarified by comparing the experimental results and theoretical predictions. Influence of the deep levels on the device performance, allowable trap density, and how to control the density should also be investigated.

D. Device-related issues

1. p-type layer

The hetero p–n-junction of α-$(Ir_xGa_{1-x})_2O_3$/α-Ga_2O_3 with small lattice mismatch is promising; however, the development is still in its infancy and there are many technical issues that need to be investigated such as carrier concentration control, point defects, and interface quality.

2. Device structure and fabrication process

Device structures of α-Ga_2O_3-based devices have been rather primitive without advanced edge-termination technologies developed for other preceding power semiconductor devices. Consequently, such immature device fabrication technologies may be a primary cause of low E_c,[80] which is far from the expected value. Accordingly, the device fabrication process needs to be further developed alongside improving the crystal quality. So far, it is difficult to use ion implantation, as explained in Sec. II, and the device structure needs to be developed by epitaxial growth and etching.[85–87] Fabrication of 3D-structures, such as trenches and fins by selective area growth without plasma damage, would also be an interesting choice, as demonstrated for β-Ga_2O_3.[88]

3. Thermal management

Self-heating of a power device driven under high-power-density condition is a serious problem that degrades device performance and destroys the device structure. In the case of Ga_2O_3, the problem is more serious than the case of SiC or GaN, primarily because the thermal conductivity is much lower, and higher power density is projected. Package-level thermal engineering alone is insufficient to enable efficient heat

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dissipation to lower the junction temperature to an acceptable level under severe conditions, and device-level engineering based on electro-thermal codesign is essential. In the case of β-Ga_2O_3, it has been predicted that the junction temperature lower than 200 °C should be possible for a lateral MOSFET driven under a power density of 10 W/mm by applying various measures, including the thinning of the β-Ga_2O_3 substrate, flip-chip heterointegration on a high-thermal-conductivity carrier wafer, and passivation using nano-crystalline diamond.[89] For more details regarding the thermal management of UWBG semiconductor power devices, refer to the excellent review by Choi *et al.*[90]

In the case of α-Ga_2O_3, thermal management has not been comprehensively investigated. Basically, similar strategies for β-Ga_2O_3 should be followed. However, it is unclear whether it is possible to realize sufficiently low thermal resistance because of the predicted thermal conductivity being even lower than those for β-Ga_2O_3 and the low thermal stability of α-Ga_2O_3. Fundamental thermal properties of α-Ga_2O_3 need to be experimentally explored for precise simulations.

E. Marketing strategies

Although the building blocks are in steady progress, it will take more time to realize commercially available high-quality α-Ga_2O_3 templates or freestanding substrates for the fabrication of power devices involving high-voltage operation. Accordingly, it would be a good strategy to initiate preliminary development in low to middle voltage device applications (<600 V), in which crystal defects would not have serious impact on the device performance. In this application area, including AC adopters, data server power supplies, and home appliances, α-Ga_2O_3 devices should have cost competitiveness, even to Si-based devices, because it should be possible to considerably reduce the epilayer thickness and device chip area owing to the higher E_c and lower R_{on}. In the future, it would also be possible to penetrate high-voltage-use or cost-effective-use market by solving the related technical problems and optimizing the mass-production technologies during the preliminary production period.

Considering the superior material properties of α-Ga_2O_3 and the progress of various technologies to compensate the drawbacks, such as high dislocation density and the difficulty in p-type conduction, we believe that α-Ga_2O_3-based devices occupy a certain position in the future power device market. The race has just started, and there are still many challenging technical problems to be overcome; however, it is worth a try.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Yuichi Oshima: Conceptualization (equal); Writing – original draft (lead). **Elaheh Ahmadi:** Conceptualization (equal); Writing – review & editing (lead).

DATA AVAILABILITY

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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