

Supporting Information

Transfer of Freestanding Fluoropolymer Films for Advanced Semiconductor Devices

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S1. Freestanding CYTOP Film Lamination

As described in the main manuscript, a polyacrylic acid (PAA) sacrificial layer was first spin-coated on Si substrates, followed by spin coating of CYTOP film. Figure S1a shows the CYTOP/PAA/Si sample (2 cm $\times$ 2 cm) after baking. A Kapton tape with a central cut was attached on top of the CYTOP film to provide wrinkle-free support during transfer (Figure S1b). The sample was then floated in deionized (DI) water (Figure S1c), dissolving the PAA layer and releasing the freestanding CYTOP film attached to the Kapton tape (Figure S1d). The film was subsequently mounted onto a copper frame with a circular aperture (Figures S1e and S1f) to facilitate precise lamination onto various substrates.

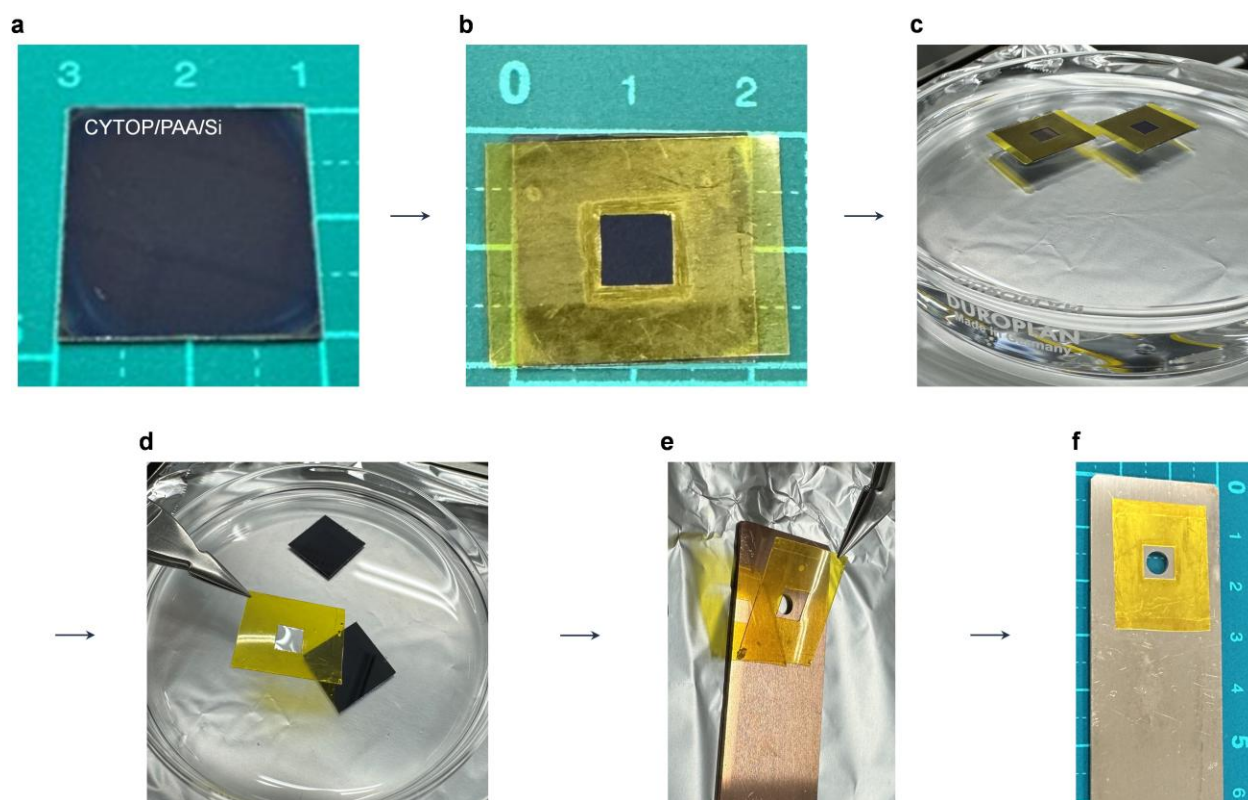


Figure S1. Photographs showing preparation of freestanding CYTOP film. (a) Spin-coated CYTOP and PAA layers on a Si substrate. (b) Attachment of Kapton tape onto the CYTOP/PAA/Si stack. (c) Kapton tape-supported assembly floated on DI water. (d) Kapton tape-supported freestanding CYTOP film. (e) Mounting CYTOP onto copper frame with a circular aperture. (f) Final CYTOP film assembly.

S2. Atomic Force Microscopy Analysis

Figure S2 presents atomic force microscopy (AFM) images of a bare Si substrate, PAA-coated Si, and CYTOP-coated Si without PAA. The AFM analysis of the bare Si substrate (Figure S2a) revealed a smooth and uniform surface morphology, with a root-mean-square (rms) roughness

of 0.10 ± 0.01 nm, measured over a $20 \mu\text{m} \times 20 \mu\text{m}$ scan area at 3 different locations. Figure S2b shows the AFM image of PAA coated on Si, which similarly exhibits a homogeneous and smooth surface, with rms roughness of 0.25 ± 0.02 nm. This indicates that the PAA layer maintains good uniformity without introducing significant topographical variations. AFM measurements of CYTOP spin-coated directly on Si (Figure S2c) reveal that the surface morphology remains nearly unchanged compared to CYTOP coated on PAA/Si (as shown in Figure 2i of the main manuscript). The rms roughness in this case is also comparable to that of CYTOP/PAA/Si, demonstrating that CYTOP forms a uniform and conformal film irrespective of the underlying substrate. Figure S2d presents histograms of the surface height distributions for the different samples, highlighting variations in roughness and providing a quantitative comparison of the topographical uniformity across Si, PAA/Si, and CYTOP films coated on Si and PAA/Si.

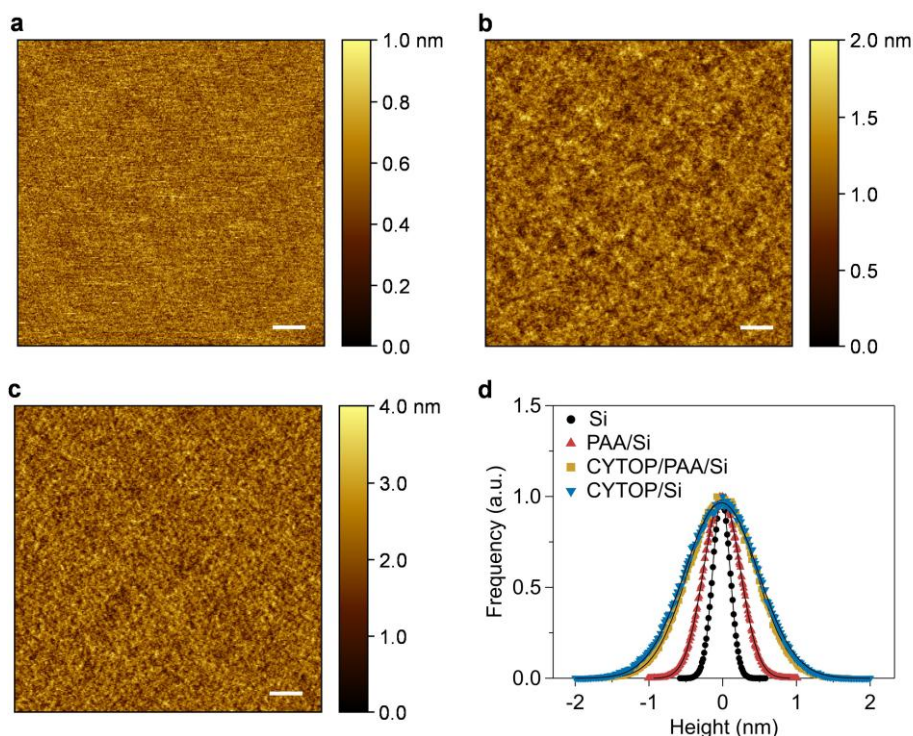


Figure S2. AFM images of (a) Si, (b) PAA/Si, (c) CYTOP/Si and (d) height histogram measured by AFM for Si, PAA/Si, CYTOP/PAA/Si and CYTOP/Si. Solid lines in (d) are Gaussian fits to the distributions. Scale bars, $2 \mu\text{m}$.

S3. Fabrication Process of H-terminated Diamond FETs

As discussed in the main manuscript, the lamination technique of the CYTOP fluoropolymer insulator was employed to fabricate FETs on H-terminated diamond substrates. Prior to the lamination process, lateral isolation of the active region was achieved via nitrogen-ion

(N-ion) implantation, which acts as a deep donor in diamond. This was performed by selectively covering the desired active region with photoresist mask, thereby shielding it from ion exposure during implantation. It has been shown^{1,2} that the surface conductivity of H-terminated diamond can be effectively suppressed by implanting a sufficiently high concentration of nitrogen near the surface. This suppression arises because the surface Fermi level remains significantly above the valence band maximum,¹ owing to the deep donor levels of nitrogen, which hinder the generation of holes via the surface transfer doping mechanism.^{3,4} Furthermore, the formation of conductive electrons in N-ion implanted diamond is also unlikely, since the donor levels associated with nitrogen are substantially deep. A comprehensive analysis of the electrical isolation achieved by N-ion implantation has been provided elsewhere.²

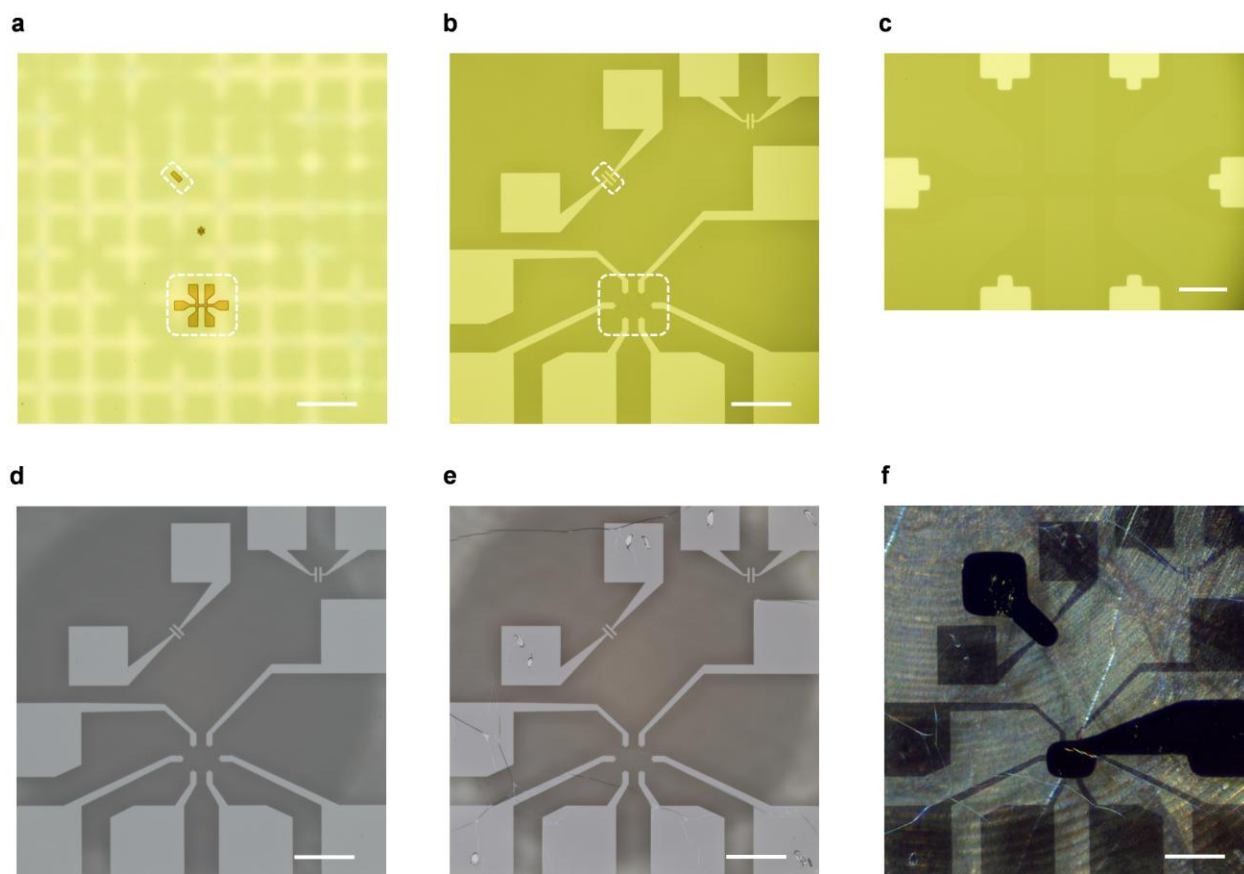


Figure S3. Optical microscope images showing the stepwise fabrication of the diamond FETs. (a) Undoped diamond substrate partially covered with photoresist mask for N-ion implantation. (b) Patterned electrodes on both unimplanted and implanted regions. (c) Magnified image displaying the unimplanted region with darker contrast. (d) Surface after H-termination. (e) After lamination of the CYTOP film. (f) Final FET structure after gate electrode deposition. All scale bars correspond to 200 μm , except for (c), which corresponds to 20 μm .

Figure S3a displays an optical microscope image of a diamond substrate patterned with photoresist mask to define the active region. The ion implantation was carried out using ^{15}N ions with a fluence of $1 \times 10^{14} \text{ cm}^{-2}$ at an energy of 10 keV under room temperature conditions. Following implantation, the photoresist mask was removed, and the substrates were subjected to a thorough cleaning process involving hot acid treatment and subsequent organic solvent cleaning to remove residual contaminants. Subsequently, bottom electrodes were defined on the cleaned substrates using maskless lithography followed by e-beam evaporation of Ti/Pt (5 nm/5 nm) metal electrodes, as shown in Figure S3b. The electrodes were patterned in both Hall bar and two-probe geometries on the unimplanted (active) region of the substrate, as marked by dashed boxes in Figures S3a and S3b. Figure S3c presents a magnified optical microscope image of the Hall bar geometry, displaying the contrast between the implanted and unimplanted regions. The darker region corresponds to the unimplanted, electrically active channel area where the electrodes are placed. Following N-ion implantation and electrode deposition, the diamond substrate was transferred to a microwave plasma-assisted chemical vapor deposition (MPCVD) system for global H-termination. The detailed procedure for H-termination and subsequent transfer of H-terminated diamond without air exposure is provided in the main manuscript. Figures S3d and S3e present optical microscope images of the H-terminated diamond and CYTOP-laminated H-terminated diamond, respectively, both captured inside an Ar-filled glove box. After lamination, an Al/Au (50 nm/100 nm) bilayer gate electrode was deposited using a shadow mask via thermal evaporation on both two-terminal and Hall bar configurations. The completed devices were then transferred to an N_2 -filled glove box for electrical measurements. Figure S3f shows an optical microscope image of the fabricated FET with a single layer CYTOP film, captured inside the N_2 -filled glove box. To assess the influence of CYTOP film on the electrical characteristics of H-terminated diamond, I - V measurements were conducted on both unimplanted and N-ion implanted regions. These measurements were performed in Ar-filled glove box to minimize the effect of ambient air on the H-terminated diamond surface. Figure S4 presents the I - V curves measured in two-probe geometry on unimplanted region before and after the lamination of the CYTOP insulating film without exposing diamond surface to ambient air. These results correspond to the device fabricated by stacking two layers of CYTOP on H-terminated diamond. The I - V measurements after CYTOP film lamination were carried out before the deposition of gate electrode (*i.e.* at the stage shown in Figures S3d and S3e). The measured resistance values were

subsequently converted to sheet resistance by multiplying the resistance by the width of the unimplanted region (or electrode width for the implanted region) and dividing by the electrode spacing. The sheet resistance before lamination was estimated to be $6 \times 10^{11} \Omega$, confirming the high resistive nature of the H-terminated diamond surface, as diamond surface was not exposed to ambient air. After the CYTOP lamination, the sheet resistance dropped to $4.5 \times 10^6 \Omega$, indicating the emergence of surface conductivity. This conductivity is attributed to the charge trapping sites within the CYTOP film, which can extract electrons from the valence band of H-terminated diamond and generate holes at the diamond surface, similar to the surface transfer doping mechanism reported for H-terminated diamond with deposited gate dielectrics.⁴ Possible mechanisms responsible for the emergence of surface conductivity after CYTOP film lamination are discussed in the *Discussion Section* of the main manuscript. The I - V measurements on implanted regions were also carried out (not shown here), which showed nearly no change in the resistivity values before and after CYTOP lamination, revealing that good isolation was achieved by N-ion implantation in diamond, consistent with results reported elsewhere.²

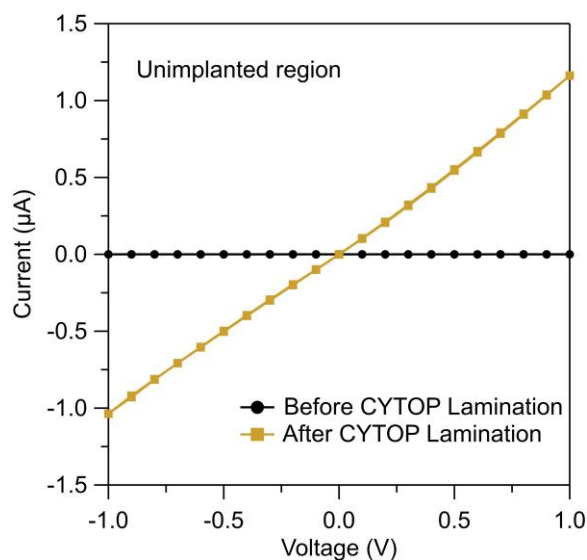


Figure S4. I - V characteristics of unimplanted region on H-terminated diamond before and after lamination with CYTOP gate insulator films without exposing H-terminated diamond to ambient air.

S4. H-terminated Diamond FETs using Double-layer CYTOP Insulating Films

As discussed in the main manuscript, the electrical performance of the fabricated diamond-based FETs was systematically evaluated at room temperature by measuring both output and transfer characteristics. To verify the reproducibility and reliability of our fabrication method, three FETs were prepared, two with single-layer CYTOP and one with double-layer CYTOP, with each

layer thickness of 90 nm. Figure S5 shows the data of a *p*-channel H-terminated diamond FET fabricated by stacking two 90 nm thick CYTOP films (total thickness of 180 nm), while the data of an FET fabricated with a single-layer CYTOP film is presented in main manuscript.

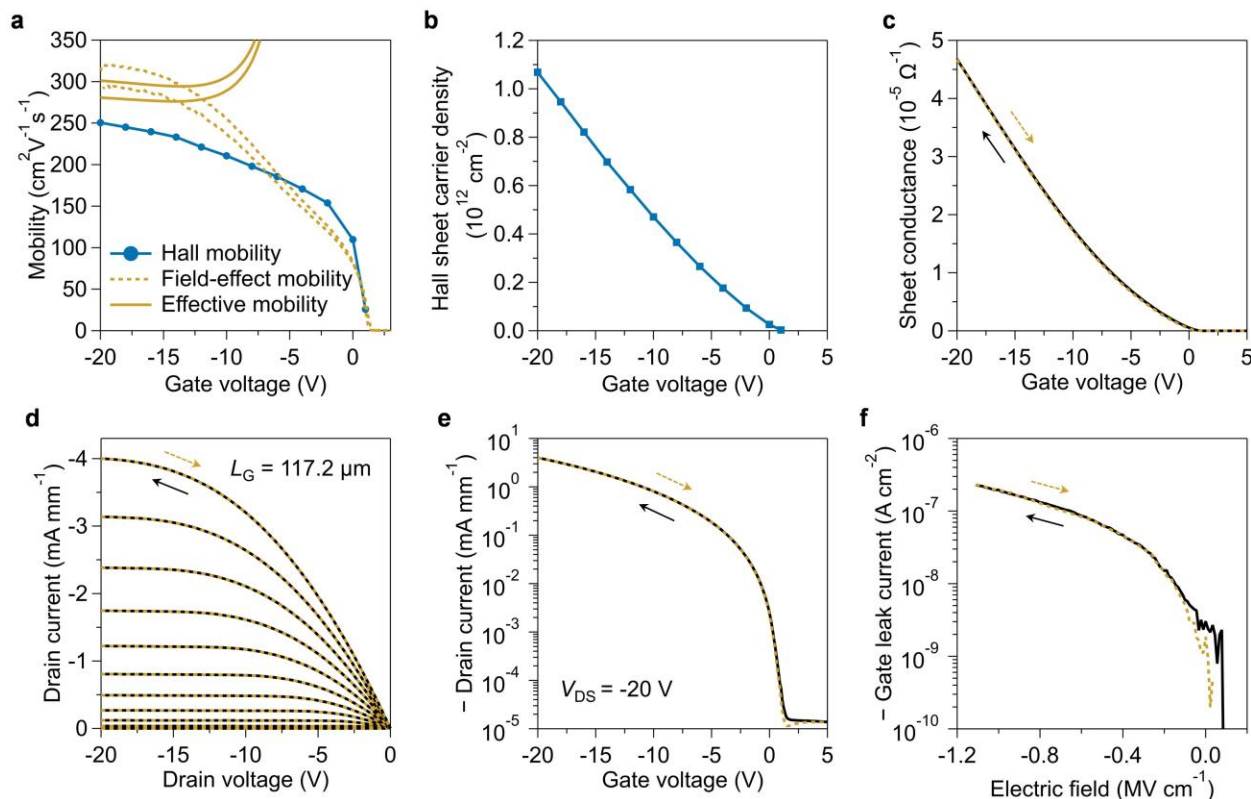


Figure S5. Electrical characteristics of the diamond FET with double-layer CYTOP insulator. (a) Gate voltage dependent Hall mobility, along with field-effect and effective mobilities. Among the two solid lines, the higher one corresponds to the effective mobility obtained without air exposure of FET, while the lower one corresponds to that after air exposure. Similarly, for the dashed lines, the higher one represents the field-effect mobility without air exposure, whereas the lower one corresponds to the values obtained after air exposure. (b) Hall sheet carrier density versus gate voltage. (c) Gate voltage dependence of sheet conductance in the linear region obtained from four-probe measurements, where the gate voltage was swept from +5 to −20 V and back. (d) Output characteristics measured using a two-probe configuration, showing the drain current versus drain voltage for gate voltages varied from +4 to −20 V in 2 V steps. (e) Drain current versus gate voltage at a fixed drain voltage of −20 V. (f) Gate leak current density versus electric field, where the electric field is calculated by dividing the gate voltage by the CYTOP film thickness. In (c)-(f), solid black and dashed brown lines correspond to forward and backward sweeps, respectively.

The geometrical parameters of the Hall-bar configuration, including the channel length (L_G), channel width (W_G), and the separation between voltage probes (L_p), were determined from optical microscope images. For this device, L_G was 117.2 μm , W_G was 7.9 μm , and L_p was 29.6 μm . Gate-voltage-dependent Hall measurements were carried out to obtain mobility and sheet

carrier density by sweeping the magnetic field between -0.5 and $+0.5$ T, and the results are presented respectively in Figures S5a and S5b. It is seen that Hall mobility and carrier density values increase monotonously with increase of gate voltage, reaching the maximum values of $250 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $1.1 \times 10^{12} \text{ cm}^{-2}$, respectively, at gate voltage of -20 V. Figure S5c shows the sheet conductance measured in four-probe configuration by sweeping the gate voltage (V_{GS}) from $+5$ to -20 V and back from -20 to $+5$ V, while applying drain voltage (V_{DS}) of ± 100 mV. The maximum sheet conductance at gate voltage of -20 V was observed to be $4.7 \times 10^{-5} \Omega^{-1}$, corresponding to a sheet resistance of $21 \text{ k}\Omega$. By extrapolating the linear region of sheet conductance in the gate voltage range of -10 V to -20 V, the threshold voltage (V_{th}) was estimated to be -4.2 V. The effective mobility was calculated to be $\approx 300 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and maximum carrier density was estimated to be $9.8 \times 10^{11} \text{ cm}^{-2}$ at V_{GS} of -20 V. Most of the FET measurements were carried out inside an N_2 -filled glove box without exposing the device to air, whereas Hall measurements required device transfer, during which ambient air exposure was unavoidable. Accordingly, Figure S5a presents both field-effect and effective (calculated using a threshold voltage of -4.2 V) mobilities derived from the gate voltage dependence of sheet conductance measured before and after air exposure. The procedure for calculating effective and field-effect mobilities is described in the main manuscript. Upon exposure to air, the effective and field-effect mobilities show slight decrease ($\approx 10\%$ reduction), which is attributed to the marginal surface transfer doping caused by the adsorption of airborne acceptor-like species in the channel region. These adsorbates can increase Coulomb scattering at the surface, thereby reducing the carrier mobility.⁵ Note that the apparent increase in effective mobility as V_{GS} approaches V_{th} arises because the denominator in the mobility extraction formula approaches zero (effective mobility $\propto 1/|V_{\text{GS}} - V_{\text{th}}|$),⁵ leading to a diverging mobility value.

Figure S5d presents the output characteristics, in which the drain current (I_{DS}) was recorded by sweeping V_{DS} from 0 to -20 V and then in the reverse direction, at different V_{GS} ranging from $+4$ to -20 V in 2 V steps. The device clearly shows current modulation across both the linear and saturation regions, confirming effective field-effect control of two-dimensional hole gas (2DHG) at the diamond surface. The drain current was normalized by dividing the values with W_{G} . The maximum drain current in this case was observed to be -4 mA mm^{-1} at $V_{\text{DS}} = V_{\text{GS}} = -20$ V. In the linear region (low V_{DS}), I_{DS} increases linearly with V_{DS} , indicating the formation of good ohmic contacts at the source and drain electrodes. As V_{DS} is increased further, the current reaches a

saturation point and becomes nearly unchanged. Figure S5e shows the transfer curve, where drain current was measured in two-probe configuration as a function of gate voltage at a fixed $V_{DS} = -20$ V. An on/off current ratio of 2.8×10^5 was extracted from Figure S5e. It is seen that the output and transfer curves display negligible hysteresis, indicative of substantially low interface trap density. The normalized hysteresis, obtained from Figure S5e in the gate voltage range of 0.3 to -1 V, was found to be ≈ 30 mV (MV cm $^{-1}$) $^{-1}$, which is slightly larger than the value presented in the main manuscript; however, it remains of the same order as those reported for highly cleaned 2D semiconductor interfaces.^{6,7} The subthreshold swing (SS) from Figure S5e was determined to be approximately 600 mV dec $^{-1}$. The interface trap density (D_{it}) can be estimated by following the equations⁸

$$SS = \ln 10 \frac{dV_{GS}}{d(\ln I_D)} = \ln 10 \frac{k_B T}{e} \frac{C_{CYTOP} + C_{depl} + e^2 D_{it}}{C_{CYTOP}} \quad (S1),$$

$$C_{depl} = \sqrt{\frac{\epsilon_{\text{diamond}} e N_D}{2\phi_S}} \quad (S2),$$

where k_B is the Boltzmann constant, T is the absolute temperature, e is the elementary charge, C_{CYTOP} ($= \epsilon_{CYTOP}/t_{CYTOP}$) is the capacitance of CYTOP gate insulator, and C_{depl} is the capacitance of the diamond depletion layer. Here, $\epsilon_{\text{diamond}}$ is the permittivity ($5.7\epsilon_0$) of diamond and ϕ_S is surface potential. Using a relative dielectric constant of 2.0 for CYTOP, subthreshold swing of 600 mV dec $^{-1}$, and thickness of 180 nm, the interface trap density for this device was estimated to be $\leq 6 \times 10^{11}$ cm $^{-2}$ eV $^{-1}$. In this calculation, we assumed C_{depl} to be zero yielding the maximum possible value of D_{it} . The diamond substrates used in this study were purchased from Element Six, which possess boron (N_A) and nitrogen (N_D) impurity concentrations of <0.5 ppm and <1 ppm, respectively. When the depletion capacitance is taken into account by assuming $N_D = 1$ ppm and $\phi_S = 4$ V,^{1,5} Equation S2 gives $C_{depl} = 4 \times 10^{-2}$ $\mu\text{F cm}^{-2}$. Under these conditions, the extracted D_{it} value decreases to $\approx 3 \times 10^{11}$ cm $^{-2}$ eV $^{-1}$. Similarly, the interface trap density reported in the main manuscript was also calculated under the assumption that $C_{depl} = 0$. However, when $C_{depl} = 4 \times 10^{-2}$ $\mu\text{F cm}^{-2}$ is considered, the estimated trap density further decreases to approximately 1×10^{11} cm $^{-2}$ eV $^{-1}$ for the FET presented in the main manuscript. The trap density for the FET with double layer CYTOP is slightly higher than the FET fabricated with single-layer CYTOP, but it remains nearly comparable to or lower than most reported values for H-terminated diamond FETs. The increase in trap density in this case may be attributed to the slight inhomogeneity of H-termination of diamond surface as well as to defects or imperfections on the diamond or CYTOP surfaces

introduced during the fabrication process. This increase in trap density likely contributed to the observed reduction in mobility compared to the device reported in the main manuscript. Figure S6 compares the interface trap density versus relative dielectric constant, including the highest D_{it} values obtained in this work and extracted results from reported studies on H-terminated diamond FETs.^{5,9-18} Figure S5f shows the gate leakage current density as a function of electric field. As also described in the main manuscript, the leakage current was measured by shorting the source and drain electrodes and sweeping V_{GS} from +4 to -20 V and then in reverse direction. The leakage current was normalized to the active channel area of Hall bar under the gate electrode. Overall, the FET shows good device performance with substantially high hole mobility values highlighting the effectiveness and reproducibility of our device fabrication process.

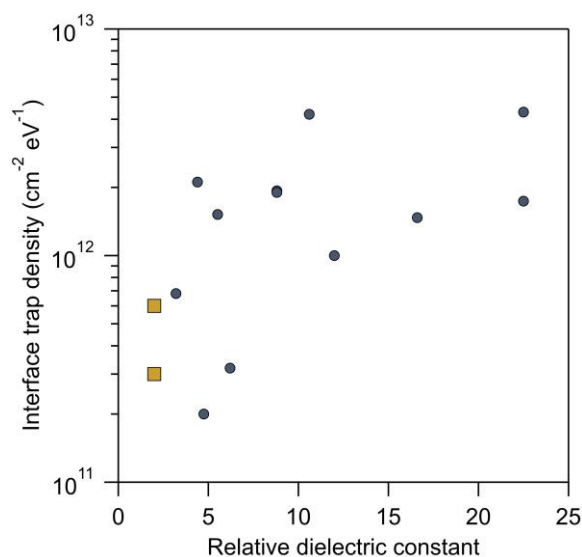


Figure S6. Comparison of the interface trap density versus relative dielectric constant for H-terminated diamond FETs. Yellow squares represent data from this work, while grey circles correspond to reported literature values.^{5,9-18}

S5. Stability After Long-Term Storage

The long-term stability of the device was assessed by comparing its electrical performance before and after extended storage. Following the initial measurements presented in the main manuscript, the same device was briefly exposed to ambient air for approximately one hour and then stored in an N₂-filled glove box. Figure S7a displays the output curves from the initial measurements, where the drain current is plotted against drain voltage ranging from 0 to -20 V at gate voltages from +2 to -20 V in 2 V steps. After 558 days of storage, output curves measured under similar conditions are shown in Figure S7b. These results demonstrate a slight increase in drain current (by approximately 20%) compared to the initial values. Figure S7c presents the gate

voltage dependence of the sheet conductance measured in a four-probe configuration, comparing the initial data with that obtained after 578 days of storage. The device exhibited no significant change in the conductance or threshold voltage, retaining similar output and transfer characteristics and demonstrating excellent long-term electrical stability. Both measurements (initial and after storage) also showed negligible hysteresis, indicating stable dielectric and interface properties consistent with the low interface trap density presented in Figure S6. In addition, preliminary bias-stress measurements (not included in the present manuscript) revealed negligible threshold voltage shift under prolonged gate bias, further supporting the high dielectric and interface quality. This is aligned with previous studies on organic FETs employing a coated CYTOP gate dielectric, which showed a low interface trap density and demonstrated high stability under bias stress.¹⁹ The slight increase in drain current may be attributed to reduced contact resistance, likely arising from enhanced surface transfer doping near the electrodes as a result of ambient exposure.^{3,4} A minor interfacial gap between the electrodes and the CYTOP film may facilitate atmospheric adsorption, thereby reducing the contact resistance and increasing the drain current. Overall, these findings demonstrate that the transferred CYTOP dielectric film provides reliable gate control and excellent long-term device stability even after environmental exposure and extended storage.

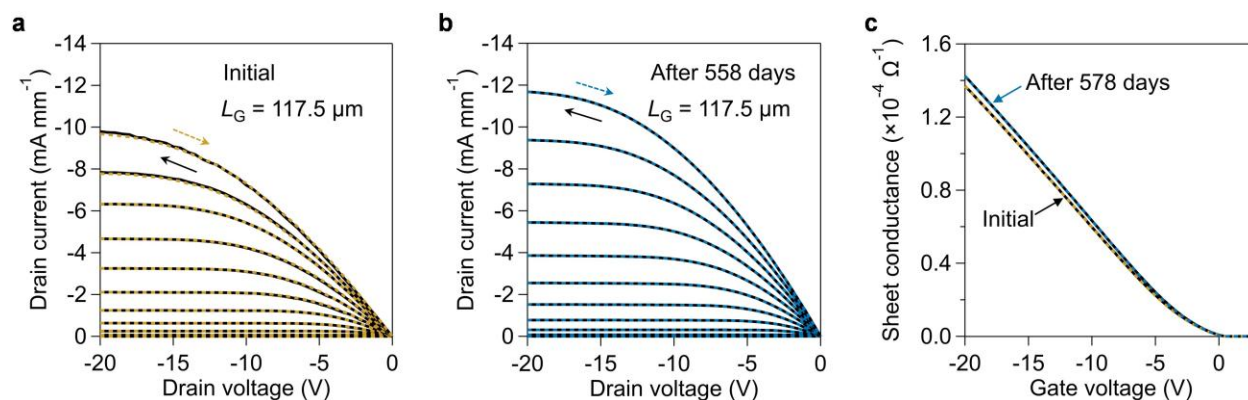


Figure S7. The stability of the diamond FET with CYTOP gate insulator after long-term storage. (a) Output characteristics measured immediately after device fabrication (as also shown in main manuscript) using a two-probe configuration, displaying the drain current versus drain voltage at different gate voltages of +2 to -20 V in 2 V steps. (b) Output characteristics of the same device measured after 558 days of storage under identical measurement conditions with gate voltages varied from +2 to -20 V in 2 V steps. (c) Comparison of the gate-voltage-dependent sheet conductance measured initially and after 578 days of storage in the linear region using a four-probe configuration while applying V_{DS} of ± 100 mV. Solid and dashed lines in (a)-(c) correspond to forward and backward sweeps, respectively.

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