

Transfer of Freestanding Fluoropolymer Films for Advanced Semiconductor Devices

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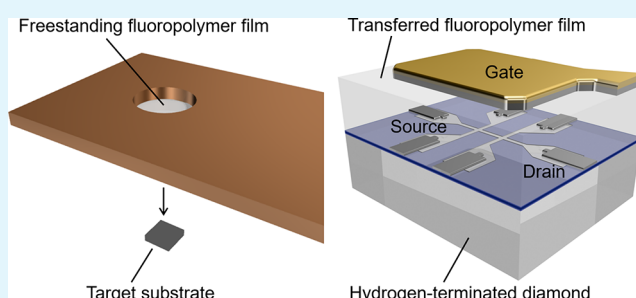
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ABSTRACT: High-quality dielectric films are essential for fabricating advanced electronic devices, but their direct deposition often degrades the films and their underlying interfaces, which compromises device performance, especially on sensitive or low-adhesion surfaces. To overcome these limitations, film transfer methods enable the integration of high-quality dielectric films onto such surfaces without damaging the underlying interfaces. However, existing transfer methods have predominantly focused on high-dielectric-constant (high- κ) materials, leaving a critical gap for transferable, high-quality low- κ alternatives, which are required for enabling low-power and high-speed electronics. Herein, we address this need by demonstrating a method to integrate freestanding low- κ fluoropolymer dielectric films with smooth surface morphology onto diverse substrates, including low-adhesion surfaces like hydrogen-terminated diamond. The transferred films revealed high breakdown fields of $8.0 \pm 1.2 \text{ MV cm}^{-1}$, with leakage current density remaining typically below $10^{-7} \text{ A cm}^{-2}$ before the breakdown. The incorporation of these fluoropolymer films as gate dielectrics in p-channel hydrogen-terminated diamond field-effect transistors resulted in transfer and output characteristics with negligible hysteresis, high channel mobility ($\approx 400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), and a low interface trap density ($\leq 3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$). These findings highlight the versatility of the transfer method and position freestanding fluoropolymers as a promising platform for forming high-quality dielectric/semiconductor interfaces for advanced electronics.

KEYWORDS: freestanding fluoropolymer films, dielectric film transfer, low- κ dielectric, low interface trap density, diamond FETs



1. INTRODUCTION

The continuing progress in unlocking new possibilities for high-performance, energy-efficient, and multifunctional semiconductor devices is paving the way for breakthroughs in power electronics, communication technologies, and wearable electronics.^{1–3} These advancements have attracted great interest in the development of next-generation transistors and hybrid electronic systems^{4,5} through the integration of high-quality gate dielectrics, which enable reduced leakage current, enhanced carrier modulation, and improved device stability. The dielectric films are routinely grown by atomic layer deposition (ALD), chemical vapor deposition (CVD), pulsed laser deposition (PLD), and sputtering; however, these techniques often involve high temperatures or energetic species, which can significantly damage chemically sensitive surfaces and degrade interfacial quality.^{6–8} Furthermore, widely used dielectric films, such as SiO_2 , Al_2O_3 , and HfO_2 , have demonstrated incompatibility with two-dimensional (2D) materials or surfaces lacking dangling bonds, resulting in poor adhesion and degraded dielectric film quality.^{8–10} These challenges have spurred significant research efforts aimed at improving dielectric film deposition approaches^{11–13} and developing alternative

strategies to enable nondestructive dielectric integration. Among these emerging approaches, the transfer or lamination of pre-formed dielectric films has recently gained considerable attention because it avoids the limitations of direct deposition.^{14–20} Although these methods have demonstrated improvements in device performance, they have predominantly focused on high- κ materials. This, however, has left a critical gap for transferable, high-quality low- κ alternatives, which are crucial for minimizing power consumption and parasitic capacitance in high-frequency applications.

CYTOP, an amorphous fluoropolymer, has potential to fill this gap, as it exhibits outstanding dielectric properties, including low- κ of 2.0–2.1, high electrical resistivity, and a large breakdown strength.^{21,22} In addition, CYTOP exhibits chemical

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inertness, extremely low water absorptivity ($<0.01\%$), and can form highly uniform, large-area films via solution processing, enabling scalable and reliable device integration. Its high optical transparency ($>95\%$) and low refractive index (1.34)²¹ further broaden its applicability to optoelectronic and photonic devices. Owing to these properties, CYTOP has been employed in a wide range of applications, including organic field-effect transistors (OFETs), bioelectronics, anti-reflective coatings, and photonic encapsulation.^{23–28} Although the inherently low surface energy and chemical inertness of the CYTOP film surface posed challenges in standard lithographic processing, recent advances in surface activation methods, resist formulation, and adhesion-promoting treatments have enabled the successful implementation of high-resolution photolithography on CYTOP films.^{29,30} Despite the excellent properties of CYTOP and the recent advancements, most studies reported to date have focused on spin-coated CYTOP films, while the properties and potential applications of pre-formed freestanding CYTOP dielectric films remain largely unexplored.

In this work, we demonstrate the transfer-integration of freestanding CYTOP films into semiconductor devices without degrading the target surface, thereby achieving high-quality interfaces. The lamination of freestanding CYTOP films was achieved onto a wide range of substrates such as silicon, sapphire, diamond, and CYTOP itself, enabling dielectric integration across diverse device architectures. The metal–insulator–metal (MIM) structures fabricated on the sapphire substrate utilizing the transferred freestanding CYTOP dielectric films revealed the breakdown fields of $8.0 \pm 1.2 \text{ MV cm}^{-1}$, while the leakage current densities remain substantially low ($<10^{-7} \text{ A cm}^{-2}$) before the breakdown. The CYTOP film was also transferred to hydrogen-terminated (H-terminated) diamond, a dangling-bond free surface where weak adhesion characteristics and high sensitivity to the deposition environment often result in poor film quality and surface degradation. The p-channel H-terminated diamond FETs incorporating the transferred CYTOP gate dielectric were fabricated, exhibiting negligible hysteresis in output and transfer characteristics, along with a substantially low interface trap density and high hole mobility. These findings demonstrate the excellent properties of CYTOP and validate the feasibility of the present transfer method, thus establishing a versatile platform for dielectric integration and broadening the scope of CYTOP applications in advanced electronic and optoelectronic technologies.

2. TRANSFER AND CHARACTERIZATION OF FREESTANDING CYTOP FILMS

2.1. Fabrication of Freestanding CYTOP Films

The fabrication and transfer process for freestanding CYTOP fluoropolymer films is schematically illustrated in Figure 1, and the details are provided in Section 6. Polyacrylic acid (PAA), a hydrophilic and water-soluble polymer,³¹ was used as a sacrificial layer to enable the subsequent lift-off or exfoliation of the CYTOP film. The PAA layer was first spin-coated onto silicon (Si) substrates and then baked. Subsequently, type-S CYTOP²¹ was spin-coated onto the PAA/Si and baked, forming the final stack structure illustrated in Figure 1a. The baking process is provided in Section 6. The photograph of the prepared CYTOP/PAA/Si sample is shown in Figure S1a of the Supporting Information. To facilitate the exfoliation

and the transfer of the freestanding CYTOP film without any distortion, a high-temperature resistant Kapton tape was fixed onto the CYTOP/PAA/Si sample with a pre-cut central aperture to define a localized area of interest for clean CYTOP film transfer, as shown in Figure 1b (see also Figure S1b for the corresponding photograph). The Kapton provides mechanical support and minimizes wrinkle formation, while simultaneously enabling a feasible transfer of CYTOP films without contaminating the localized area of interest. After this step, the assembled stack (Kapton/CYTOP/PAA/Si) was floated on a deionized (DI) water bath, which was kept on a hot plate with temperature of 50°C to accelerate the dissolution of the underlying PAA layer, as shown in Figure S1c. Although PAA is water-soluble at room temperature, elevated temperature ensures faster and more consistent water penetration to dissolve PAA. During the dissolution of PAA, only the lower surface of the CYTOP film was exposed to water, while the upper surface remained pristine thereby preserving the surface integrity and minimizing contamination on the intended transfer surface. After the complete dissolution of the PAA layer, the underlying Si substrate was detached and the Kapton-tape-supported CYTOP film remained floating on the water surface, as illustrated in Figure 1c. To prevent wrinkle formation, enable accurate film alignment, and improve handling during lamination, the tape-supported CYTOP film was mounted onto a copper frame with a circular aperture near one of the edges of the frame, as illustrated in Figure 1d. The aperture in the copper frame allows alignment of the freestanding CYTOP film during the lamination under the optical microscope. Finally, the assembly was baked at 100°C for 5 min to remove residual moisture and stored in a vacuum-sealed container to prevent contamination from airborne particulates.

2.2. Transfer of Freestanding CYTOP Films

The freestanding CYTOP films prepared as discussed above were transferred onto various substrates, including Si, CYTOP laminated Si, sapphire, and H-terminated diamond. Figure 1e depicts the lamination step of the copper-frame-supported CYTOP film onto the target substrate, while Figure 1f presents a schematic of the final sample. The transfer was carried out by using a movable stage, which provided x-y-z control of the copper frame holding the freestanding CYTOP film under an optical microscope, enabling accurate positioning and controlled contact with the target substrate. The target substrate was mounted on an adjacent sample stage equipped with a vacuum chuck to securely hold the substrate, which also featured a heater to bake the substrate when necessary to remove surface adsorbates during CYTOP film transfer. The corresponding photograph of the sample stage and movable stage holding the copper frame is shown in Figure 2a. The copper frame is fixed in a way that the pristine CYTOP surface faces downward, allowing direct contact with the target substrate. Prior to CYTOP lamination, the sample stage temperature was set to 110°C . The aperture in the copper frame, which is larger than the size of the substrate, was aligned above the substrate using fine x-y adjustments (Figure 2a) under the optical microscope. After alignment, the copper frame was gradually lowered to bring the CYTOP film into contact with the target substrate surface. The CYTOP films were found to adhere immediately to the substrate; therefore, the film and substrate were aligned parallel before contact to prevent misalignment or wrinkles. The freestanding CYTOP films were transferred to various

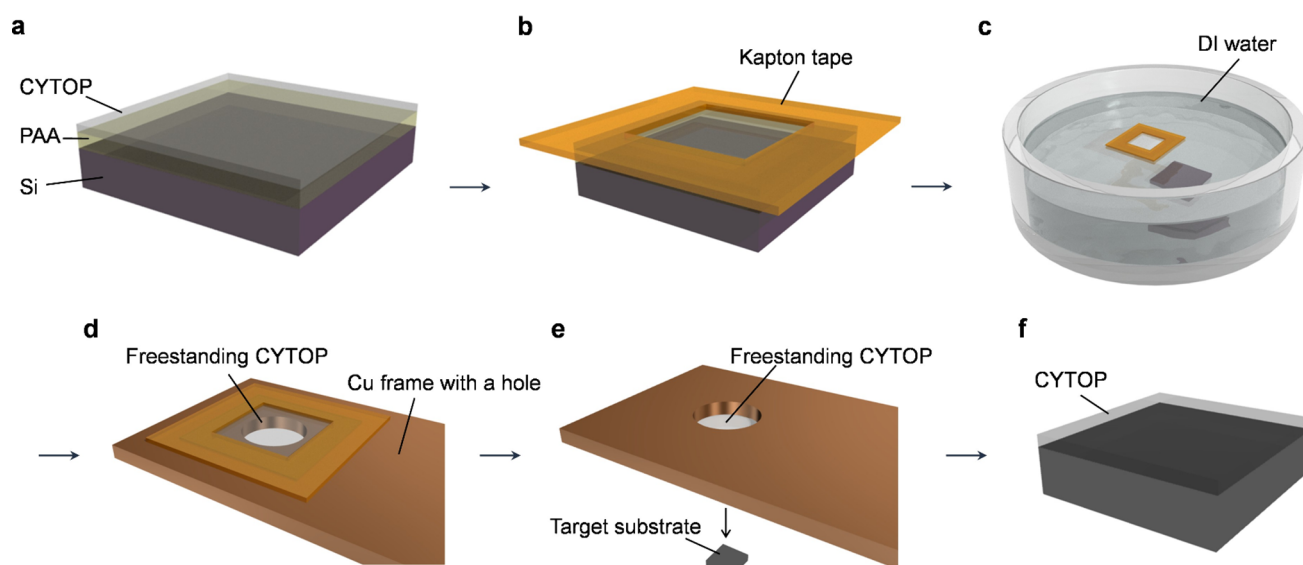


Figure 1. Schematic illustration of the CYTOP film transfer process. (a) Spin-coated CYTOP and PAA layers on the Si substrate. (b) Attachment of a Kapton tape on the CYTOP surface for mechanical support. (c) Release of the Kapton-supported CYTOP film by dissolving the PAA layer in water. (d) Mounting of the Kapton-supported CYTOP film onto a copper frame with an aperture. (e) Lamination of the freestanding CYTOP film onto the target substrate. (f) Target substrate laminated with the CYTOP film.

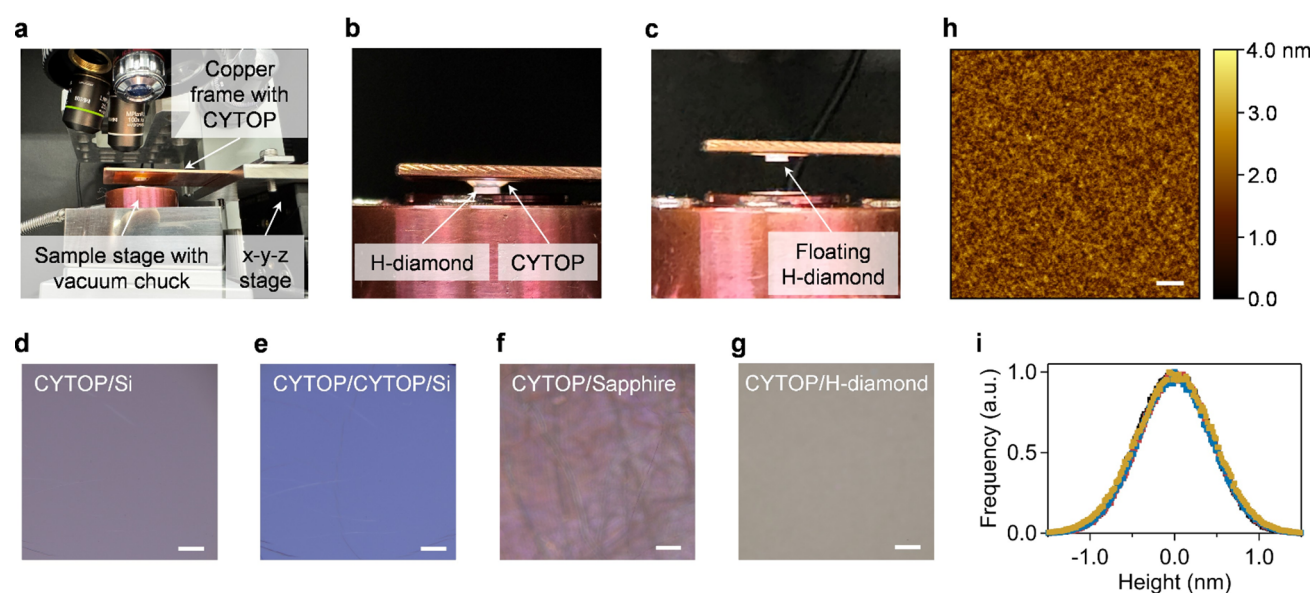


Figure 2. Transfer of freestanding CYTOP films. (a) Sample stage with vacuum chuck along with an adjacent x-y-z movable stage holding the copper frame containing the freestanding CYTOP film. (b) Laminated CYTOP film on H-terminated diamond in ambient air, showing CYTOP bending at the diamond periphery due to slight upward movement of the copper frame while the diamond remains fixed on the stage. (c) H-terminated diamond floating after release from the sample stage and further upward movement of the copper frame. CYTOP film laminated on (d) Si, (e) CYTOP/Si, (f) sapphire, and (g) H-terminated diamond. (The dark lines observed in (f) do not correspond to features of the CYTOP films, but originate from the underlying sample stage, made visible by the high transparency of the sample, and further enhanced by slight focus deviations.) Scale bars in (d–g): 200 μm . (h) AFM image of a spin-coated CYTOP film on PAA/Si (scale bar: 2 μm). (i) Height histogram obtained for four different samples.

substrates, including a H-terminated diamond surface, which typically resists the deposition of metals and insulators. Figure 2b shows the photograph of a CYTOP film laminated on a H-terminated diamond substrate in ambient air, which was captured after slightly retracting the copper frame (or moved in an upward direction) in the z-direction after lamination, while the diamond substrate remained fixed on the stage.

It is seen that the CYTOP film is bent around the edge of the diamond substrate, demonstrating substantial bonding between CYTOP and the diamond surface. After turning off the vacuum to the vacuum chuck to release the diamond substrate from the sample stage, the z-axis of the stage holding the copper frame was raised further. The diamond substrate remained attached to the CYTOP film and was lifted along with it, as shown in

Figure 2c. The optical microscope images of CYTOP films laminated on various substrates are shown in **Figure 2d–g**. Minor wrinkles observed in the transferred CYTOP films were effectively removed by post-annealing at 130 °C (not shown), likely due to the relaxation of residual mechanical stress generated during the transfer process. These observations suggest that CYTOP can be used as a transferable film that adheres to various substrates.

2.3. Surface Morphology

The atomic force microscopy (AFM) was performed on CYTOP films to study the surface morphology. The surface morphology plays a crucial role in determining the effectiveness of dielectric films in electronic devices, particularly by ensuring uniform film coverage and minimizing local electric field enhancements that could lead to early breakdown.^{32,33} **Figure 2h** displays the AFM image of the spin-coated CYTOP film on PAA/Si over a scan area of 20 $\mu\text{m} \times 20 \mu\text{m}$, which reveals a substantially smooth and featureless surface morphology. The AFM measurements were performed at multiple locations on four different samples prepared under similar conditions, yielding a root-mean-square (rms) roughness of $0.45 \pm 0.03 \text{ nm}$. The height histogram in **Figure 2i** corresponding to the AFM measurements of four different samples confirms negligible variation, indicating high uniformity and consistent roughness values. In order to compare, the AFM measurements were also performed on the Si substrate, PAA coated on Si, and the CYTOP film coated on Si without PAA, which are shown in **Figure S2**. The surface morphology and roughness of CYTOP films were also found to be nearly the same when directly spin-coated on Si without PAA, as shown in **Figure S2**, indicating that the film morphology does not change due to the underlying layer. The high uniformity and low roughness of CYTOP films make them suitable for the transfer method.

2.4. Electric Breakdown Strength

The electric breakdown strength of freestanding CYTOP films was evaluated by fabricating the MIM structure. Initially, bottom electrodes were patterned on cleaned sapphire substrates using maskless laser lithography followed by the deposition of Ti/Pt (5 nm/5 nm) electrodes by e-beam evaporation. After bottom electrode deposition, the freestanding CYTOP film was laminated in ambient air following the transfer method discussed above. The film thickness was controlled in the range of 25 to 221 nm by systematically adjusting both the CYTOP solution concentration and the spin-coating rotation speed. Finally, after the lamination, top electrodes (Al/Au: 50 nm/100 nm) were deposited through a metal shadow mask using a thermal evaporator. **Figure 3a** and the inset of **Figure 3b** show the schematic and optical microscope images of the MIM structure, respectively. **Figure 3b** presents the current–voltage (*I*–*V*) characteristics of MIM devices, with the negative voltage applied to the top electrode and current measured from the bottom electrode. The *I*–*V* measurements show that the devices consistently exhibited low leakage current densities, typically remaining below $10^{-7} \text{ A cm}^{-2}$, and in all cases not exceeding the $10^{-6} \text{ A cm}^{-2}$ range prior to dielectric breakdown. The breakdown electric field was measured to be in the range of 5.9–10.4 MV cm^{-1} . The substantially high breakdown fields obtained across the devices confirm the excellent insulating characteristics of laminated CYTOP films. Moreover, these breakdown field values are comparable to those of directly spin-coated thick CYTOP films,²² which demonstrates that our transfer approach preserves the insulating property of CYTOP. To further evaluate the dielectric properties of the transferred films, capacitance–voltage (*C*–*V*) measurements were performed on diamond FETs employing transferred CYTOP as the gate dielectric. The extracted relative dielectric constant was 2.0, which is consistent with previously reported values for CYTOP²¹ and will be discussed in detail in the next

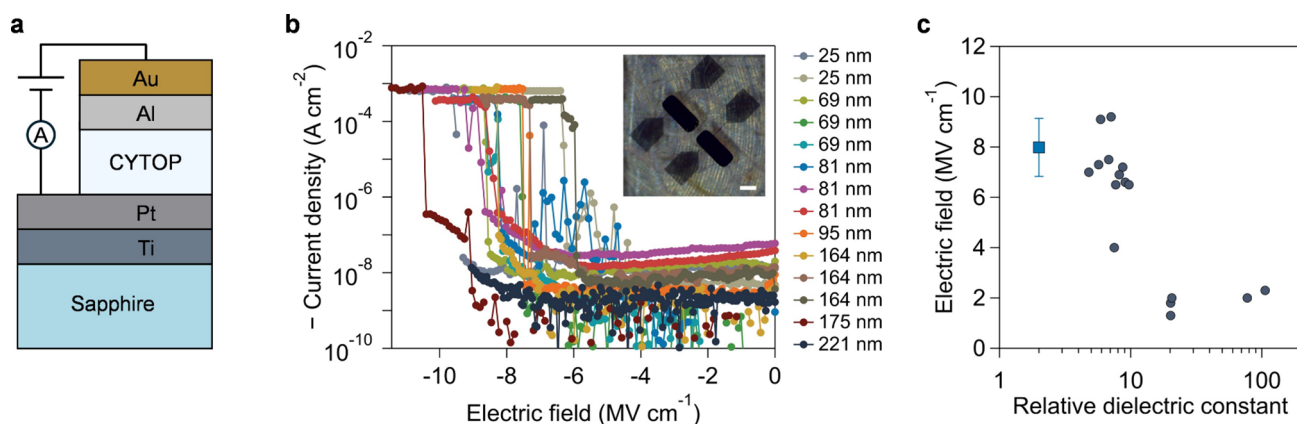


Figure 3. Electrical characteristics of metal–insulator–metal (MIM) structures. (a) Schematic illustration of the MIM structure. (b) Leakage current density as a function of electric field for MIM structures fabricated with transferred, freestanding CYTOP dielectric films of varying thicknesses. The data for the 175 nm device corresponds to a two-layer stack of CYTOP films. The measured current was converted to current density using the overlapping area between the top and bottom electrodes, while the voltage was converted to electric field by normalizing it to the CYTOP film thickness. A negative sign of the electric field corresponds to negative voltage applied to the top electrode (Al/Au) with respect to the bottom electrode (Ti/Pt). The current density after the breakdown corresponds to the source meter compliance limit. The inset in (b) shows an optical microscope image of a representative MIM structure fabricated on sapphire with CYTOP as the dielectric. Scale bar: 200 μm . (c) Comparison of the electric field at a current density of $10^{-5} \text{ A cm}^{-2}$ for different transferred gate insulators versus the relative dielectric constant. A blue square represents the average value from 13 devices (excluding the device with 221 nm thick CYTOP) measured in this work, where the error bar corresponds to the standard deviation, while gray circles denote reported data from the literature.^{14–16,19,20}

section. Figure 3c shows the breakdown fields at a leakage current density of 10^{-5} A cm^{-2} plotted against the relative dielectric constant, which includes the average value of 8.0 ± 1.2 MV cm^{-1} from all of the devices measured in this work (excluding the MIM device with 221 nm thick CYTOP, as this device remained stable without breakdown up to the maximum applied electric field of ≈ 9 MV cm^{-1}), along with the extracted results from reported studies on various transferred insulators^{14–16,19,20} evaluated in MIM configurations. The comparison reveals that the transferred CYTOP films exhibit exceptional insulating characteristics, sustaining among the highest breakdown fields reported for transferred dielectrics. The high breakdown field of CYTOP makes it a highly suitable gate dielectric for transistors, ensuring low leakage and stable device operation under high-voltage conditions. Furthermore, its low dielectric constant enables reduced parasitic capacitance, which is advantageous for high-frequency transistor operation and also for inter-metal dielectric applications, where it can minimize capacitance between densely packed interconnects. The reduction in capacitance mitigates resistance-capacitance delays, suppresses signal cross-talk, and lowers power dissipation, thereby enabling high-frequency and power-efficient operation.^{34–36}

3. H-TERMINATED DIAMOND FETS WITH TRANSFERRED CYTOP FILMS AS A GATE INSULATOR

To validate the effectiveness of our lamination-based approach and to demonstrate the formation of a high-quality dielectric/substrate interface, H-terminated diamond FETs were fabricated by employing CYTOP as the gate insulator. Owing to its ultra-wide bandgap, high thermal conductivity, high carrier mobility, and large breakdown field,³⁷ diamond has emerged as a promising candidate to fabricate FETs for advanced electronic applications.^{38–45} The H-terminated diamond exhibits high valence band maximum, which facilitates the generation of two-dimensional hole gas (2DHG) at the surface. This 2DHG can be generated either by applying a gate voltage^{39,43,44} or, more commonly, through surface transfer doping by exposing the H-terminated diamond surface to ambient air,⁴⁶ gases such as NO_2 and O_3 ,⁴⁷ or deposition of high-electron-affinity oxides like MoO_3 and V_2O_5 .⁴⁸ The surface transfer doping has widely been used to fabricate p-channel FETs, offering practical alternatives, given the high activation energies associated with conventional dopants in diamond.⁴⁶ However, the surface transfer doping introduces ionized acceptors or fixed negative charges on the diamond surface, which scatter carriers and limit device performance. To address these limitations, H-terminated diamond FETs were fabricated without surface transfer doping by processing the devices in an inert environment using h-BN as a gate insulator, which showed high channel mobility.^{39,44} Here, we use the transferred CYTOP film as a gate insulator while avoiding surface transfer doping by processing the lamination on H-terminated diamond in an inert environment. This offers a simple and large-area-compatible approach to fabricating high-performance H-terminated diamond FETs.

In the present work, (100)-oriented single-crystalline undoped diamond substrates grown by CVD were used. To define the active channel and nonconductive regions, nitrogen ion implantation was performed on diamond substrates by masking the desired regions for the active channel with patterned photoresist, as shown in Figure S3a.

Nitrogen-implanted regions in diamond maintain high resistivity even after H-termination and subsequent air exposure.^{49,50} Following implantation and photoresist mask removal, Ti/Pt (5 nm/5 nm) electrodes were patterned on the defined active channel regions (Figure S3b). The samples were then transferred to a microwave-plasma assisted CVD (MPCVD) system and annealed in a H_2 environment at a stage temperature of 650 °C for 35 min, followed by hydrogen plasma exposure at 570 °C for 15 min, enabling titanium-carbide (TiC) ohmic contact formation and H-terminated diamond surface. The H-terminated diamond was subsequently transferred to an Ar-filled glove box using a vacuum suitcase, where CYTOP lamination was carried out without air exposure to avoid surface transfer doping. The detailed procedures for FET fabrication are provided in Section 6.

Figure 4 presents the room-temperature electrical characteristics of a H-terminated diamond FET with a 90 nm thick CYTOP gate insulator (see also Section S4 and Figure S5 of the Supporting Information for the characteristics of second H-terminated diamond FET). The schematic of H-terminated diamond FET using the CYTOP gate insulator is illustrated in Figure 4a, while the optical microscope image of the FET is shown in Figure 4b. The output curves of the FET are shown in Figure 4c, in which the drain current (I_{DS}) was measured by sweeping the drain voltage (V_{DS}) from 0 to -30 V and then in the reverse direction at various gate voltages (V_{GS}), which were varied from $+2$ to -30 V in 2 V steps. These results show typical p-type FET behavior and negligible hysteresis. The output curves demonstrate clear current modulation across both the linear and saturation regions, confirming effective field-effect control of 2DHG at the diamond surface. The geometrical parameters of Hall-bar configuration, including the channel length (L_{G}), channel width (W_{G}), and the separation between voltage probes (L_{p}), were determined from optical microscope images, following the procedure described in our previous work.³⁹ For this particular device, L_{G} was estimated to be 117.5 μm , W_{G} was 8.4 μm , and L_{p} was 29.8 μm . As shown in Figure 4c, the drain current was normalized by dividing the values with W_{G} . The maximum drain current was observed to be -23 mA mm^{-1} at $V_{\text{DS}} = V_{\text{GS}} = -30$ V, which is considerably high given the relatively long gate length of 117.5 μm .

Figure 4d presents the transfer characteristic of the FET measured in a two-probe configuration, where the drain current is plotted on a logarithmic scale as a function of gate voltage at $V_{\text{DS}} = -30$ V, from which an on/off current ratio of 5.7×10^6 was extracted. The normalized hysteresis width, obtained from Figure 4d in the gate voltage range of 0.5 to -1 V, was found to be <5 mV (MV cm^{-1})⁻¹, which is comparable to the lowest values reported for 2D semiconductors employing the transferred gate insulators.^{14,18} The hysteresis width was normalized by dividing it by maximum applied field (i.e., maximum V_{GS} divided by the CYTOP thickness). The subthreshold swing (SS) from Figure 4d was determined to be 220 mV dec^{-1} , corresponding to a low interface trap density of $\leq 3 \times 10^{11}$ cm^{-2} eV^{-1} , which was obtained following the procedure described in Section S4 of the Supporting Information. The interface trap density in the present case is comparable to or lower than most reported values for H-terminated diamond FETs,^{39,45,51–54} which indicates that a clean and high-quality interface is achieved through our freestanding CYTOP transfer method and fabrication process that avoid ambient air exposure of the H-terminated diamond surface. The reduced trap density is

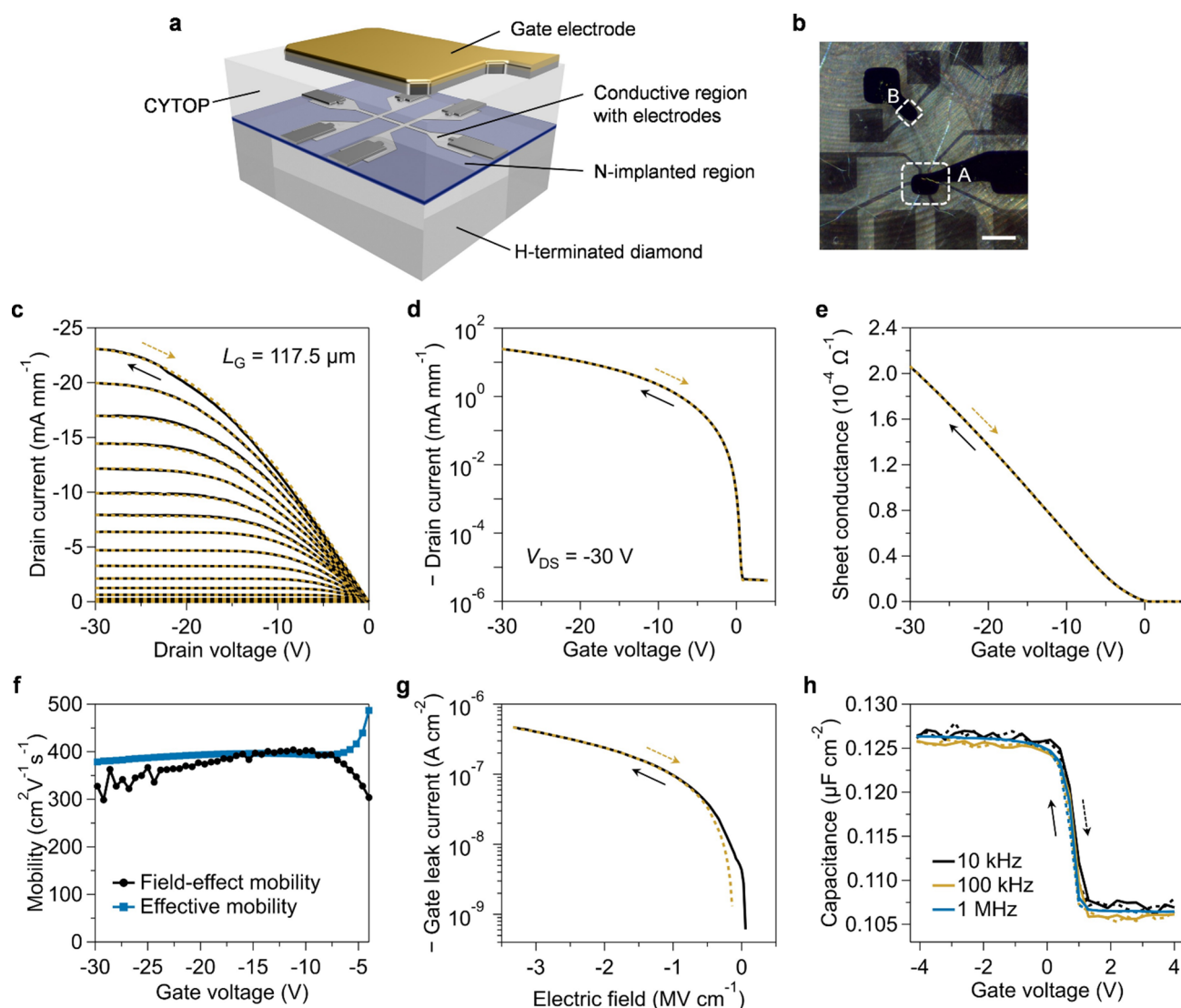


Figure 4. Electrical characteristics of the diamond FET with a CYTOP gate insulator at room temperature. (a) Schematic illustration of the CYTOP-gated diamond FET with Hall-bar geometry on diamond. (b) Optical microscope image of the FET. Scale bar: 200 μm . (c) Output characteristics showing drain current vs drain voltage for gate voltages varied from +2 to -30 V in 2 V steps. (d) Drain current versus gate voltage at a drain voltage of -30 V, with the gate voltage swept from +4 to -30 V and back. (e) Gate voltage dependence of sheet conductance in the linear region obtained from four-probe measurements, where the gate voltage was swept from +5 to -30 V and back. (f) Effective and field-effect mobilities as a function of gate voltage. (g) Gate leakage current density as a function of electric field. The electrical characteristics shown here were obtained for the device enclosed by dashed line A in (b), which has a gated Hall-bar structure as shown in (a). In (c), (d), (e), and (g), solid black and dashed brown lines correspond to forward and backward sweeps, respectively. (h) Capacitance–voltage (C – V) curves obtained from the three-terminal FET device enclosed by dashed line B in (b) at different frequencies, where solid and dashed lines represent the measurements from +4.0 to -4.1 V and from -4.1 to +4.0 V, respectively.

attributed to the nondestructive lamination of the CYTOP film, which substantially avoids any distortion on the H-terminated diamond surface in contrast to direct dielectric deposition, as well as to the inherent absence of dangling bonds in CYTOP. The sheet conductance shown in Figure 4e was measured using a four-probe configuration by sweeping V_{GS} from +5 to -30 V and then in the reverse direction, while applying V_{DS} of ± 100 mV. The maximum sheet conductance was $2.1 \times 10^{-4} \Omega^{-1}$, corresponding to a sheet resistance of 4.8 k Ω . By extrapolating the linear region of sheet conductance in the gate voltage range of -5 to -15 V, the threshold voltage (V_{th}) was estimated to be -2.3 V. Figure 4f presents the calculated field-effect

mobility ($\mu_{\text{FE}} = \frac{t_{\text{CYTOP}}}{\epsilon_{\text{CYTOP}}} \left| \frac{\partial \sigma}{\partial V_{\text{GS}}} \right|$) and effective mobility ($\mu_{\text{eff}} = \frac{t_{\text{CYTOP}}}{\epsilon_{\text{CYTOP}}} \frac{\sigma}{|V_{\text{GS}} - V_{\text{th}}|}$) as functions of gate voltage by following the reported procedure.³⁹ Here, t_{CYTOP} and ϵ_{CYTOP} are the thickness and dielectric constant of CYTOP films, respectively, and σ is the sheet conductance. The maximum effective mobility was calculated to be $\approx 400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. A maximum hole density reached $3.2 \times 10^{12} \text{ cm}^{-2}$ at $V_{\text{GS}} = -30$ V. The estimated mobility in CYTOP-based diamond FETs is significantly high and falls within the upper range of reported values using various gate insulators.^{39–45,51–54} The stability of the FET after long-term storage was also evaluated, demonstrating nearly identical

output and transfer characteristics, as discussed in Section S5 of the Supporting Information. Figure 4g shows the gate leakage current density as a function of electric field, where the leakage current was measured by shorting the source and drain electrodes and sweeping V_{GS} from +4 to −30 V and then in reverse direction. The leakage current was normalized to the active channel area under the gate electrode ($8.4 \times 10^3 \mu\text{m}^2$), and the gate voltage was converted to electric field by dividing by the CYTOP film thickness. The resulting current density remains below $5 \times 10^{-7} \text{ A cm}^{-2}$ at an electric field of 3 MV cm^{-1} . The electric field value is found to be larger than or comparable to those reported for diamond FETs using other gate dielectrics.^{51–58}

To further investigate the interface quality of CYTOP/H-terminated diamond, as well as the dielectric properties of the transferred CYTOP film, C – V measurements of the diamond FET were performed at different frequencies in the range of 10 kHz to 1 MHz in a N_2 -filled glove box, by sweeping V_{GS} in the range of +4.0 and −4.1 V in both forward and reverse directions. The C – V curves were obtained from a three-terminal FET device fabricated on the same substrate, as shown in Figure 4b. The channel width and length, in this case, are 41.9 and 8.4 μm , respectively. To minimize the influence of parasitic capacitances on the estimation of the insulator capacitance, the source and drain electrodes were electrically shorted during the measurements. Figure 4h presents the C – V characteristics obtained using an AC signal of 50 mV, measured across various gate voltages and frequencies, in which the capacitance was normalized to the channel area. Initially, the C – V measurements were performed between the gate and the shorted electrodes at frequencies ranging from 10 kHz to 1 MHz with the V_{GS} set to 0 V. Similarly, a series of measurements were performed over a gate voltage sweep from +4.0 to −4.1 V with a 0.3 V step. Figure 4h displays OFF-state and ON-state regions. For the case of 1 MHz frequency, the measured capacitance in the ON-state regime was found to be $0.126 \mu\text{F cm}^{-2}$ and remained relatively stable up to $V_{GS} = 0 \text{ V}$. As the device transitioned toward the OFF-state, the capacitance began to drop, reaching a steady value of $0.106 \mu\text{F cm}^{-2}$ at $V_{GS} = 1 \text{ V}$ and remains unchanged thereafter. The OFF-state capacitance arises due to the overlap of source–drain and gate electrodes, which also includes the parasitic contribution mainly from probe needles. Conversely, in the ON-state, the total measured capacitance includes both the OFF-state contribution and the capacitance of the gate dielectric corresponding to the conductive channel. Therefore, the capacitance of CYTOP can be estimated by subtracting the OFF-state value from the ON-state value. Hence, the capacitance associated with the CYTOP layer under the channel region is found to be $0.020 \mu\text{F cm}^{-2}$, which corresponds to a dielectric constant of $2.0 \epsilon_0$ (where ϵ_0 is the vacuum permittivity), given the CYTOP thickness of 90 nm. Notably, the dielectric constant remained consistent across different measurement frequencies and the value aligns well with reported values for CYTOP.²¹ The C – V measurements show nearly overlapping curves for the forward and reverse sweeps, which corroborate well with the transfer curve (Figure 4d) and further confirm a substantially low interface trap density at the CYTOP/H-terminated diamond interface.

4. DISCUSSION

The transfer and lamination method demonstrated in this work has broad applicability for the integration of fluoropolymer dielectric onto substrates that are considered incompatible with

conventional solution-based methods like spin coating or dip coating. For example, H-terminated diamond surfaces exhibit high water contact angles and strong liquid repellency,^{49,59} which leads to poor wettability and nonuniform film formation when polymer solutions are applied. By following our transfer method, CYTOP films were laminated on the H-terminated diamond without exposing the surface to ambient air or any solvents. Hence, this approach enables the integration of pre-formed and thermally cured dielectric films onto solvent- or heat-sensitive substrates without distorting the surface properties by any solvents and heat treatments. This method further holds significant promise for encapsulation and passivation in flexible electronics, in which solvent resistance and low-temperature processes are essential. Additionally, the transfer of CYTOP films may also be suitable for protecting moisture-sensitive devices due to their low water vapor permeability, and they also hold potential for optoelectronics and light-emitting devices owing to the high optical transparency of CYTOP. Furthermore, the lamination of CYTOP films onto diamond substrates may open new possibilities in quantum technologies, particularly in devices employing nitrogen vacancy (NV) centers in diamond for sensing or quantum information processing. Owing to the high optical transparency of CYTOP and nondestructive integration, it is expected to preserve the optical quality and spin coherence vital for NV center functionality.⁶⁰

From the electronic device perspective, the present study employed type-S CYTOP, which has been shown to exhibit an electron affinity of approximately 3.6 eV based on low-energy inverse photoelectron spectroscopy (LEIPS).⁶¹ Accordingly, the lowest unoccupied molecular orbital (LUMO) level of type-S CYTOP is estimated to lie near −3.6 eV with respect to the vacuum level, which is energetically higher than the valence band maximum (VBM) of H-terminated diamond (−4.2 eV).⁶² In addition, CYTOP exhibits optical absorption in the ultraviolet region below 200 nm,²¹ suggesting an energy gap between LUMO and highest occupied molecular orbital (HOMO) levels exceeding 6 eV. This indicates that the HOMO level of CYTOP is located significantly deeper than VBM of H-terminated diamond, thereby enabling stable p-channel FET operation. Under ideal conditions where the LUMO level of type-S CYTOP lies above the VBM of H-terminated diamond, electron transfer from the valence band of H-terminated diamond to the LUMO of S-type CYTOP is energetically unfavorable. Nevertheless, lamination of the CYTOP film onto H-terminated diamond induced a slight surface conductivity, as shown in Figure S4, although the conductivity remained significantly lower than that reported for other gate dielectrics such as Al_2O_3 .⁶³ The emergence of the surface conductivity may arise from charge trapping sites within the CYTOP film, which can accept electrons from the valence band of H-terminated diamond and generate holes at the diamond surface, similar to the surface transfer doping mechanism reported for H-terminated diamond with deposited gate dielectrics.⁴⁶ Such trapping sites in the CYTOP could originate from the distortion of polymer chains due to local strain,⁶⁴ or residual solvent and adsorbate species, although their exact origin and energetic distribution remain unclear at present. Further experimental and theoretical investigations are therefore required to clarify the electronic interactions responsible for the observed conductivity following CYTOP lamination. Other variants, such as type-M and type-A CYTOP, have been reported to exhibit

larger electron affinity values,⁶² positioning their LUMO level comparable to or below the VBM of H-terminated diamond. Therefore, direct lamination of these types of CYTOP on H-terminated diamond could lead to a more pronounced charge transfer even in the absence of charge trapping sites. This would enhance the generation of holes, but the increased amount of transferred charge in the CYTOP would act as a scattering source, limiting the hole mobility. An interesting future strategy for generating a high hole density while maintaining high mobility could involve a modulation doping scheme^{65,66} by stacking different types of CYTOP layers, where a low electron affinity CYTOP is first laminated on H-terminated diamond followed by a higher electron affinity CYTOP layer. Such a stacking approach enables the creation of functional heterostructures with well-defined layers, which are challenging to achieve by conventional solution-based methods due to intermixing of polymer molecules, and therefore offers an additional merit of the film transfer method.

5. CONCLUSIONS

In summary, we demonstrated a simple and effective approach for the transfer of freestanding low- κ amorphous fluoropolymer films, enabling their integration onto various substrates, including low-adhesive and sensitive substrates like H-terminated diamond. This process allows the transfer of CYTOP dielectric films in ambient air and inert atmospheres, without compromising the integrity of dielectrics or surface quality of the target substrate. The MIM structures fabricated by the integration of freestanding CYTOP films have shown high dielectric breakdown fields, indicating high quality and robustness of the insulator. Notably, p-channel FETs fabricated on H-terminated diamond using CYTOP gate insulators exhibit excellent electrical performance, including high hole mobility, negligible hysteresis, and substantially low interface trap density, validating the high-quality CYTOP/H-terminated diamond interface. Overall, these results validate the efficacy of the proposed transfer method and highlight the excellent dielectric properties of CYTOP films. This work establishes a promising large-area-compatible integration strategy, offering a new pathway for creating high-quality interfaces on sensitive surfaces, holding significant potential for utilizing CYTOP in a wide range of advanced electronic and optoelectronic applications.

6. EXPERIMENTAL SECTION

6.1. Preparation and Transfer Method of Freestanding CYTOP Films

3 wt % fluoropolymer solution was prepared by dissolving type-S CYTOP (CTX-809SP2)²¹ in the CT-Solv.180 solvent (both from Asahi Glass Co., Ltd., Japan). To ensure complete dissolution and homogenization, the solution was magnetically stirred for 2 h. Parallely, a 3 wt % PAA solution was prepared by dissolving PAA powder (average molecular weight = 5000 g mol⁻¹, Wako Pure Chemicals) in DI water. Single-side polished Si substrates with the approximate size of 2 cm × 2 cm were subjected to a sequential ultrasonic cleaning in DI water, isopropanol (IPA), acetone, IPA, and finally, DI water to remove organic and particulate surface contaminants. The substrates were then treated with oxygen plasma (20 sccm O₂ flow, 10 Pa chamber pressure, 250 W RF power, 3 min at room temperature) to further eliminate organic residues and enhance surface energy for better film adhesion. After plasma treatment, Si substrates were first coated with PAA solution by spin-coating at 3000 rpm for 60 s, followed by baking at 155 °C for 2 min to evaporate residual water and

enhance film integrity. Subsequently, the CYTOP solution was spin-coated onto the PAA layer under identical parameters and underwent stepwise thermal annealing: 50 °C for 10 min (solvent removal), 80 °C for 30 min (film densification), and 130 °C for 10 min (curing and mechanical reinforcement). This resulted in uniform and substantially smooth CYTOP films with an approximate thickness of 90 nm, suitable for exfoliation from the substrate by dissolving the PAA sacrificial layer. The thickness of CYTOP films can be controlled by varying the speed of spin coating (rotation speed) or the concentration of CYTOP solution.²¹ To enable exfoliation, high-temperature silicon-adhesive double-sided Kapton tape (KTP36-3/4SD, TECSAM, Japan; maximum operating temperature 260 °C) was cut to ≈1.9 cm × 2.5 cm with a central ≈6 mm × 6 mm aperture, forming a transfer window, and affixed onto the CYTOP film. Although the Kapton tape is double-sided, only one side was used, leaving the protective layer on the opposite side intact. The resulting Kapton/CYTOP/PAA/Si stack was floated on a DI water bath at 50 °C to accelerate dissolution of the underlying PAA layer. After complete PAA dissolution, the Si substrate was detached, leaving the Kapton-supported CYTOP film floating on the water surface. For improved alignment and handling, the freestanding CYTOP film was mounted onto a 2 mm thick copper frame (2.6 cm × 8.6 cm) containing a 4.5 mm circular aperture near one edge. For the transfer or lamination of freestanding CYTOP films onto the target substrate, an x-y-z direction movable stage to hold the copper frame was used, while the target substrate was mounted on an adjacent stage (equipped with x-y translation and rotation adjustment) with vacuum chuck for stable lamination under an optical microscope (Figure 2).

6.2. Characterization of CYTOP Films

The CYTOP film thickness was measured using Thickness Monitor FE-3000 (Otsuka Electronics), with refractive index values of CYTOP²¹ calibrated for the relevant spectral range. A thickness variation of ±5 nm was observed across samples prepared from separate CYTOP solutions with identical spin-coating parameters, confirming the process reproducibility. Furthermore, the thickness measurements conducted at multiple locations on the same sample showed a negligible variation of ±0.6 nm, indicating the overall uniformity of CYTOP films. The thickness of the PAA layer was measured using Bruker's DektakXT profiler, which was estimated to be 33 ± 4 nm. AFM was performed using AFM5100N (Hitachi High-Tech) to evaluate surface morphology and roughness. MIM structures were fabricated using CYTOP as the dielectric film on polished sapphire substrates with an approximate size of 2 mm × 2 mm × 0.5 mm. The substrates were cleaned by dipping in a base Piranha solution consisting of DI water, ammonium hydroxide, and hydrogen-peroxide at 80 °C, followed by the ultrasonic cleaning in organic solvents, as mentioned above. Bottom electrodes were patterned with the widths of 5 μm and 10 μm on the same substrate (inset of Figure 3b) using maskless laser lithography (DL-1000, Nano System Solutions) and metal (Ti/Pt, 5 nm/5 nm) deposition via e-beam evaporation. The CYTOP film was laminated onto the patterned substrate by following the transfer method described above, and the top electrodes (Al/Au, 50 nm/100 nm) were deposited through a shadow mask using a custom-built thermal evaporator to complete the MIM devices. To determine the current density, the overlapping area of CYTOP films between bottom and top electrodes was estimated from optical microscope images by plotting brightness versus distance and fitting the resulting profile using an error function.³⁹

6.3. H-Terminated Diamond Field-Effect Transistors

CVD-grown standard grade Ila-type (100) single-crystalline diamond substrates, procured from Element Six, were employed to fabricate FETs in this study. The diamond substrates were polished to minimize surface roughness and diced into pieces of approximately 2.2 mm × 2.2 mm × 0.5 mm. The substrates were then subjected to sequential ultrasonic cleaning in DI water, IPA, acetone, IPA, and DI water to remove organic and particulate contaminants. To isolate device regions, nitrogen ion implantation (¹⁵N, 10 keV, 1 × 10¹⁴ ions cm⁻²)

was performed at room temperature by partially covering diamond with photoresist to protect the channel region. After the implantation, the photoresist mask was removed and substrates were cleaned using a hot acid mixture ($\text{HNO}_3\text{:H}_2\text{SO}_4 = 1\text{:}3$) at 200 °C for 30 min, followed by a final organic cleaning step. The electrodes were patterned for electrical measurement using laser lithography and subsequent deposition of Ti/Pt (5 nm/5 nm) using e-beam evaporation. After formation of Ti/Pt electrodes, the sample was transferred to an MPCVD (Seki Technotron, AX-5000) system and annealed in H_2 gas at a temperature of 650 °C for 35 min. After annealing, the sample was exposed to hydrogen plasma at 570 °C for 15 min with a hydrogen flow rate of 500 sccm and chamber pressure of 27 Torr. These steps facilitated the formation of TiC-based ohmic contacts and hydrogen termination of the diamond surface, as reported previously.³⁹ Note that during the hydrogen plasma treatment, the actual diamond surface temperature reached approximately 700–750 °C, as measured by a pyrometer. After H-termination, the diamond substrate was transferred to an Ar-filled glove box using a vacuum suitcase, without exposing the diamond surface to the ambient air. The vacuum suitcase is equipped with a nonevaporable getter (NEG) pump, which maintains pressure below 1×10^{-7} Torr. The high purity of Ar inside the glove box was maintained by circulating the Ar gas through a purifier, which maintained oxygen and water contents below 0.5 and 2 ppm, respectively. In order to remove any atmospheric adsorbates, the freestanding CYTOP film supported by the copper frame was baked inside an Ar-filled glove box at temperatures of 80, 100, and 120 °C for 3 min each to remove atmospheric adsorbates before transferring the H-terminated diamond from the vacuum suitcase. No change in the purity of Ar was observed inside the glove box during the CYTOP film baking, suggesting minimum adsorbates on the film. After this step, the H-terminated diamond was immediately transferred to the Ar-filled glove box and CYTOP lamination was performed, following the methodology described above. The lamination was completed within 5 h after transferring the diamond from the MPCVD system to the Ar-filled glove box. Following lamination, a metal shadow mask was fixed to the sample inside the glove box. The sample was then transferred via a vacuum suitcase to a thermal evaporator, where the gate electrode (Al/Au, 50 nm/100 nm) was deposited. Finally, the completed FET device was transferred via a vacuum suitcase to a N_2 -filled glove box for electrical characterization.

6.4. Electrical Measurement Setup

The electrical measurements were performed inside the N_2 -filled glove box using a probe station by directly touching the gold-alloy probe needles with a tip diameter of 20 μm to the electrode pads on the substrate. The output and transfer characteristics were measured on the gated Hall-bar sample (Figure 4b) in a two-probe configuration, while the gate voltage dependence of sheet conductance was measured on the same sample in a four-probe configuration. Output characteristics were obtained using a source measure unit (Keysight Technologies, B2901A) for gate biasing, a source meter (Keithley Instruments, 2410) for drain voltage, and a current preamplifier (DL Instruments, 1211) to measure the drain current. Transfer characteristics were obtained by sweeping the gate voltage with the source measure unit while applying a fixed drain voltage via the source meter, with the drain current recorded using an electrometer (Keithley Instruments, 6514). For the measurements of the gate voltage dependence of sheet conductance, the gate bias was applied using the source measure unit, while the drain voltage was provided by a function generator (Agilent Technologies, 33220A). A voltage amplifier (DL Instruments, 1201) and the current preamplifier were used to measure longitudinal voltage and drain current, respectively. The sheet resistance was obtained by applying a voltage of ± 100 mV between source and drain electrodes. Sheet resistance (ρ) was calculated using the formula $\rho = (V_{p+} - V_{p-}) / (I_{D+} - I_{D-}) \times (W_G/L_p)$, where V_{p+} and V_{p-} are the measured voltages across the longitudinal probes for positive and negative drain currents, I_{D+} and I_{D-} , respectively. The sheet conductance (σ) was calculated as

the reciprocal of ρ . To measure the gate leakage current, the source and drain electrodes were shorted together and the current was measured while applying voltage to the gate electrode. The capacitance–voltage characteristics were measured using a precision impedance analyzer (Agilent Technologies, 4294A). To minimize the effects of parasitic capacitance, coaxial probe needles were employed, in which only a small portion of the gold-alloy needle was exposed.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsami.6c05045>.

Photographs of the transfer process, AFM analysis, optical microscope images detailing each step of device fabrication, a brief description of the device isolation procedure, FET characteristics of an additional device, a comparative figure of interface trap density in diamond FETs, and measurements demonstrating the stability of FETs after long-term storage (PDF)

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Notes

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