

Supplementary Information - Moving Beyond Scotch Tape: Scalable Transfer of Research-grade CVD Graphene

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Methods

Single crystal Cu(111) thin film epitaxy on sapphire

Epi-polished 50.8 mm sapphire wafers diced along the c-plane (AdValue Technology SS-1WCF-2-50) were first cleaned by annealing at 1000 °C for 12 h in a pure oxygen atmosphere, following previous reports [1]. Each wafer was immediately loaded into a magnetron sputtering system (AJA Orion 3) until base vacuum was achieved (1×10^{-8} Torr), and a 1000-nm-thick Cu film was deposited with the following conditions: RF power 125 W, deposition rate 0.23 nm/s, argon partial pressure of 4 mTorr, substrate rotation speed of 0.67 Hz, and chamber temperature of 20 °C. The wafer was then left in the chamber overnight to cool. To promote Cu recrystallization, each wafer was then annealed at 1025 °C with 50 sccm Ar and 50 sccm H₂ at atmospheric pressure for 1 h with rapid cooling. Each Cu(111)/sapphire wafer was diced into 6 mm $\times$ 6 mm squares.

OF-CVD graphene growth

The furnace was first heated to 500 °C in 100 mTorr H₂ (ULSI-6N) and held for 30 min for sample annealing. The temperature was then ramped to 1000 °C with 100 mTorr H₂ and held for 10 min for a stabilization period. Next, 5 % CH₄ (ULSI-6N) diluted in argon (ULSI-6N) was introduced into the growth chamber for the specified growth time 10 min. Finally, methane flow was cut off and a linear actuator quickly moved the furnace away from the growth region, facilitating rapid cooling to room temperature under 600 mTorr H₂.

Ni deposition

After graphene synthesis, the samples were quickly loaded into a UHV electron-beam evaporation chamber (Angstrom Engineering Nexdep). Ni was then deposited directly on the graphene in a pulsed scheme to reduce lattice damage (Fig. S1a-b) with the following condi-

tions: deposition rate 2 Å/s, deposition time 50 s, rest time of 30 min, and total film thickness of 40 nm. We found that 40 nm was the lowest thickness where we reliably obtained a uniform, crack-free film. To further prevent graphene damage, a neodymium permanent magnet was placed close to the graphene sample to deflect secondary electrons (Fig. S1c-d).

SiNx shadow mask fabrication

Silicon nitride (SiNx) shadow masks were fabricated using standard bulk Si micromachining protocols. Membranes were lithographically defined (Heidelberg DWL 66+; S1805 photoresist, 4000 rpm) on the backside of lightly boron-doped (10-20 $\Omega\cdot\text{cm}$) Si wafers coated with 200 nm of ultra-low-stress, nonstoichiometric SiNx on both sides (Ted Pella). The SiNx was completely etched with a CHF_3/O_2 RIE process for 90 seconds (Oxford PlasmaPro 80 Cobra RIE; 80/15 sccm gas flow, 15 mTorr operating pressure, 300 W ICP, 20 W table RF power). After ashing the photoresist, anisotropic Si etching with potassium hydroxide (KOH; 45 wt%, 80°C) yielded free-standing SiNx membranes. The membranes were flipped, and frontside features were patterned using the same procedure. Following shadow mask fabrication, Cr/Au (4/11 nm) was deposited via e-beam evaporation on both sides to facilitate Ni deposition. During Ni deposition, the SiNx shadow mask was adhered to the sample using a standard metal clip with extra care to not laterally slide the mask during mounting.

Ni transfer

Polypropylene carbonate (PPC) (rotation speed 4000 rpm, 1 min, bake at 180 °C, 10 min) was coated on the Ni/Gr/Cu sample. The bottom sample face was then epoxied (JB Weld ClearWeld) to a glass slide and left 1 hour to cure. Thermal release tape (TRT - Revalpha 3193MS (4M)) was then adhered to the PPC layer. A glass slide was then epoxied to the TRT top surface with another 1 hour cure time to create a stable handle for exfoliation. The top glass slide was then hand-pulled directly upward without rotation to exfoliate the

TRT/PPC/Ni/Gr from the Cu surface. The glass-slide/TRT/PPC/Ni/Gr was then quickly adhered to a hexamethyldisilazane (HMDS) treated $\text{Si}^{++}/\text{SiO}_2$ substrate (oxide thickness 285 nm). The glass-slide/TRT was removed by heating the sample to 155 °C for 1 min. PPC and other tape residues were mostly removed by 70 °C acetone for 60 min. The remaining polymer residue was removed using a gentle plasma process: 20 W table power, 100 mTorr process gas pressure, $\text{O}_2:\text{Ar}$ (40:10 sccm), 20 sec process time, 60 sec rest, 30 cycles in an ICP-RIE system (Oxford Plasmalab 100). The Ni was then etched using 1:1 HCl:DI water for 20 min and rinsed with DI water. Without drying, the sample was then submerged in a dilute piranha solution (20:5:75 mL $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{DI}$ water) for 10 sec with three rinses in DI water to remove etchant residues.

Wet transfer on SiO_2

The Gr/Cu(111) film was first mounted to a glass slide on all sides with polyimide tape prior to polymer spinning. A thin layer of PMMA (495 PMMA A4 from Kayaku, rotation speed 4000 rpm, 1 min, bake at 140 °C, 2 min) was spun followed by a thick layer of paraffin for structural support. First, the paraffin pellets (Sigma-Aldrich #18634) were heated at 110 °C while the PMMA covered sample was heated to 50 °C to prevent paraffin solidification. Then the paraffin was quickly spun at a rotation speed of 1000 rpm for 10 s without further baking. The sample was then submerged in APS-100 copper etchant until the Cu was completely etched allowing the PMMA/Gr to float to the liquid surface. The sample was rinsed with DI water 5× and transferred to a HMDS treated $\text{Si}^{++}/\text{SiO}_2$ substrate. The HMDS treatment along with the stiff paraffin layer were crucial steps to avoid trapped water in the Gr/ SiO_2 interface. The sample was left to dry for 24 h at room temperature. The sample was submerged into acetone to remove the PMMA layer thus lifting the entire paraffin layer off. Finally, the sample was rinsed with IPA and dried with N_2 .

Atomic force microscopy

Atomic force microscopy (AFM) measurements were performed using a Park FX40 AFM system in tapping/NCM mode with SSS-NCHR probes (Nanosensors). Lateral force microscopy (LFM) measurements were performed using a Jupiter XR Asylum Research AFM system with AC240 tips under a bias voltage of 750 mV. Measurements were performed at room temperature (300 K).

Raman spectroscopy

Raman characterization of Gr/SiO₂ and Gr/Cu was performed using a commercial Renishaw inVia Raman spectrometer with 532 nm excitation and collection in a 180-degree back-scatter geometry (1800 lines/mm grating). Measurements were performed under ambient conditions.

Device fabrication

Polydimethylsiloxane (PDMS) for the glass transfer slides was prepared from SYLGARD 184 by mixing ten parts base and one part curing agent. The PDMS was then mixed well and placed in a vacuum desiccator for bubble reduction. The resulting mixture was poured into a plastic Petri dish and cured at 60 °C for 48 h. To create a glass slide for transferring hBN onto the graphene surface, PDMS was cut into a 2 mm × 2 mm cube and gently mounted onto a glass slide. A liquid PDMS drop was introduced onto the cube with curing at 60 °C for 2 h to impose the top surface with a larger curvature to finely control layer-by-layer pickup. Liquid polycarbonate (PC) in chloroform (10 wt%) layer was sheared between glass slides, released with a hole-punched Scotch tape, and then transferred to the PDMS surface. The final PC/PDMS slide was heated at 180 °C for 1 min to flatten the top surface.

Both monolayer graphene devices (Si⁺⁺/SiO₂ and dual-graphite-gated) were assembled using the van der Waals dry transfer technique [2] at temperatures ranging from 90 to 130 °C. After assembly, the heterostructure was released onto a silicon substrate with 285 nm of thermal

oxide at 180 °C and rinsed with chloroform for 1 hour.

The $\text{Si}^{++}/\text{SiO}_2$ -gated device was etched into a Hall bar geometry using reactive ion etching with SF_6 and O_2 plasmas. The metal electrodes to the graphene were deposited using electron-beam evaporation consisting of (Cr/Au) 2 nm/60 nm (inset of Fig. S10a).

The dual-graphite-gated device was etched into a Hall bar geometry using reactive ion etching with SF_6 and O_2 plasmas (Fig. S11b). The metal electrodes to contact the gates and graphene contacts were deposited using electron-beam evaporation consisting of (Cr/Pd/Au) 2 nm/20 nm/70 nm (Fig. S11c). A final trench-style etch was made to electrically isolate the top graphite gate from the graphene channel (Fig. S11d).

Electrical characterization

The $\text{Si}^{++}/\text{SiO}_2$ -gated monolayer graphene device was measured in a 4He cryostat with a base temperature of 1.6 K with a superconducting magnet up to 12 T. The carrier density was tuned by applying voltage on the $\text{Si}^{++}/\text{SiO}_2$ gate. The dual-graphite-gated monolayer graphene device was measured in a 3He cryostat with a base temperature of 300 mK with a superconducting magnet up to 15 T. Four terminal resistance measurements were carried out using a low-frequency lock-in technique at a frequency of 17 Hz. The carrier density was tuned by applying voltage on one of the graphite gates while holding the other constant with a DC source meter (Yokogawa). A large voltage (40 V) was applied to the Si^{++} gate to heavily dope the graphene region that was not covered by the bottom graphite gate to reduce contact resistance.

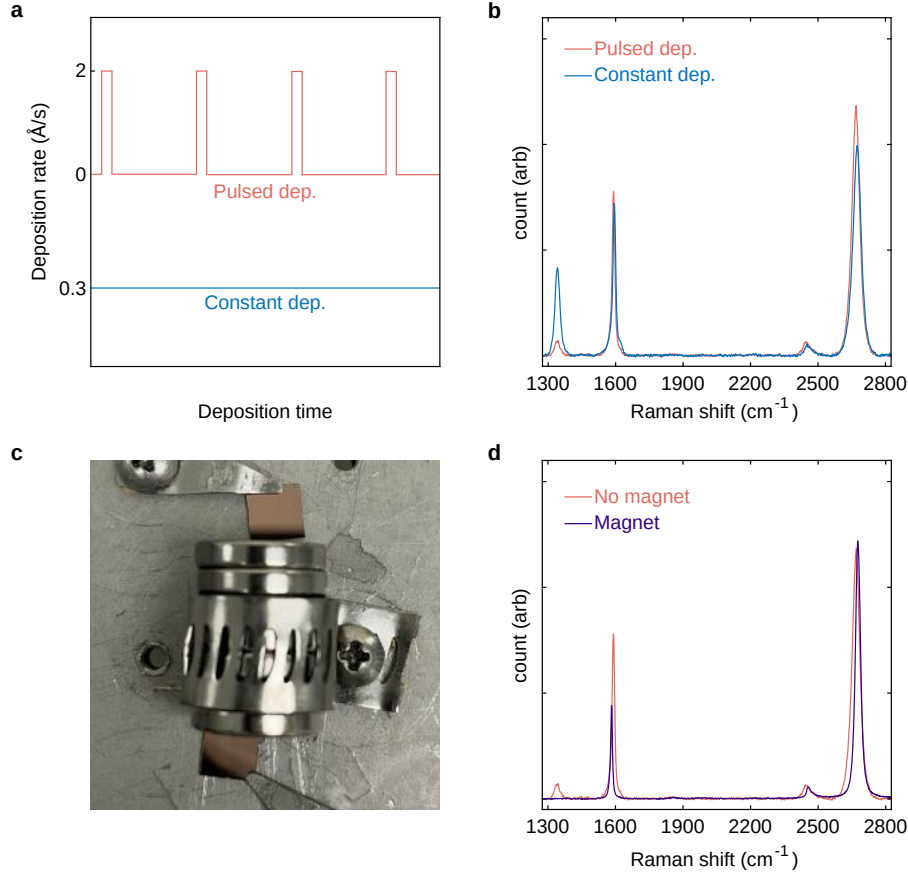


Figure S1: **Effect of Ni deposition conditions on graphene quality.** **a**, Deposition rate as a function of deposition time for a fixed rate and pulsed rate procedure. **b**, Raman spectra for a graphene sample transferred to SiO₂ using either a constant (blue) or pulsed (orange) Ni deposition process. The D peak is significantly reduced when using the pulsed deposition technique ($I_D/I_G = 0.57$ reduced to $I_D/I_G = 0.1$). **c**, Optical image of the neodymium permanent magnet used to screen secondary electrons during deposition. **d**, Raman spectra for a graphene sample transferred to SiO₂ either utilizing (purple) or not utilizing (orange) the magnet during Ni deposition process. The D peak is further reduced when using the magnet during deposition ($I_D/I_G = 0.1$ reduced to $I_D/I_G < 0.013$). For **d**, the pulsed deposition technique was used for both samples.

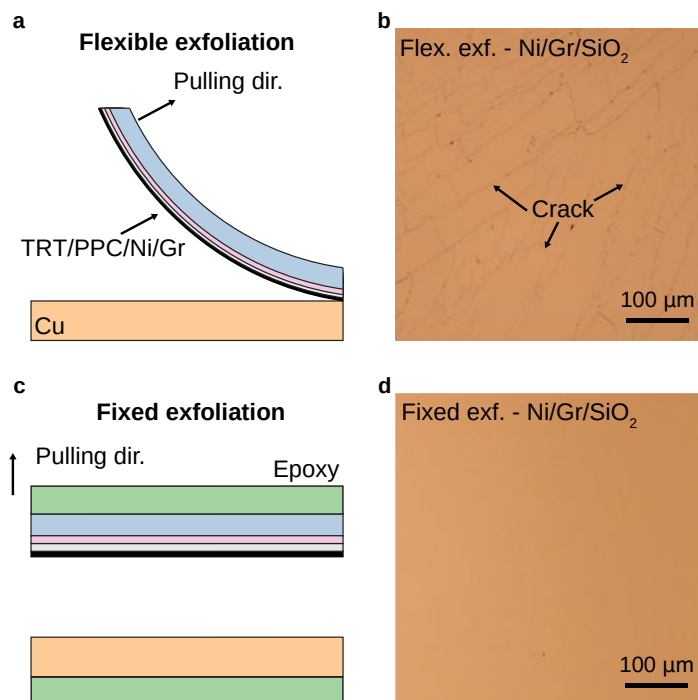


Figure S2: **Graphene crack reduction from exfoliation method.** **a**, Flexible Ni exfoliation highlighting a large bending curvature. **b**, The resulting Ni/Gr film on SiO₂ has widespread cracks during flexible exfoliation and lamination. **c**, Fixed Ni exfoliation with epoxy used on both the tape and substrate to reduce excessive stress in the Ni/Gr film. **d**, Optical image of the crack-free Ni/Gr film on SiO₂ when using fixed exfoliation.

The releasing method of Ni/Gr structure from the Cu substrate can affect the overall film quality. By exfoliating the Ni/Gr film with the use of a flexible thermal release tape (TRT), the metal film undergoes substantial flexural stress leading to widespread cracks in the Ni/Gr film (Fig. S2a,b). Epoxy was then used to secure the substrate and provide rigidity to the TRT thus minimizing crack formation (Fig. S2c,d).

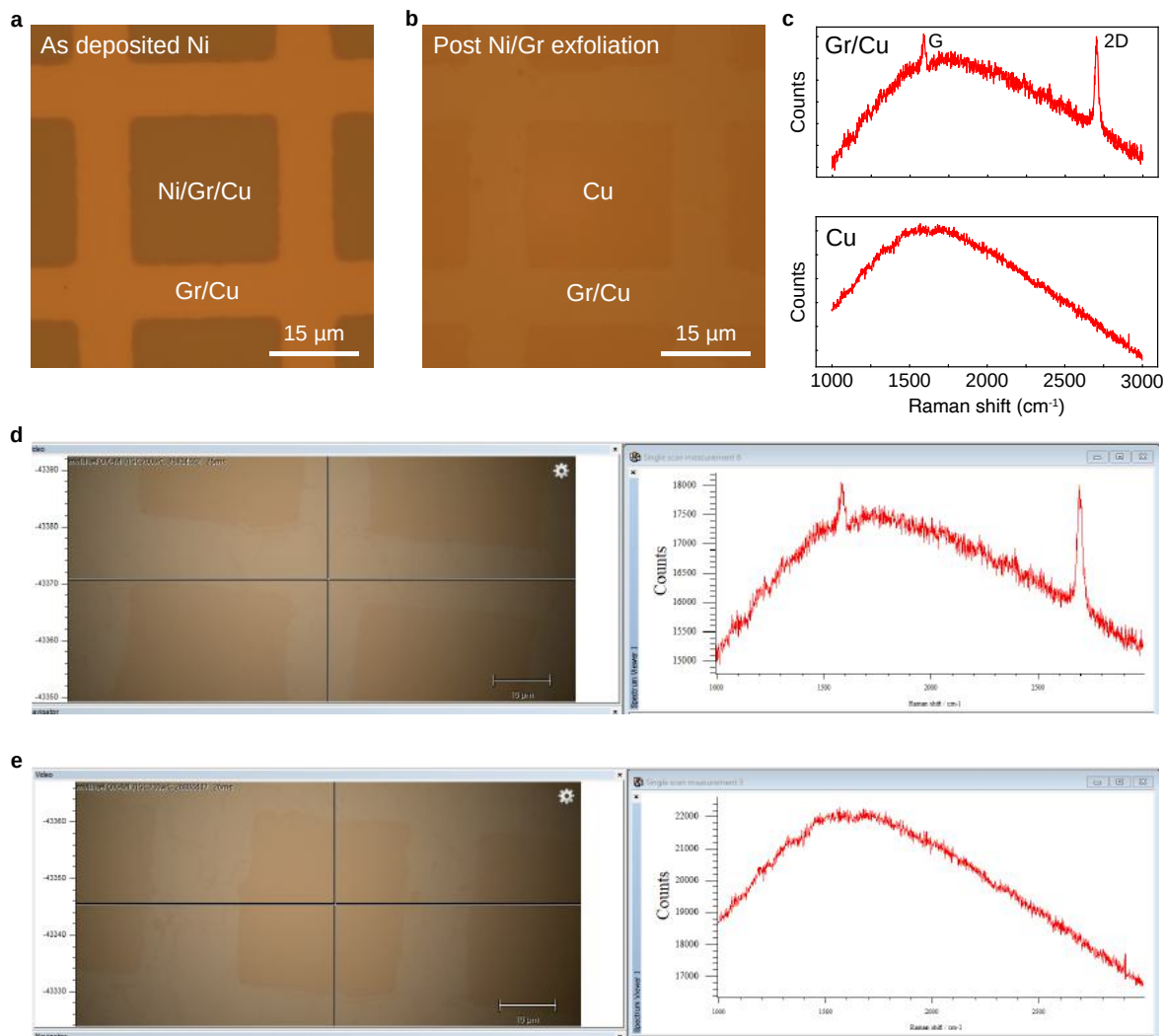


Figure S3: **Evidence of patterned graphene removal after Ni transfer.** **a**, Optical image of a square Ni/Gr/Cu array after metal evaporation. **b**, The same region after Ni/Gr exfoliation. The sample was oxidized in air (200 °C, 3 min) to increase the contrast between the bare Cu and graphene covered Cu. **c**, Raman spectra of the Cu/Gr and Cu spots seen in **(b)** collected with 532 nm excitation (0.06 mW, 120 second exposure, 1 accumulation). **d-e**, Images from the Renishaw inVia interface during the acquisition of the data seen in **(c)**.

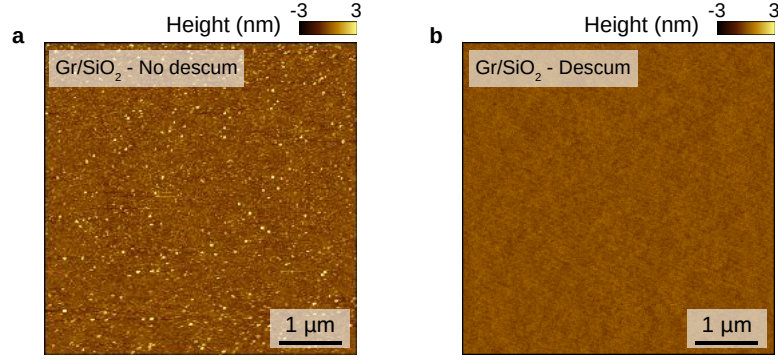


Figure S4: **The effect of descum techniques on graphene cleanliness.** **a**, AFM image of a large-area graphene film on SiO₂ in which only acetone was used to clean the Ni film prior to HCl treatment. **b**, AFM image of a large-area graphene film on SiO₂ where in addition to acetone, a gentle O₂/Ar plasma was performed prior to Ni etching in HCl. After HCl, the sample in **(b)** was cleaned in a dilute piranha solution for 10 seconds.

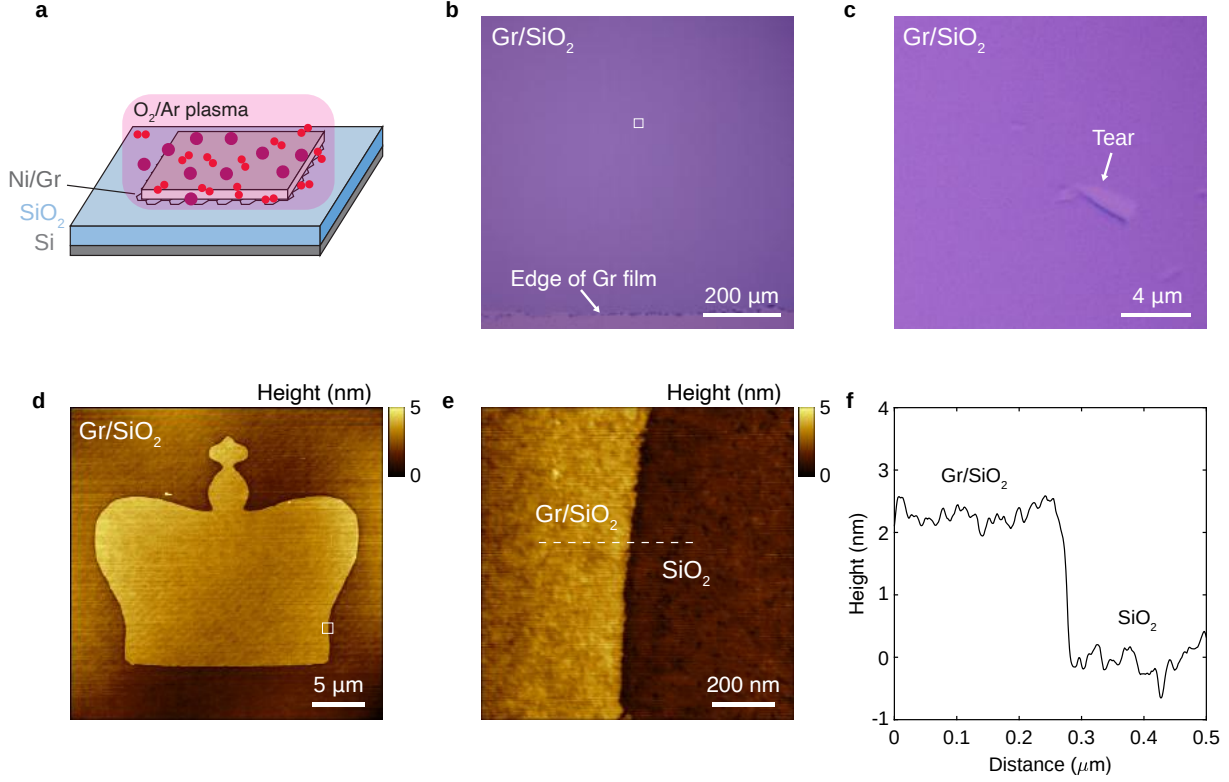


Figure S5: **Step height considerations of Ni transfer.** **a**, Illustration depicting the RIE process to descum the Ni film with O₂/Ar plasma prior to Ni etching. **b**, Large-area graphene film after Ni etching. **c**, Small tear in the graphene film located within the white box in **(b)** used for thickness characterization. **d**, AFM image of a graphene crown transferred to SiO₂. **e**, Magnified AFM scan of the edge profile region marked with a white box in **(d)**. **f**, Linecut of the edge profile shown by a white dashed line in **(e)**.

To ensure the final graphene films remained clean, a gentle plasma descum process was performed on the Ni/Gr structure prior to Ni etching (Fig. S5a). The physical bombardment of the argon ions within the plasma etches both the Ni and SiO₂ surfaces. Therefore, an artificial step height at the Gr/SiO₂-SiO₂ boundary will be present due to SiO₂ etching. To determine the true graphene film thickness, a local tear within the otherwise pristine boundary was mapped via AFM and depicted in the main text figure 1e (Fig. S5b-c). This tear occurred after the RIE etching, therefore, it is not influenced by argon ion-based etching. The artificial step height from plasma descum was characterized further on a crown patterned graphene transfer (Fig. S5d). A magnified AFM scan of the the white box in Fig. S5d illustrates that the Gr/SiO₂-SiO₂ boundary height is ~ 2 -3 nm (Fig. S5e-f).

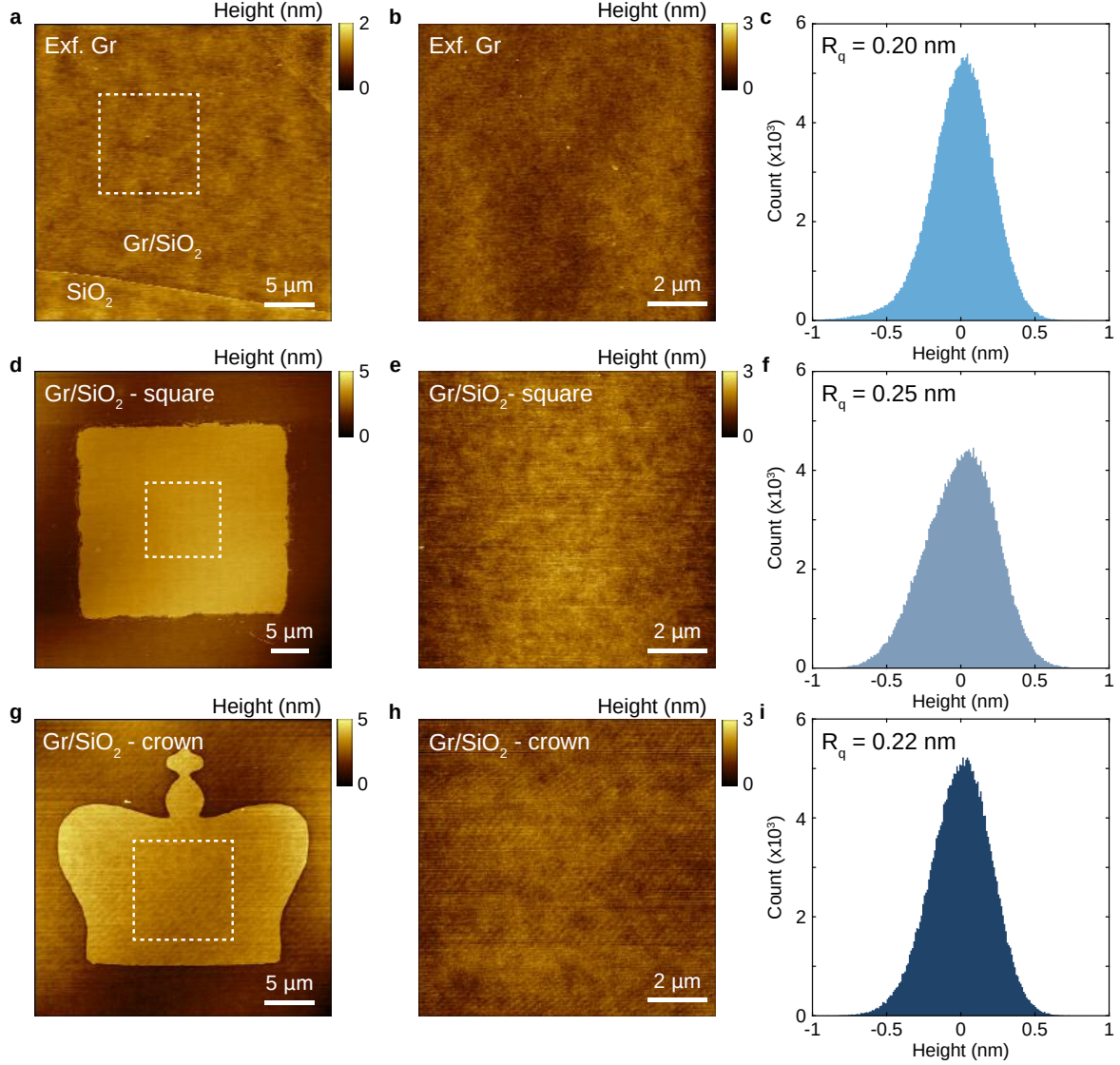


Figure S6: AFM analysis of patterned graphene transfer. **AFM analysis of patterned graphene transfer.** **a**, AFM image of a mechanically exfoliated graphene flake on SiO_2 . **b**, Zoomed in AFM image of the interior area of the white dashed box seen in **(a)**. **c**, Histogram of measured Z-height collected in **(b)**. **d**, AFM image of a square graphene pixel transferred to SiO_2 via technique 2. **e**, Zoomed in AFM image of the interior area of the white dashed box seen in **(d)**. **f**, Histogram of measured Z-height collected in **(e)**. **g**, AFM image of a graphene square transferred to SiO_2 via technique 3. **h**, Zoomed in AFM image of the interior area of the white dashed box seen in **(g)**. **i**, Histogram of measured Z-height collected in **(h)**.

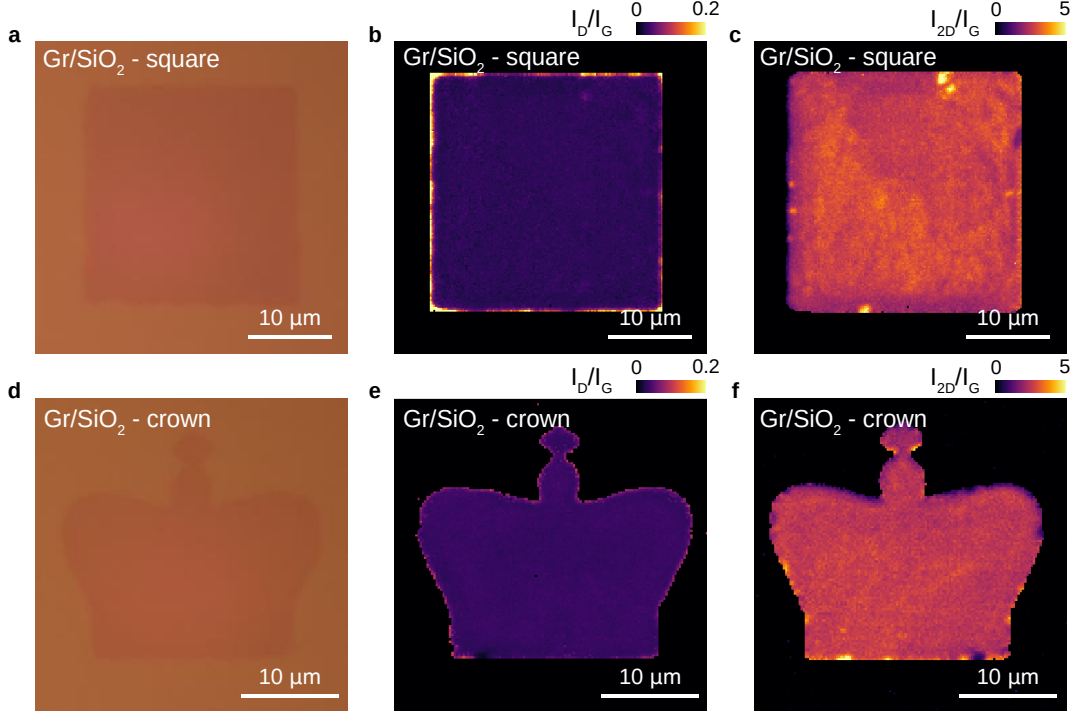


Figure S7: **Raman analysis of patterned graphene transfer.** **a**, Optical image of a graphene square transferred to SiO₂ via a TEM grid shadow mask. **b-c**, Raman I_D/I_G and I_{2D}/I_G of the transfer seen in **(a)** collected with 532 nm excitation (0.6 mW, 1 second exposure, 1 accumulation, $N = 32,761$ (including the surrounding black region)), respectively. **d**, Optical image of a graphene crown transferred to SiO₂ via a SiN_x/Si shadow mask. **e-f**, Raman I_D/I_G and I_{2D}/I_G of the transfer seen in **(d)** collected with 532 nm excitation (0.6 mW, 1 second exposure, 1 accumulation, $N = 21,316$ (including the surrounding black region)), respectively.

I_D/I_G maps shown in figure S7b,e depict the spread of graphene defects throughout the patterned films. For points where the D peak intensity is below the noise floor of the tool ($I_D < 100$ counts) and thus not fittable, I_D was derived by averaging the intensity from wavenumbers 1340 to 1360 cm⁻¹. The edge of the graphene does incur significant damage from the patterning process with $I_D/I_G > 0.1$. The high and uniform 2D-to-G peak ratio ($I_{2D}/I_G \sim 3$) points to minimal strain/doping disorder (Fig. S7c,f).

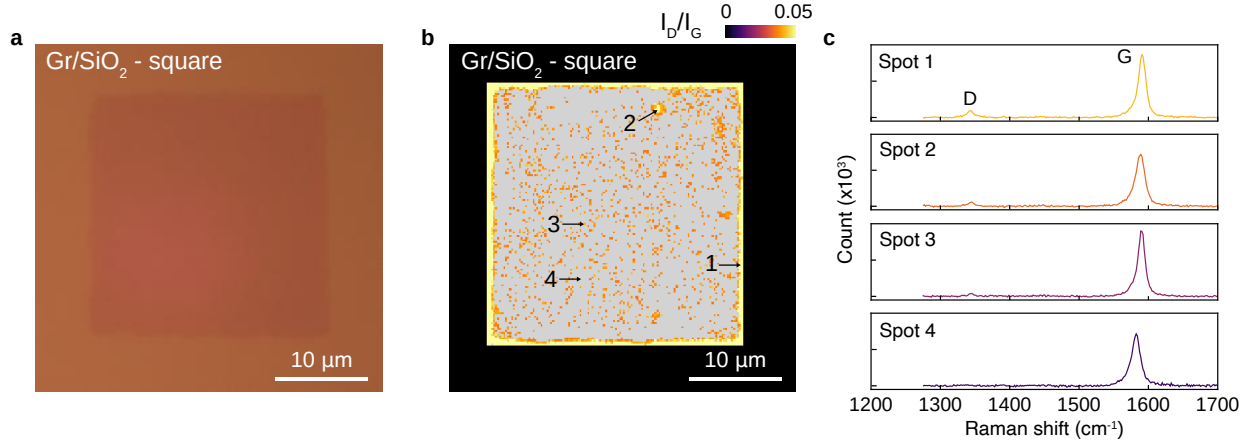


Figure S8: **Defect characterization via Raman spectroscopy.** **a**, Optical image of the graphene square seen in Fig. S7(a). **b**, I_D/I_G mapping now excluding all points within the interior where the D peak is below the noise floor of the tool ($I_D < 100$ counts). **c**, Raman spectra narrowed around the D and G peaks at spots 1-4 shown in (b).

Figure S8b replots the I_D/I_G data from figure S7b over a narrower range (0 to 0.05). Four representative spectra corresponding to the points indicated are shown in Fig. S8c. The edges of the square (Spot 1) and a single spot within the interior (Spot 2) show I_D/I_G of $0.05 \sim 0.08$. Roughly 7% of the interior points (Point 3) show fittable D peaks, with I_D/I_G of $0.035 \sim 0.05$. For the remainder of the interior points (Point 4), no D peak can be identified, i.e. I_D is below the noise floor and $I_D/I_G < 0.035$. These points are colored gray in Fig. S8b to represent that no value of I_D/I_G can be accurately assigned.

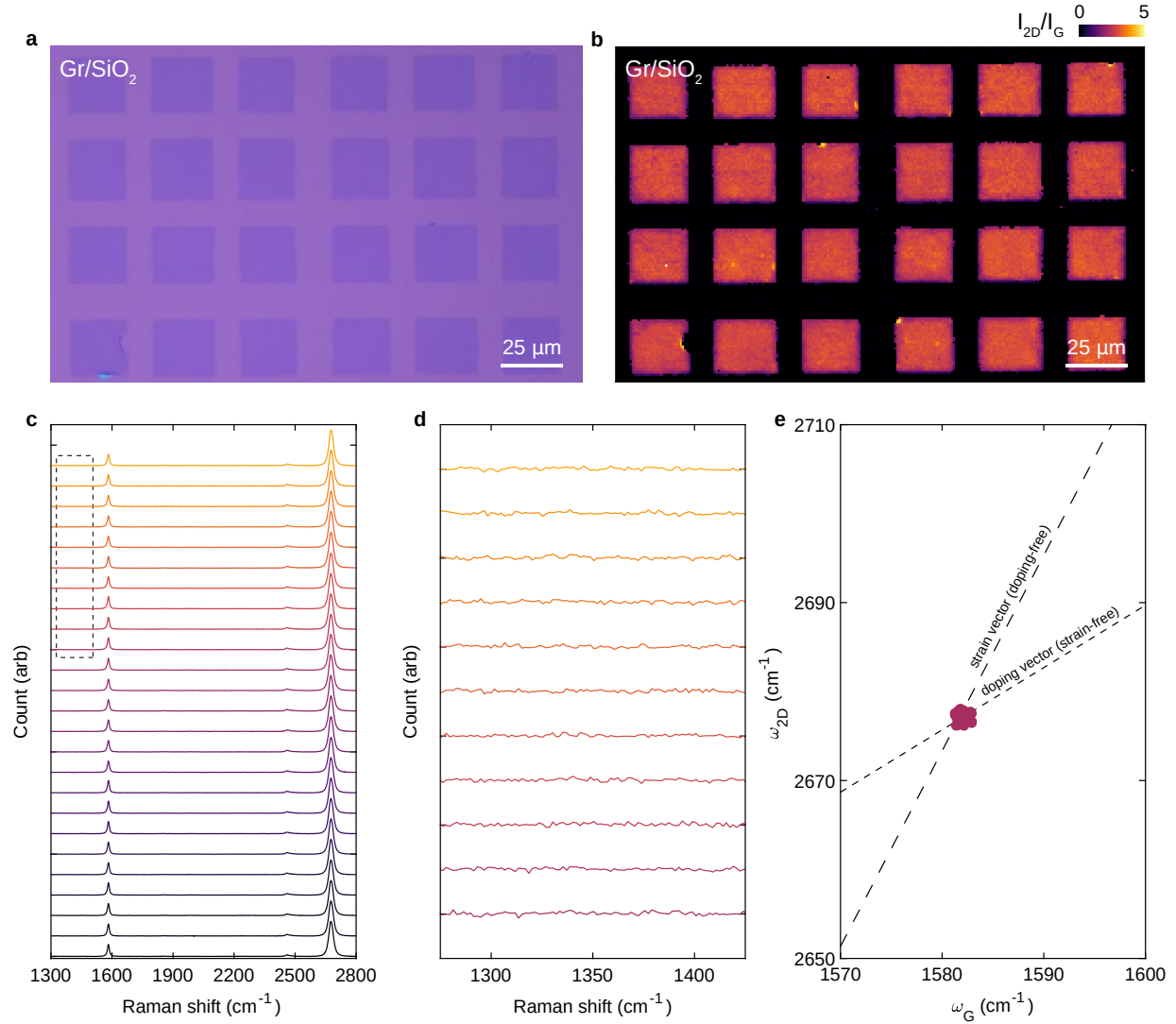


Figure S9: **Raman analysis of patterned graphene array transfer.** **a**, Optical image of an array of graphene transferred to SiO_2 via a TEM grid shadow mask. **b**, Raman I_{2D}/I_G of the transfer seen in (a) collected with 532 nm excitation (0.6 mW, 1 second exposure, 1 accumulation, $N = 42,251$). **c**, Raman spectra for all 24 graphene pixels collected with 532 nm excitation (0.3 mW, 60 second exposure, 1 accumulation). **d**, Zoom in view of 10 selected spectra illustrating the lack of a D peak. **e**, Plot of G-band versus 2D-band frequencies for all 24 graphene pixels.

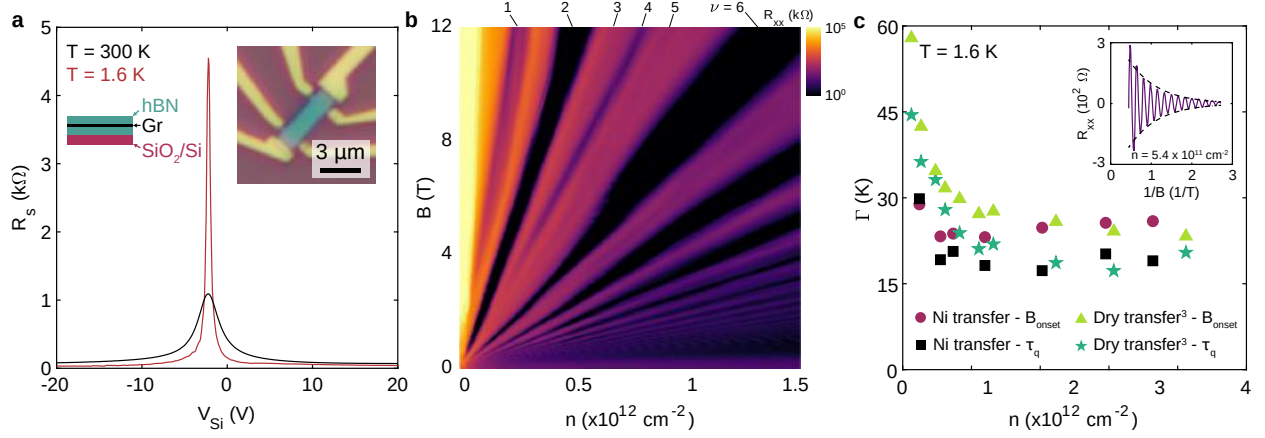


Figure S10: **Ni-transferred graphene device with $\text{Si}^{++}/\text{SiO}_2$ gating.** **a**, Room-temperature (300 K) and low-temperature (1.6 K) sheet resistance (R_s) as a function of back-gate voltage (V_{Si}). Inset of **(a)** is an optical image of the Hall bar device. **b**, Landau fan diagram of the longitudinal resistance, R_{xx} , as a function of density and magnetic field. **c**, Landau level broadening Γ , extracted from quantum lifetime τ_q and the onset of SdH oscillations vs. carrier density n for both $\text{Si}^{++}/\text{SiO}_2$ and graphite gating. Inset of **(c)** is Shubnikov-de Haas oscillation for the $\text{Si}^{++}/\text{SiO}_2$ gated device measured at carrier density $n = 5.4 \times 10^{11} \text{ cm}^{-2}$.

Zero-field transport measurements reveal low residual doping disorder with the charge neutrality point residing at -2 V at both room (300 K) and low (1.6 K) temperature (Fig. S10a). Figure S10b shows a high-field map of longitudinal resistivity (R_{xx}) as a function of density (n) and magnetic field (B) measured at 1.6 K. Prominent integer quantum Hall states (e.g. $\nu = 2, 6$) are resolvable below 1 T.

The quantum scattering time τ_q is derived from the Dingle analysis described in previous work [3]. The inset of figure S10c shows longitudinal resistance (R_{xx}) is plotted as a function of inverse magnetic field (B^{-1}) and fit with the Ando formula:

$$\Delta\rho_{xx}/\rho_0\gamma_{th} = 4\exp(-\pi/\omega_c\tau_q) \quad (1)$$

where $\gamma_{th} = (2\pi^2k_B T/\hbar\omega_c)/\sinh(2\pi^2k_B T/\hbar\omega_c)$ is the Dingle term, and τ_q is the quantum scattering time. The cyclotron frequency is $\omega_c = eB/m^*$, with effective mass given by $m^* = \hbar\sqrt{n\pi}/(V_F m_e)$.

Figure S10c shows the Landau level broadening Γ as a function of density for the Ni-

based transfer device and previous work on dry transferred graphene [3]. Γ is derived from τ_q by $\Gamma = \hbar/2\tau_q$. A second estimate of Γ is provided from the onset of SdH oscillations by $\Gamma = v_f \sqrt{2e\hbar B_{onset}} (\sqrt{|N|} - \sqrt{|N-1|})$ where the Fermi velocity in graphene is $v_f = 1 \times 10^6$ m/s and $N = \frac{nh}{4eB} - 0.5$.

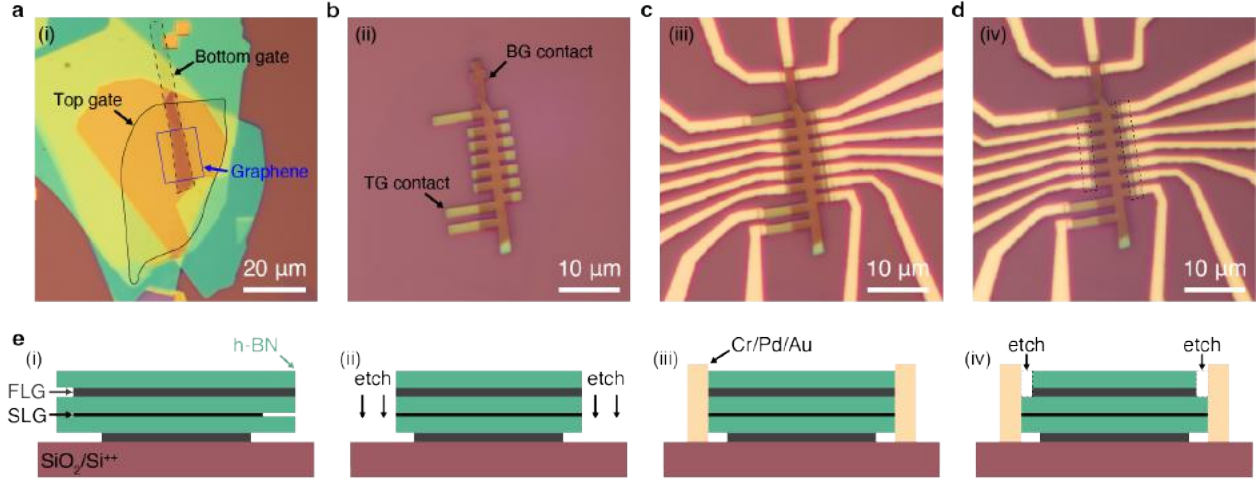


Figure S11: **Dual-graphite-gated monolayer graphene device fabrication.** **a**, Optical microscope image for the stack diagrammed in **a** outlining the positions of graphite and graphene layers. **b**, Device geometry and edge contacts were formed by etching in SF_6 and O_2 plasmas. **c**, Contacts were made to graphite and graphene by metal deposition and subsequent metal lift-off. **d**, A trench etch was made through to top hBN and graphite to completely isolate the graphene from both gates. **e**, Cross-sectional views of the fabrication steps (i-iv).

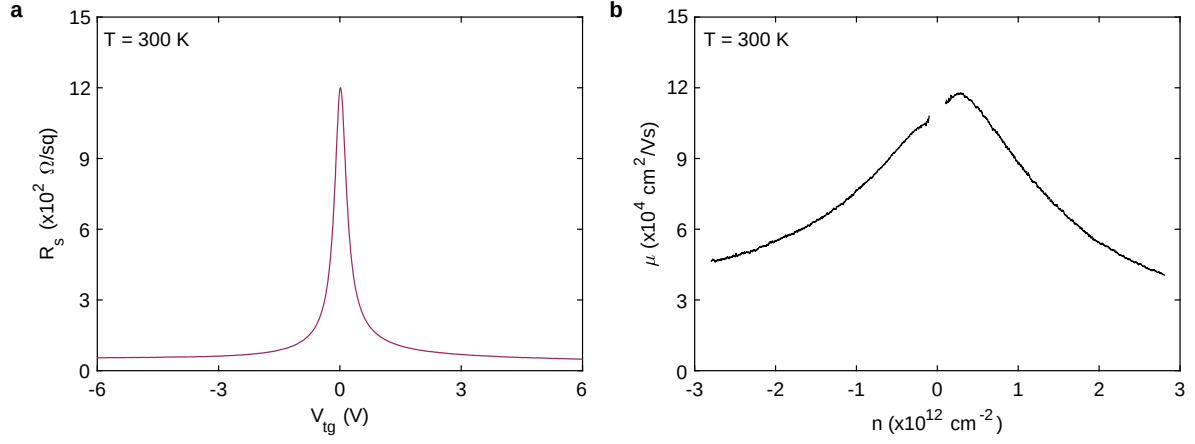


Figure S12: **Room temperature transport of the dual-graphite-gated transport device.** **a**, Room-temperature sheet resistance (R_s) as a function of top-gate voltage (V_{tg}). **b**, Room-temperature mobility (μ) as a function of density (n).

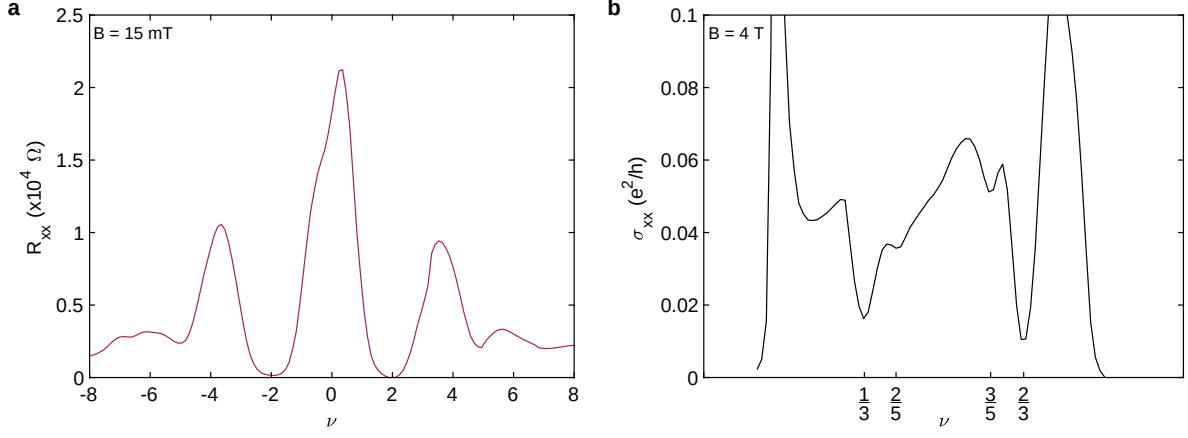


Figure S13: **Linecuts from data in Fig. 3.** **a**, Linecut of Fig. 3b at a constant field of 15 mT. We observe full quantization of the integer quantum hall states $\nu = \pm 2$. **b**, Linecut of Fig. 3c at a constant field of 4 T. We observe moderate quantization of the fractional quantum hall states $\nu = \frac{1}{3}, \frac{2}{3}$ with onset quantization of filling fractions $\nu = \frac{2}{5}, \frac{3}{5}$.

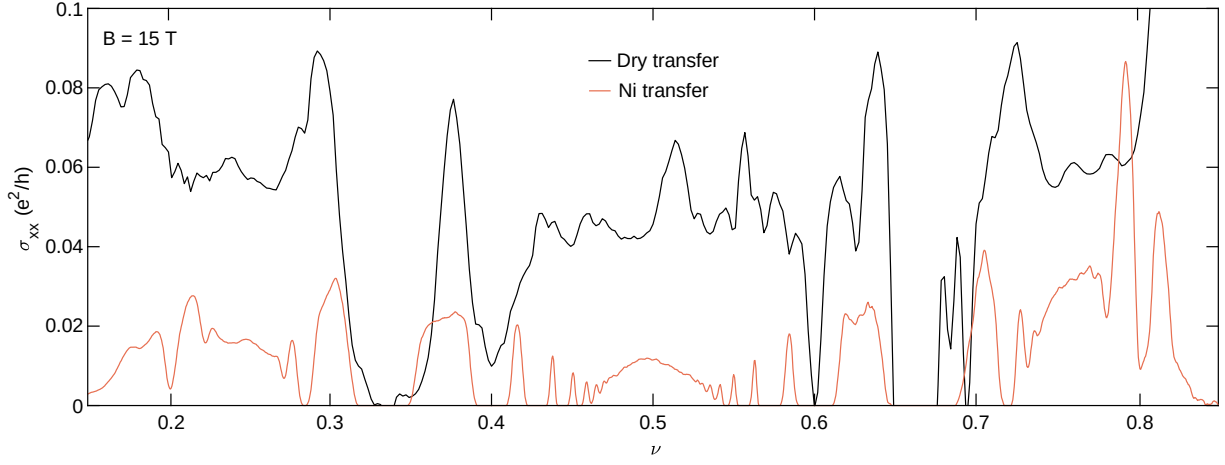


Figure S14: σ_{xx} versus ν of the $N = 0$ LL at $B = 15$ T for our previous dry transfer device [3] and Ni-based transfer with dual-graphite-gating.

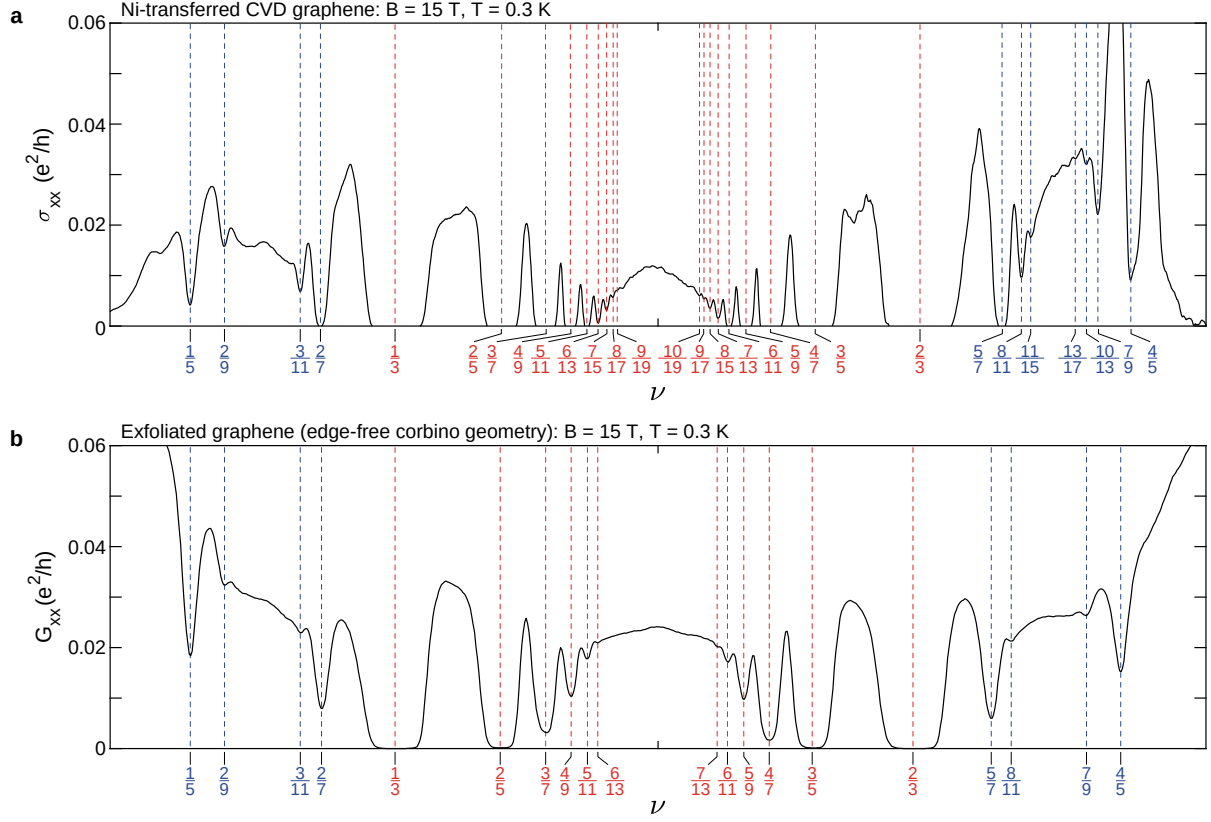
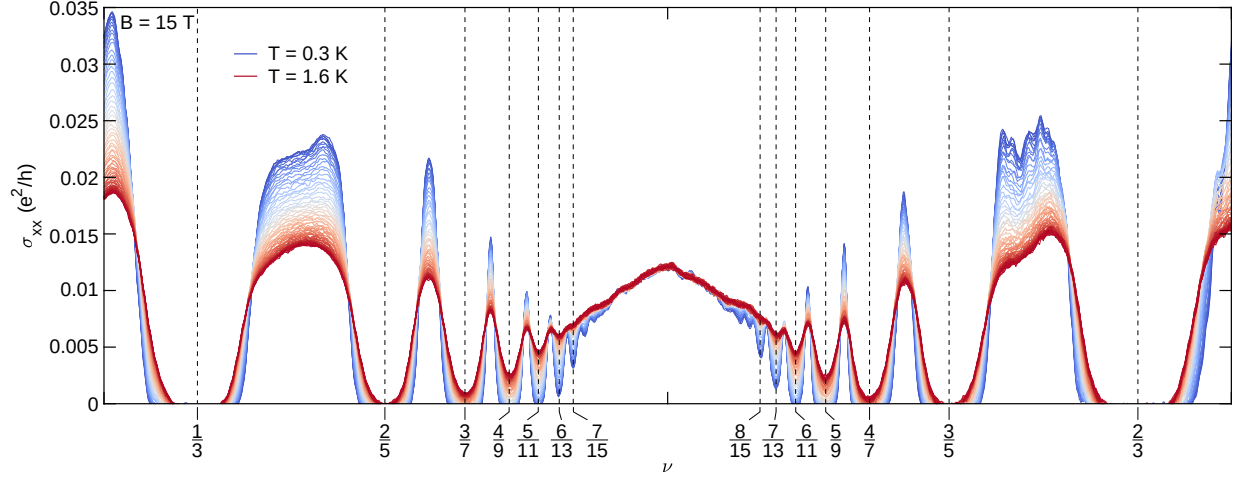


Figure S15: **a-b**, σ_{xx} and bulk conductance (G_{xx}) versus ν of the $N = 0$ LL at $B = 15$ T and $T = 0.3$ K for Ni-transferred CVD graphene with dual-graphite-gating and exfoliated graphene (edge-free corbino geometry) [4], respectively.



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