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Research Article

Interface-Engineered Proton-Gated Oxide Transistors with Multitimescale Synaptic Plasticity

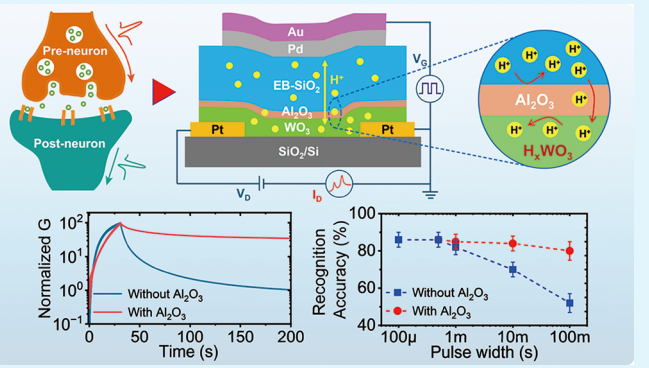
Rupam Mandal,* Kazuya Terabe, and Tohru Tsuruoka*

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ABSTRACT: Ion-gated transistors that mimic biological synapses are essential for energy-efficient neuromorphic hardware capable of adaptive learning and sensory processing. However, achieving both high-speed operation and stable memory in silicon-compatible platforms remains challenging due to the trade-off between ionic mobility and retention characteristics. In this work, we developed proton-gated synaptic transistors composed of an electron-beam (EB)-deposited SiO_2 electrolyte and a sputtered WO_3 channel. A low film density with the oxygen deficiency of EB-deposited SiO_2 enables gate-controlled proton intercalation and deintercalation, producing versatile synaptic plasticity of continuously modulating the WO_3 channel conductance. The devices exhibit a wide time response range (pulse widths from 100 ms to 50 μs) and a large dynamic range (>10^3) with a retention time of ∼18 s, successfully emulating short-term plasticity and nociceptor-like sensory behaviors such as threshold spiking, relaxation, and sensitization. They also achieve ∼90% image recognition accuracy and a low power consumption of ∼200 fJ for a single synaptic event. Furthermore, an introduction of a thin Al_2O_3 layer between the electrolyte and channel effectively suppresses proton back-diffusion, extending the retention time to ∼860 s. This also results in high recognition accuracy across a wide range of pulse widths, from subseconds to submilliseconds. By integrating two transistors with different retention times into a "one-transistor−one-synapse" architecture, we further demonstrated hardware-level temporal control of synaptic plasticity that enables event-driven learning, forgetting, and memory without altering input stimuli. These results indicate that all-oxide proton-gated transistors incorporating interface engineering provide a neuromorphic platform that enables highly flexible designs with excellent synaptic characteristics.



KEYWORDS: *ion-gated transistor, synaptic device, proton intercalation/deintercalation, metal oxides, interface engineering, event-driven learning/forgetting, neuromorphic computing*

1. INTRODUCTION

The rapid growth of artificial intelligence (AI) has exposed fundamental limitations of conventional von Neumann computing architectures, particularly for tasks requiring adaptive learning, real-time sensory processing, and energy-efficient parallelism. Neuromorphic hardware, inspired by the structure and dynamics of biological neural systems, offers a promising pathway to overcome these challenges by physically emulating synaptic plasticity at the device level.[1] The human brain can perform difficult tasks with ultralow power consumption (∼20 W) through synaptic plasticity (synaptic weight modulation) despite its massive complex network comprising 100 billion neurons connected by 100 trillion synapses.[2] Among various emerging devices, memristors have emerged as especially attractive candidates for implementing artificial synapses, owing to their analog conductance modulation, low power consumption, high-speed operation, and structural similarity with biological synapses.[3−5]

Extensive efforts on two-terminal memristors revealed their capability to emulate synaptic plasticity through voltage-driven ionic motion within a single active layer and have been widely employed in artificial neural network (ANN) simulations to evaluate neuromorphic task performance.[6−8] Despite their scalability, these devices suffer from read disturbance and nonideal weight updates due to coupled read/write operations.[9] Moreover, they draw a high write current (from μA to mA) due to conducting filament formation, resulting in higher power consumption, limited effective weight resolution, and low

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lifespan due to excessive power dissipation.[5,10−12] To address these bottlenecks, three-terminal ion-gated transistors have emerged, decoupling read and write operations via an electrolyte gate and a mixed-conductor channel.[13−15] Modulating channel conductance through electrochemical doping of mobile ions, these transistors enable nondestructive readout, linear synaptic weight update, and sub-μA operation, ensuring the high training stability and low power consumption required for large-scale neuromorphic systems.[15,16]

While tungsten trioxide (WO_3) is a premier channel material due to its expansive tunnels for ion intercalation,[15,17] achieving high-performance synaptic transistors depends strongly on the ion-conducting electrolyte. For instance, Li-ion gated transistors employ composite electrolytes like LiPON, $LiCoO_3$, Li_xSiO_2, and $Li_3PO_xSe_x$.[9,18−22] Meanwhile, the proton-gated WO_3 transistors mostly utilize ionic liquids or organic polymer electrolytes such as Nafion and chitosan.[23−25] Despite their good synaptic responses, challenges remain in their fabrication and integration due to limited compatibility with lithography processes and poor environmental stability. On the other hand, oxide electrolytes with oxygen vacancies or cations (like Cu^{2+}) provide better integration, but their low ionic mobility results in slow operating speed (from 100 to 10 ms) and nonlinear weight updates.[14,26−29] In this regard, proton-conducting oxide electrolytes emerge as a superior alternative, leveraging the high-speed kinetics of proton migration and robust solid-state reliability.[16,30,31] These devices achieved high-speed operation (from μs to ns) with low current levels (<μA), but protonation methods (like spillover) make the overall fabrication processes complicated. Furthermore, a fundamental trade-off persists between fast synaptic weight modulation and its long-term retention, dictated by proton migration (controlled by ionic conductivity and activation energy) and intercalation processes within devices.[20,32] Low activation energy facilitates fast proton migration (increases exponentially with reducing activation energy) but also leads to rapid back-diffusion (deintercalation) and volatile relaxation (poor retention).[33] On the contrary, high activation energy reduces proton mobility, resulting in a slow operating speed. Therefore, interface engineering between the electrolyte and channel is important to create an optimal potential barrier that enables fast operating speed and suppresses spontaneous deintercalation in proton-gated transistors.

Herein, we develop proton-gated synaptic transistors with a WO_3 channel and an electron-beam (EB)-deposited SiO_2 electrolyte, which have full complementary metal-oxide-semiconductor (CMOS) compatibility, excellent chemical stability, and precise thickness controllability. The inherent hydrogen species in EB-deposited SiO_2 enable gate voltage-driven proton migration while maintaining excellent insulation to source and drain electrodes, allowing low power operation with suppressed channel current. As a result, the device exhibits short-term plasticity with high operating speed (down to 50 μs) with a large dynamic range ($>10^3$) and emulates nociceptor-like sensory behaviors. Owing to the high-speed operation, the devices operate at a low energy consumption (~200 fJ per synaptic event). The short retention characteristic can be improved by inserting a thin Al_2O_3 layer between the electrolyte and channel, which acts as a proton diffusion barrier. It is also found that both transistors achieve high online image recognition accuracy (~90%) in ANN simulations. Furthermore, we integrate transistors with different retention times into a "one-transistor−one-synapse (1T−1S)" architecture and demonstrate hardware-level temporal gating of synaptic plasticity, enabling selective learning, forgetting, and signal filtering without modifying the input stimuli. These results indicate that the interfacial optimization between the oxide electrolyte and channel can realize proton-gated transistors with excellent synaptic plasticity with varied retention characteristics, while maintaining high CMOS compatibility.

2. RESULTS AND DISCUSSION

Figure 1a illustrates the basic structure of the fabricated transistors (under biased conditions) composed of a SiO_2 electrolyte and a WO_3 channel. The SiO_2 electrolyte is EB-deposited, while the WO_3 channel is deposited using radio-frequency (RF) sputtering. Pt/Ti is used as the source and drain electrodes, whereas Au/Pd is used as the gate electrode. Figure 1b shows an optical microscope image of the entire transistor device. An image of the channel region after forming the source/drain electrodes is shown in Figure S1a (Supporting Information). The channel length and width are 2 and 25 μm, respectively. We also fabricated another transistor by inserting a thin Al_2O_3 layer between the SiO_2 electrolyte and WO_3 channel, which is deposited by RF sputtering. Figure 1c displays a cross-sectional transmission electron microscopy (TEM) image of the pristine $SiO_2/Al_2O_3/WO_3$ transistor. The image confirms a uniform film deposition for all layers with thicknesses of ~36, ~21, and ~3 nm for the SiO_2, WO_3, and Al_2O_3 layers, respectively. The interfaces are sharply identified, excluding any possible interlayer/interfacial mixing during the deposition of successive layers, which are also confirmed by energy-dispersive X-ray spectroscopy (EDS) mapping, as shown in Figure S1b (Supporting Information). X-ray diffraction (XRD) measurements revealed that both the SiO_2 electrolyte and WO_3 channel are amorphous in nature, as depicted in Figure S2 (Supporting Information).

The output curve (drain current (I_D)−drain bias (V_D)) of a SiO_2/WO_3 transistor is shown in Figure S3a (Supporting Information). The pristine device exhibits a low current of less than 1 nA, as indicated by the black curve. If the gate bias (V_G) is repeatedly swept within a range of ±2 V from this state, then the I_D gradually increases and eventually reaches saturation. After that, the output curve shows a linear characteristic, which confirms an ohmic conduction between the source and drain electrodes, as indicated by the red curve. Figure 1d plots the transfer curves of the SiO_2/WO_3 transistor for different V_G sweep ranges. The results show a large counterclockwise hysteresis loop, indicating the ionic memory (distinct from electronic charge-based memory) characteristics.[13] The I_D increases under positive V_G sweep, whereas it reduces under negative sweep. As the maximum sweep voltage increases, the I_D increases by more than two orders of magnitude, suggesting a significantly enhanced hysteresis loop. It was found that the I_D also increases with a decreased V_G sweep rate (Figure 1e) and the hysteresis loop becomes larger with increasing sweep cycles (Figure 1f). When a thin Al_2O_3 layer is inserted between the SiO_2 electrolyte and WO_3 channel, the initialization conditions are slightly different. The pristine device exhibits a low current of less than 1 nA in the output curve, similar to the SiO_2/WO_3 transistor (black curve in Figure S3b). No increase in I_D is observed even when V_G is swept to ±3 V, but if V_G is swept to ±4 V or higher, then I_D increases distinctly (red curve in Figure S3c). After this V_G sweep, the output curve exhibits ohmic behavior (red curve

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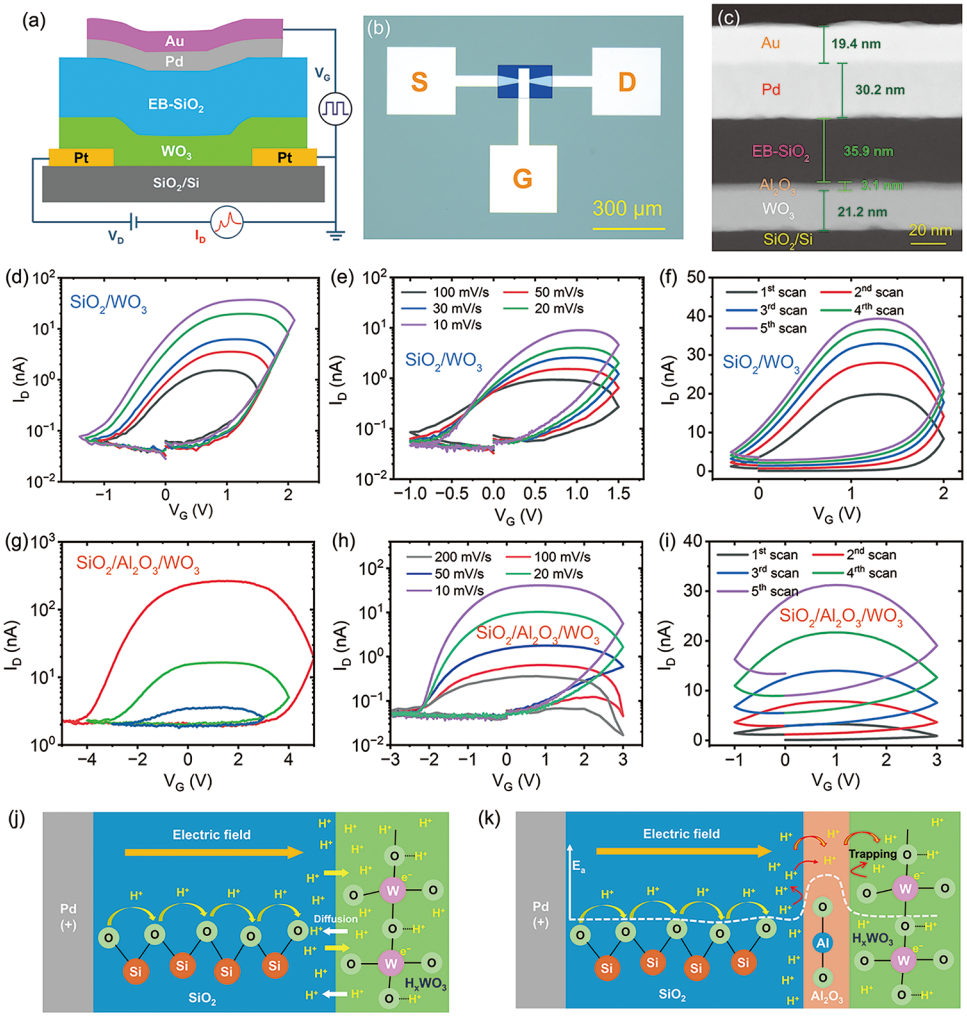


Figure 1. (a) Schematic illustration of a SiO_2/WO_3 transistor. (b) Optical microscopic image of the fabricated device. (c) Cross-sectional TEM image of the channel of a $SiO_2/Al_2O_3/WO_3$ transistor. Transfer curves of a SiO_2/WO_3 transistor measured under (d) different V_G sweeps, (e) various V_G sweep rates, and (f) increased sweep cycles. (g–i) Similar transfer curves measured for a $SiO_2/Al_2O_3/WO_3$ transistor with a 3 nm-thick Al_2O_3 layer. Schematics of gate bias-induced proton transport in transistors (j) without and (k) with an Al_2O_3 layer. The dashed line in (k) represents the activation energy (E_a) for proton migration.

in Figure S3b). Figure 1g shows the transfer curves of a $SiO_2/Al_2O_3/WO_3$ transistor with a 3 nm-thick Al_2O_3 layer, measured over different voltage sweep ranges. The curves display wider and more symmetrical hysteresis loops because a higher negative bias is required to reset I_D.

Figure 1h displays the transfer curves of the $SiO_2/Al_2O_3/WO_3$ transistor, measured under different V_G sweep rates. The slower sweep rate produces a larger hysteresis loop, similar to the SiO_2/WO_3 transistor (Figure 1e). Furthermore, the hysteresis loop clearly shifts upward as the number of sweep cycles increases, as shown in Figure 1i. We see that the current modulation is highly consistent and symmetrical during both positive and negative sweeps, unlike the SiO_2/WO_3 transistor (Figure 1f). These results indicate that the insertion of a thin Al_2O_3 layer between the electrolyte and channel improves the memory behavior. Good device-to-device reproducibility is also obtained for both transistors with and without an Al_2O_3 layer, as shown in Figures S4 (Supporting Information). Note that the gate leakage current (I_G) is very small <2 nA under the V_G range used, indicating good insulating properties of the EB-deposited SiO_2 film, as shown in Figure S5 (Supporting Information).

The nonlinear and large current change observed in oxide channel-based transistors is generally attributed to migration of mobile ions under high electric fields.[13,34] To elucidate the operating mechanism of our transistors, the physical properties of the SiO_2 electrolyte and WO_3 channel were examined in detail. X-ray reflectivity (XRR) measurements reveal that the film densities of the EB-deposited SiO_2 and sputtered WO_3 are estimated to be 2.14 and 6.61 g/cm^3, respectively, which are lower than the density of the bulk SiO_2 (2.65 g/cm^3) and WO_3 (7.16 g/cm^3), as shown in Figure S6 (Supporting Information). These lower densities originate from the amorphous nature of both deposited films, as evidenced by XRD. The chemical compositions of both films were further investigated using hard X-ray photoelectron spectroscopy (HAXPES). The survey spectra and core-level spectra of each element are shown in Figure S7 (Supporting Information). The elemental compositions are estimated to be $SiO_{1.75}$ and $WO_{2.82}$, which are ~20% and ~8% oxygen-deficient compared

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to the stoichiometric SiO_2 and WO_3, respectively. These oxygen deficiencies are consistent with the lower film densities evaluated from the XRR analyses. Detailed analyses of HAXPES data are described in the Supporting Information.

The low film density can promote protonic migration between the SiO_2 electrolyte and WO_3 channel under V_G bias, resulting in I_D modulation. In addition, the presence of oxygen vacancy defects in EB-deposited SiO_2 further reduces the activation energy for proton migration.[33] To examine the presence of protons in the SiO_2 electrolyte, Fourier-transform infrared spectroscopy (FTIR) was used to investigate the chemical bonding state of an EB-deposited SiO_2 films. For this measurement, a 100 nm-thick SiO_2 film was EB-deposited on a Pt-coated Si substrate. The FTIR spectrum shows small peaks at ~940 and ~1630 cm^{-1} and a broad absorption band ranging from 2400 to 3700 cm^{-1}, as shown in Figure S8 (Supporting Information). The peaks correspond to the stretching and bending modes of Si−H bonds, respectively, while the broad band is attributed to the OH stretching vibration of hydrogen-bonded silanol groups (Si−OH).[35] This suggests that the EB-SiO_2 film contains a large number of protons even in the as-deposited state. From the integrated absorbance of the Si−OH band, the proton concentration was estimated to be $\sim 6.5 \times 10^{21}$ cm^{-3}. The detailed estimation method is described in the Supporting Information. The ionic conductivity of an EB-deposited SiO_2 film was then evaluated by electrochemical impedance spectroscopy (EIS). For this measurement, a two-terminal Pd/SiO_2/Pt device was fabricated. The conductivity was estimated to be ~10^{-7} S/cm from the fitting of an equivalent circuit to the EIS curve, as shown in Figure S9 (Supporting Information), which is higher than thermally grown SiO_2 (<10^{-9} S/cm).[36] This higher ionic conductivity of EB-deposited SiO_2 enables migration of protons under electrical bias. It was also found that the absolute capacitance varies from 3.7 pF at 1 MHz to 0.27 nF at 1 Hz. Considering the device area (50×50 μm^2), the specific capacitance is calculated to be ~10.8 $\mu F/cm^2$ at 1 Hz, which is ~500 times higher than that of thermally grown SiO_2 films (~20 nF/cm^2).[37] This significantly large capacitance can be attributed to the formation of an electric double layer (EDL) at the SiO_2/metal interfaces under small ac biases.[38]

The proton transport mechanisms in our transistors without and with an Al_2O_3 layer are schematically illustrated in Figures 1j and 1k, respectively. Generally, hydrogen resides inside SiO_2 by forming −OH groups, which become the origin of mobile protons (H^+). When an external electrical field is applied across SiO_2, protons dissociate from their localized oxygen site and hop to adjacent oxygen sites along the electric field by overcoming a small diffusion barrier (~0.4 eV).[39] Proton migration in SiO_2 generally takes place through cross-ring and nearest neighbor hopping mechanisms, and the presence of vacancy defects makes it easier.[40] When positive V_G is applied, protons in the SiO_2 electrolyte migrate toward the WO_3 channel and intercalate into the WO_3 lattice, which increases the I_D. Once the protons reach the WO_3 channel, they form a mixed ionic−electronic conducting H_xWO_3 phase, according to the electrochemical reaction given by[23]

$$xH^+ + xe^- + WO_3 = H_xWO_3 \quad (1)$$

where e^- is the number of electrons supplied through the outer circuit and x indicates the degree of intercalation. WO_3 can host a large number of protons (up to x ~0.5), corresponding to proton density as high as ~10^{21} cm^{-3}.[41] The intercalated protons can reside in the WO_3 matrix through bond formation with oxygen ions (forming OHO defects) like doping elements due to their small size. However, the intercalated protons spontaneously diffuse back to the SiO_2 electrolyte due to concentration gradients and low diffusion barrier, which reduces the x content in H_xWO_3, leading to a decrease in I_D over time after removal of V_G.

In contrast, the insertion of an Al_2O_3 layer between the SiO_2 electrolyte and WO_3 channel alters the dynamics of proton migration due to its ion blocking characteristics. The highly insulating Al_2O_3 (resistivity ~10^{12} Ω cm) layer increases the resistance between the gate and source/drain, and its ionic barrier (~1−1.5 eV; represented by the activation energy (E_a) curve in Figure 1k) retards the migration of protons toward the WO_3 channel.[42] As a result, the channel current reduces significantly, and a higher V_G (>4 V) is required to cause the change in I_D. This allows protons to jump across the barrier and increases the initial channel conductance. After that, the device exhibits a more symmetric hysteresis curve under V_G sweeps (with a strong dependence on the bias range and scan rate), as shown in Figure 1g,h. Besides lowering the maximum conductance level, the high proton barrier simultaneously suppresses spontaneous proton back-diffusion, confining protons within the WO_3 channel to promote the long-term stability of the H_xWO_3 phase, thereby significantly enhancing the retention characteristic of drain current. This is evident from prominent and symmetric analog current modulation under consecutive V_G sweeps (Figure 1i).

To verify the proton conduction mechanism, we investigated the effect of differences in the surrounding environment and film deposition methods on transistor characteristics. First, the transfer curves were measured in vacuum after confirming the device performance in the atmosphere. Under vacuum conditions, the I_D decreased to less than 1 nA, and no hysteresis loop was observed even when V_G was swept over a range of ±10 V, as shown in Figure S11a (Supporting Information). This behavior was found to be reversible; when the device was returned to atmosphere conditions, the transfer curve reverted to its initial state. This is because, under vacuum conditions, protons desorb from the SiO_2 electrolyte (and the WO_3 channel) and therefore cannot contribute to changes in I_D. It should be noted that, as shown in Figure S11b (Supporting Information), the transfer curves remain relatively stable over a wide range of humidity (20−80% RH). Next, we investigated the transfer curves of SiO_2/WO_3 transistors with a sputtered SiO_2 instead of the EB-deposited SiO_2 under atmospheric conditions. As shown in Figure S12 (Supporting Information), this device exhibits no memory behavior even when V_G is swept up to ±10 V. This behavior is consistent with the FTIR results (Figure S8), in which no peaks associated with Si−H and Si−OH bonds were observed in the sputtered SiO_2 film. These results support the conclusion that SiO_2 deposited by EB evaporation can function as a proton conductor (electrolyte) that facilitates the proton intercalation into and deintercalation from the WO_3 channel.

The influence of EDL must also be taken into account as a cause of the change in I_D under V_G application. To investigate this, capacitance−frequency measurements were performed on two-terminal Au/Pd/SiO_2/Pt and Au/Pd/SiO_2/WO_3/Pt devices under different bias conditions, as shown in

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Figure S10 (Supporting Information). The Au/Pd/SiO_2/Pt device exhibits flat capacitance characteristics in the low-frequency range, suggesting that an EDL is formed at the Pd/SiO_2 and SiO_2/Pt interfaces. On the other hand, no capacitance plateau was observed in the Au/Pd/SiO_2/WO_3/Pt device; instead, a sharp increase in capacitance was observed in the low-frequency range. This capacitance increase can be attributed to an increase in the electrical conductivity of the WO_3 layer caused by proton intercalation from the SiO_2 layer. Based on these results, we conclude that although EBL contributes to some extent, proton intercalation and deintercalation still play the primary role in the observed changes in I_D.

Analog conductance modulation is further employed to emulate key synaptic functionalities of the human brain toward neuromorphic computing applications. Figure 2a sketches the structure and signal transmission mechanism at a synapse connection between two neurons in parallel to the present devices under electrical spikes. In the human brain, signal transmission between neurons occurs through synaptic weight modulation, which is known as synaptic plasticity.[2] In our transistors, channel conductance modulation mimics synaptic plasticity, governed by gate bias-controlled proton intercalation into and deintercalation from the WO_3 channel.[17] In this configuration, the gate electrode acts as the presynaptic terminal while the drain/source electrodes act as the postsynaptic terminal. To demonstrate synaptic properties, channel conductance (G) is used in pulsed I−V measurements. Figure 2b shows the G of the SiO_2/WO_3 transistor under applications of consecutive V_G pulses to the gate. The G increases from ∼0.02 to ∼80 μS under 100 positive V_G pulses of +3 V, giving rise to a very high dynamic range of ∼4 × 10^3. Subsequently, the G reduces rapidly to its initial level under 100 negative V_G pulses of −1 V. Here, the pulse width and interval time were fixed at 100 ms and the I_D is measured with V_D = 0.1 V. The conductance increase and decrease mimic the long-term potentiation (LTP) and depression (LTD) behaviors of biological synapses, respectively. The G gradually increases in LTP but sharply drops in LTD due to rapid back-diffusion of protons from the channel to the electrolyte, as discussed earlier. The dynamic range strongly depends on the amplitude of V_G pulses, as shown in Figure 2c, and the LTP/LTD behavior exhibits excellent stability and high reproducibility for at least 18 cycles, as shown in Figure 2d.

In contrast, the SiO_2/Al_2O_3/WO_3 transistor exhibits slower conductance modulations under V_G pulse applications, as shown in Figure 2e. The G increases from 0.03 to 2.85 μS (dynamic range ∼95) under 100 positive V_G pulses of +3.5 V. The subsequent negative V_G pulses of −1.5 V reduce the G gradually, but it does not return to the initial level even after 100 pulses. This indicates that the Al_2O_3 layer effectively inhibits the back-diffusion of protons from the WO_3 channel to the SiO_2 electrolyte, thereby improving the retention property. The significantly lower conductance level suggests that the Al_2O_3 layer limits the number of protons contributing to the conductance variations. The device also exhibits tunable

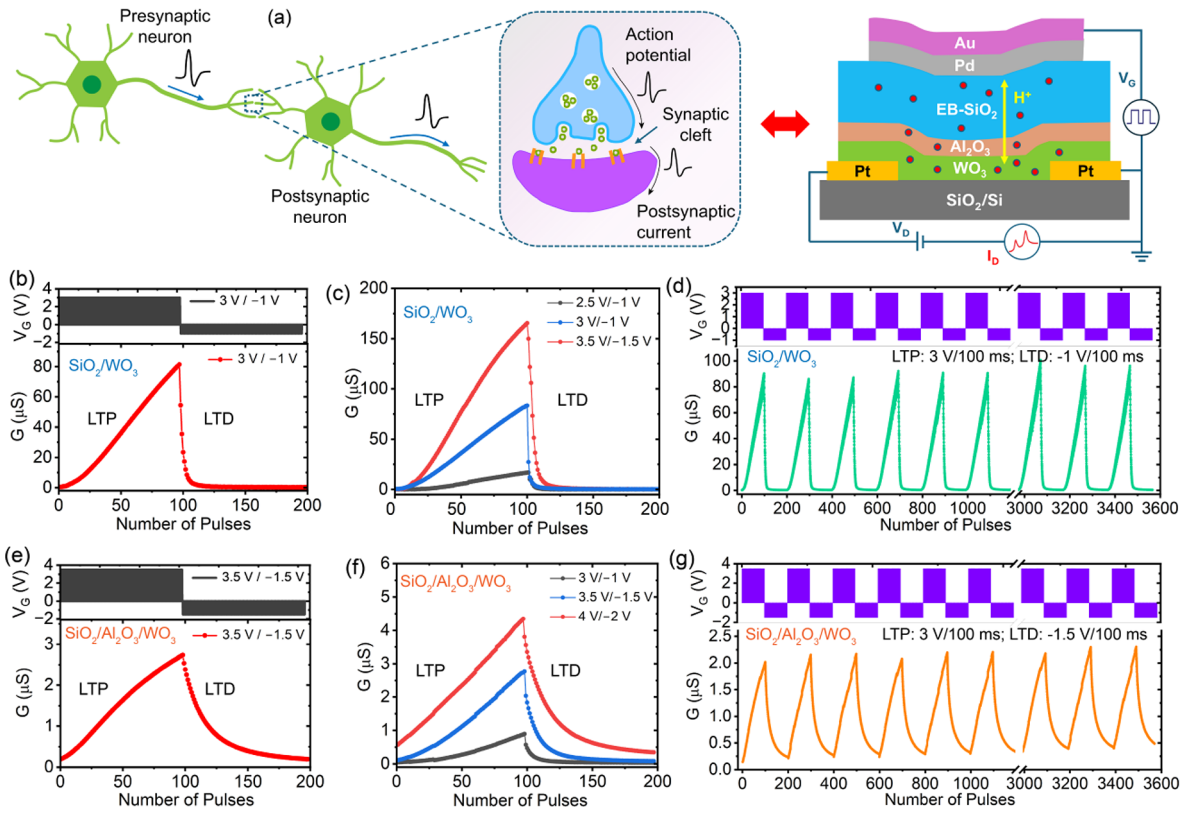


Figure 2. Channel conductance (G) modulation of SiO_2/WO_3 transistors under V_G pulse applications. (a) Schematics of a biological synapse and structural similarities to our transistor. (b) LTP/LTD of a SiO_2/WO_3 transistor under application of consecutive 100 positive and 100 negative V_G pulses. (c) LTP/LTD under application of V_G pulses with different amplitudes. (d) LTP/LTD characteristics for 18 successive cycles. (e) LTP/LTD of a SiO_2/Al_2O_3/WO_3 transistor under application of consecutive 100 positive and 100 negative V_G pulses. (f) LTP/LTD under application of V_G pulses with different amplitudes. (g) LTP/LTD characteristics for 18 successive cycles.

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conductance changes under different pulse amplitudes, as shown in Figure 2f, similar to the SiO_2/WO_3 transistor. Figure 2g further depicts stable conductance modulations confirmed by reproducible LTP/LTD cycles with improved symmetricity. The temperature dependence of the LTP/LTD characteristics was also examined up to 100 °C, as shown in Figure S13a (Supporting Information). It can be determined by two competing thermal mechanisms, resulting in nonmonotonic changes. At relatively low temperatures up to 40 °C, an increase in proton mobility within EB-SiO_2 facilitates proton intercalation into the WO_3 channel, giving rise to increased changes in channel conductance. On the other hand, at high temperatures above 60 °C, thermally activated proton desorption from SiO_2 takes place, reducing the number of protons in the channel. As a result, the magnitude of conductance change decreases at elevated temperatures.

To determine the barrier effect of the Al_2O_3 layer, the LTP/LTD characteristics were investigated for $SiO_2/Al_2O_3/WO_3$ transistors with different Al_2O_3 thicknesses. Figures 3a and 3b depict the LTP/LTD plots measured for devices with 1.5 and 7 nm-thick Al_2O_3 layers, respectively, under application of 100 positive (+3.5 V) and subsequent 100 negative (−1.5 V) V_G pulses. When the Al_2O_3 layer is thin, the change in LTP is large, but the G value of LTD decays rapidly. On the other hand, when the Al_2O_3 layer is thick, the G decays rapidly only at the beginning but then decreases gradually in LTD. This suggests that a thinner (1.5 nm) Al_2O_3 layer provides a weak barrier to protons, whereas a thicker (7 nm) layer not only strengthens the barrier effect but also slows down the back-diffusion from the WO_3 channel to the Al_2O_3 electrolyte. Figure 3c plots the dynamic range of G variation and V_G required to initialize transistors (maximum sweep voltage) as a function of Al_2O_3 thickness. The maximum sweep voltage increases with increasing Al_2O_3 thickness. The dynamic range becomes smaller for devices with thicker Al_2O_3, as the maximum conductance value decreases even though higher V_G pulses are applied. This is because the thick Al_2O_3 layer inhibits not only proton back-diffusion but also intercalation into the WO_3 channel.

Figures 3d and 3e show LTP and the subsequent conductance decay of the SiO_2/WO_3 transistor and $SiO_2/Al_2O_3/WO_3$ transistor with a 3 nm-thick Al_2O_3 layer, respectively, measured under 100 positive V_G pulses of +3.5 V. In SiO_2/WO_3 transistors, the G decays rapidly over time and drops to one-tenth of its maximum value in ∼18 s, which is defined as the retention time. The conductance decay can be fitted using an exponential double decay function, and the two decay constants of 2.7 s (τ_1) and 18.4 s (τ_2) are obtained. In contrast, in the $SiO_2/Al_2O_3/WO_3$ transistor, the decay of G is small and decreases to only one-third after 170 s. The decay constants are estimated to be 6.5 and 47 s, indicating a significant improvement in retention characteristics. For a comparison, Figure 3f plots the decay curves up to 1000 s for transistors with different Al_2O_3 layer thicknesses, where G is normalized to its maximum value at the last V_G pulse and the origin of the retention time is set just after the last pulse. We see that the insertion of the Al_2O_3 layer plays a crucial role in improving the long-term memory retention. The retention times for devices with 1.5, 3, and 7 nm-thick Al_2O_3 layers are estimated to be ∼160, ∼620, and ∼860 s, respectively. Considering the findings from transistors with different Al_2O_3 thicknesses, we conclude that 3 nm-thick Al_2O_3 is the optimal barrier layer, exhibiting well-balanced and improved synaptic characteristics. Furthermore, the retention property was measured at elevated temperatures up to 100 °C, as shown in Figure S13b (Supporting Information). The results indicate a comparable decay rate across all examined temperatures without any abrupt degradation, showing the robust thermal stability and reliability of $SiO_2/Al_2O_3/WO_3$ transistors.

Besides analog conductance modulation and state retention, the operating speed of synaptic devices is another crucial factor as far as their application in future data-intensive neuromorphic tasks is concerned. Our synaptic transistors exhibit G modulation on a wide timescale ranging from seconds to microseconds. Figure 4a–c shows repeated LTP/LTD characteristics

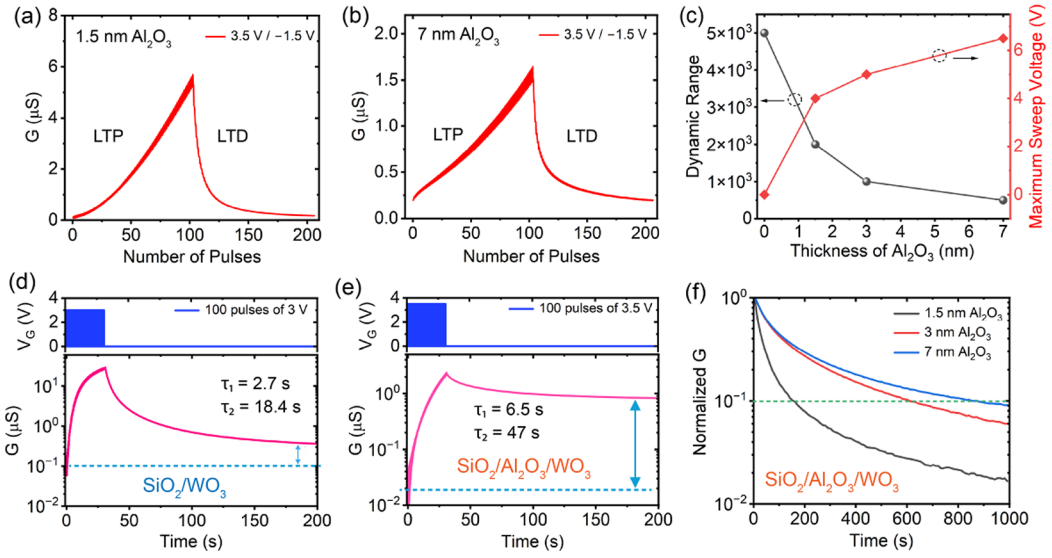


Figure 3. Impacts of Al_2O_3 layer thickness on the synaptic plasticity. LTP/LTD characteristics of transistors with Al_2O_3 layer thicknesses of (a) 1.5 nm and (b) 7 nm. (c) Dynamic range of G modulations and maximum sweep voltage required to initialize transistors plotted as a function of Al_2O_3 thickness. Conductance decay curves after application of 100 positive V_G pulses, measured for transistors (d) without an Al_2O_3 layer and (e) with a 3 nm-thick Al_2O_3 layer. (f) Normalized conductance decay curves plotted up to 1000 s for transistors with different Al_2O_3 thicknesses.

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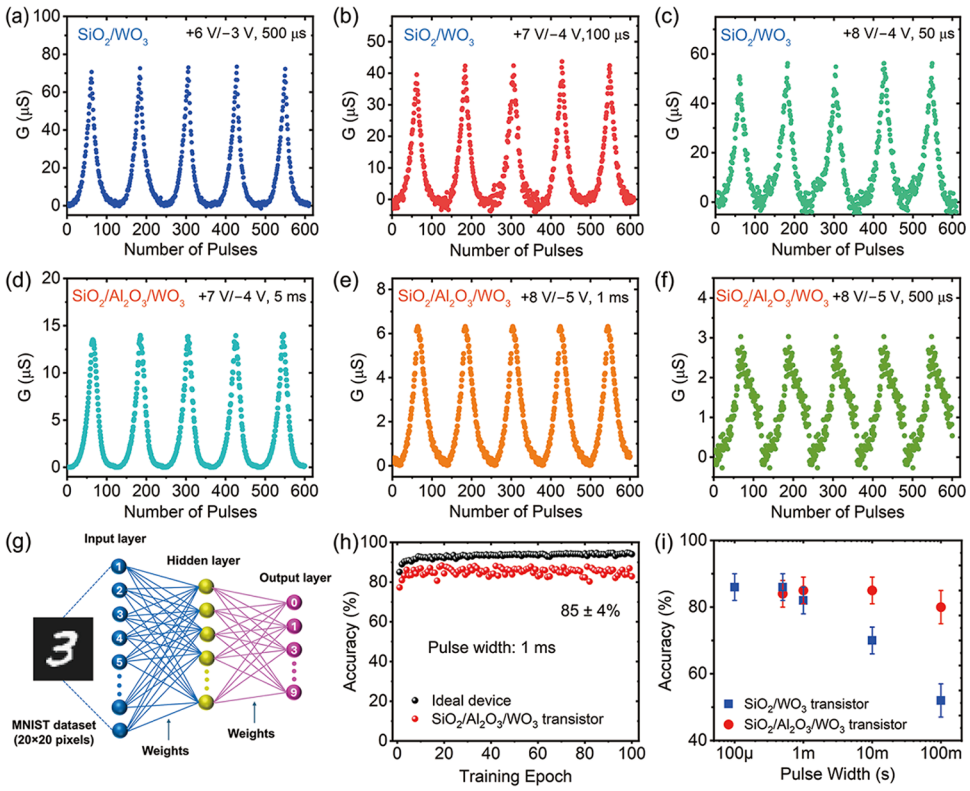


Figure 4. LTP/LTD characteristics under applications of different pulse widths and ANN simulations. Conductance modulations of SiO_2/WO_3 transistors with (a) 500 μs, (b) 100 μs, and (c) 50 μs pulse widths. Conductance modulations of $SiO_2/Al_2O_3/WO_3$ transistors with (d) 5 ms, (e) 1 ms, and (f) 500 μs pulse widths. (g) Schematic presentation of an ANN model used for image recognition of MNIST handwritten digits. (h) Image recognition accuracy plotted as a function of training epoch for $SiO_2/Al_2O_3/WO_3$ transistors. (i) Image recognition accuracy plotted as a function of pulse width for both transistors.

measured for the SiO_2/WO_3 transistor under applications of positive and negative V_G pulses with different widths from 500 to 50 μs. The interval time was set to the same as the pulse width. The linearity and symmetry in G modulation are significantly improved on timescales below milliseconds because the effect of proton back-diffusion becomes smaller. With decreasing pulse width, higher pulse amplitudes are required to achieve linear G modulations. Although LTP/LTD characteristics can be observed even with pulse widths of less than 50 μs, an amplitude of 9 V or higher is required, and the device starts getting damaged due to dielectric breakdown of the SiO_2 electrolyte.[43] The observed time responses on the order of tens of microseconds are attributed to fast migration of protons through a low-density SiO_2 electrolyte, which is unlikely in sputtered SiO_2 layers. Most previous reports on oxide-based synaptic transistors have demonstrated slow operating speeds on the order of milliseconds, highlighting the potential of our transistor for high-speed neuromorphic applications.[14,44] Another important point is that the diffusivity of protons within low-density oxide structures is significantly higher than that of the electromigration of heavier species such as oxygen or metal/alkali ions.[45] Note that the operating speed of three-terminal ionic devices is generally lower than that of two-terminal configurations (~ns) because the coupling between ions and electrons is inherently sequential in nature.[15,46] However, we believe that the operating speed can be further improved by reducing the channel length and electrolyte thickness to shorten the travel distance, as demonstrated by Onen et al.[30]

When the thickness of the SiO_2 electrolyte is increased to 60 nm in SiO_2/WO_3 transistors, the device exhibits good G modulation down to 1 ms pulses of +8 V, but it becomes inconsistent below 500 μs pulses, as presented in Figure S14 (Supporting Information). This result indicates a profound impact of the SiO_2 electrolyte thickness on the operating speed. For thicker SiO_2 electrolytes, protons need to migrate a larger distance to reach the WO_3 channel, which takes a longer time. However, if the thickness is reduced to less than 20 nm, then the gate leakage current increases, leading to a decline in the device's stability and performance. On the other hand, $SiO_2/Al_2O_3/WO_3$ transistors exhibit reproducible LTP/LTD behavior even at short pulse widths of down to 1 ms (Figure 4d,e), maintaining linearity and symmetry throughout the entire cycle. Notably, in these devices, conductance modulation is maintained even under 500 μs pulses (Figure 4f), with only slight fluctuations observed in the discrete conductance levels. This excellent performance confirms that the Al_2O_3 layer serves as an effective interfacial barrier that optimally balances the operational timescales and effectively suppresses rapid proton relaxation, thereby ensuring long-term retention of synaptic weights.

In addition to the operating speed, energy consumption is also the crucial parameter of artificial synaptic devices in neuromorphic computing applications. In synaptic transistors, the energy consumption for a single weight updating event is estimated ($=V_D \times \Delta I_D \times$ pulse width), by considering the drain voltage and increment/decrement (ΔI_D) in I_D (per V_G pulse).[47,48] From the I_D waveforms under consecutive V_G

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pulses, the values of ΔI_D were calculated, as shown in Figure S15 (Supporting Information). The energy consumption per synaptic event is estimated to be ~200 fJ under 50 μs pulses for SiO_2/WO_3 transistors and ~500 fJ under 1 ms pulses for $SiO_2/Al_2O_3/WO_3$ transistors. These values are quite impressive compared to the previously reported oxide-based devices, as summarized in Table S1 (Supporting Information). Although the energy consumption of our transistors is one or two orders of magnitude higher than that of synaptic devices based on two-dimensional materials or organic semiconductors,[48,49] oxide-based devices offer significant advantages for integration and commercialization due to their high compatibility with the current CMOS fabrication processes. We also believe that the energy consumption can be reduced by manifold either by achieving faster response (<50 μs) or by reducing the current change under successive pulses, which remains as a matter of future investigation. To assess the potential advantages of our transistors, a comparative performance table with previously reported devices is provided in Table S1.

Using the experimental LTP/LTD data obtained for both transistors, we carried out ANN simulations for image recognition of handwritten digits sourced from the Modified National Institute of Standards and Technology (MNIST) data set. From the conductance change normalized to the conductance and the number of pulses, the nonlinearity factors of LTP and LTD are estimated to be 0.72 and −4.25 for SiO_2/WO_3 transistors and 0.34 and −3.2 for $SiO_2/Al_2O_3/WO_3$ transistors, as shown in Figure S16 (Supporting Information).[50] The extracted nonlinearity factors and measured conductance values are subsequently incorporated into the ANN simulation framework to perform training and inference, enabling quantitative evaluation of image recognition task performance. Figure 4g schematically illustrates a fully connected ANN based on a two-layer perceptron model, consisting of 400 neurons in the input layer, 100 in the hidden layer, and 10 in the output layer. MNIST images of 20 × 20 pixels were fed as inputs, and digit classification (0−9) was performed using the NeuroSim+ platform.[50] Figure 4h plots the image recognition accuracy as a function of training epoch, using LTP/LTD data of $SiO_2/Al_2O_3/WO_3$ transistors, obtained with 1 ms V_G pulses. The result for SiO_2/WO_3 transistors with 100 μs pulses is shown in Figure S17 (Supporting Information). Both devices can achieve a high recognition accuracy of ~90% within only five training epochs, which is significantly superior to most previously reported synaptic devices, where comparable accuracy (>80%) typically requires 20−25 training epochs. Figure 4i plots the recognition accuracy as a function of pulse width for the two transistors. The SiO_2/WO_3 transistor exhibits high recognition accuracy (>85%) for short pulses of 1 ms or less, but this accuracy gradually decreases as the pulse width increases, falling below 50% at 100 ms. This is due to the nonlinearity of LTD, as observed in Figure 2b. In contrast, the $SiO_2/Al_2O_3/WO_3$ transistor maintains a high recognition accuracy of ~85% across a wide range of pulse widths from 500 μs to 100 ms. This demonstrates that the insertion of the Al_2O_3 layer enables both high-speed and multitimescale neuromorphic operations. Detailed parameters used in the simulations are summarized in Table S2 (Supporting Information).

Beyond image recognition, our transistors can also be utilized for high-speed tactile sensors and signal filtering, depending on the operating speed and desired retention characteristics. For instance, SiO_2/WO_3 transistors with fast operation and short retention times can serve as artificial nociceptors, as illustrated parallelly with biological analogy in Figure 5a. Nociceptors are key sensory receptors distributed throughout the human body that detect harmful stimuli and generate action potentials, which are transmitted to the central nervous system via the spinal cord to initiate protective motor responses and prevent further injury.[51,52] They respond only when the strength of the external stimulus is beyond a certain threshold and exhibit relaxation (the pain reduces gradually) once the stimulus is removed. If the nociceptor is damaged under strong harmful stimuli, then the pain sensation is enhanced under subsequent weak stimuli, which is defined as the pain sensitization. Artificial nociceptors are crucial to develop electronic skin and humanoid robots for sophisticated task performance under different atmospheres. Figure 5b shows the threshold spiking behavior of SiO_2/WO_3 transistors under V_G pulses with increased amplitudes from +2 to +7.2 V (3 ms pulse width and 0.5 s interval). The I_D shows almost no response up to +6 V, but beyond which the current increases (i.e., a pain response) rapidly with an increasing pulse amplitude, which is consistent with that of human nociceptors. Here, a threshold current (I_{th}) of 50 nA is set for pain recognition (green dashed line), and the corresponding threshold amplitude of +7 V (pink dashed line) is required. When the V_G pulse is less than +7 V, a pulse width of at least 10 ms is needed to exceed the threshold current. This is evident from the pulse width-dependent I_D response shown in Figure 5c, where the amplitude is fixed at +6 V. This indicates that even a painless signal can become a painful signal if exposure to it lasts longer enough. This pain response is represented by the counter map shown in Figure 5d, in which the pain response is plotted as a function of pulse amplitude and width. The dashed line defines the threshold boundary for the pain response, distinguishing between innocuous and harmful stimuli. The I_{th} is selected as the operational threshold to clearly differentiate between the subthreshold resting state ($I_D < I_{th}$, innocuous/nonpainful regime) and the beyond-threshold active state ($I_D > I_{th}$, noxious/painful regime). The selected value is well above the channel current baseline (~few nA) and corresponds to the onset of significant channel conductance activation under noxious pulse trains. This also ensures a high signal-to-noise ratio when defining pain response metrics like latency and hyperalgesia.

When the harmful stimulus is removed, nociceptors begin to relax, and the pain sensation gradually goes away depending on the level of injury. To emulate this relaxation characteristic, the transient current responses after harmful stimuli (≥7 V) are measured. In the case of mild injury (+7 V, 5 ms), the pain relaxes in less than 1 s, whereas pain relaxes partially under strong injury (+8 V, 5 ms) and persists for a much longer time, as shown in Figure 5e. Another important feature of nociceptors is the temporal correlation between consecutive harmful stimuli. This was demonstrated by applying a pair of identical V_G pulses (+7 V, 5 ms) at various interval times, and the ratio of the channel currents (I_2/I_1) is plotted as a function of interval time in Figure 5f. The current ratio is high for shorter intervals (<200 ms) and becomes nearly one for longer intervals, which means that the device does not induce pain potentiation for longer intervals. This temporal integration can be further realized by the frequency-dependent current response, as shown in Figure 5g. While high-frequency pulses (5 Hz or higher) cause a high pain response ($I_D > I_{th}$), the device does not generate a pain sensation with low-frequency pulses (2 Hz or less).

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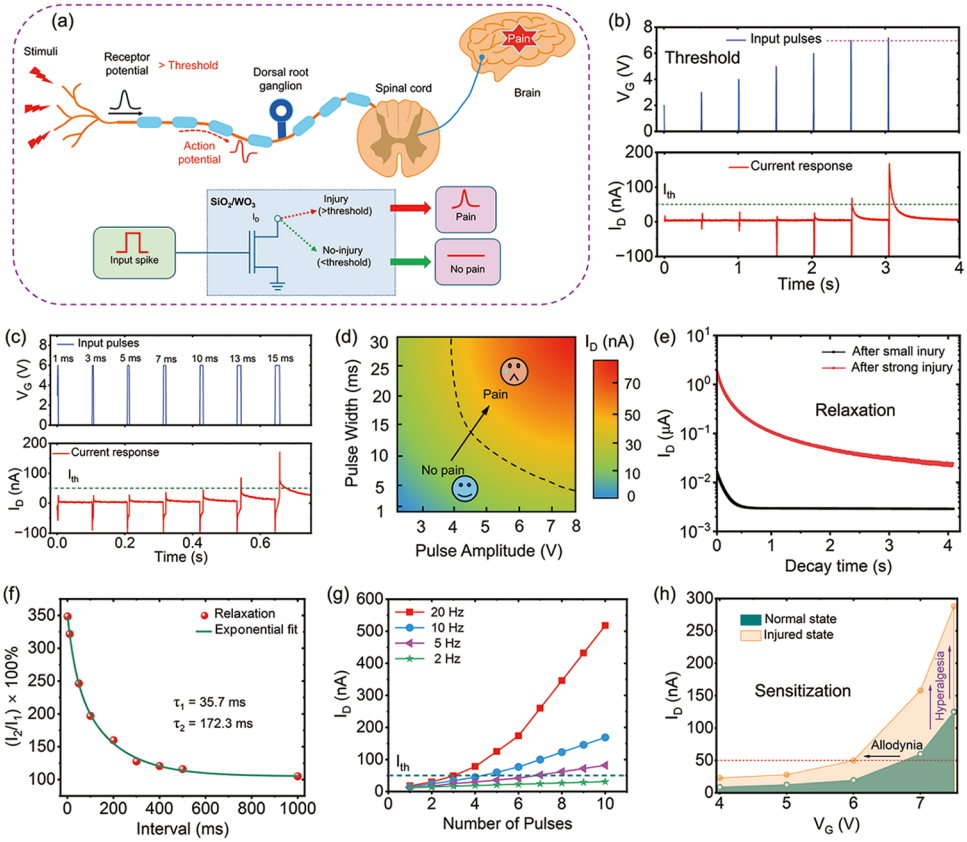


Figure 5. Nociceptive (pain-sensing) characteristics of an SiO_2/WO_3 transistor. (a) Schematic illustration of the pain perception mechanism in biological nociceptors and analogous function of the transistor. (b) Threshold characteristics of the transistor under V_G pulses with increased amplitudes (b) and pulse widths (c). The dashed curve indicates the threshold current (I_{th}). (d) Counter map of pain perception as a function of the pulse amplitude and width. (e) Relaxation behavior under weak and strong injury pulses. (f) Temporal correlation between successive harmful stimuli. (g) Frequency-dependent pain responses under repetitive noxious stimulation. (h) Sensitization-induced allodynia and hyperalgesia characteristics.

In contrast, $SiO_2/Al_2O_3/WO_3$ transistors having longer retention times cannot reduce pain sensation even after the stimulus is removed, as shown in Figure S18 (Supporting Information), making them unsuitable for nociceptor applications. Note that sharp negative and positive current spikes in Figure 5b,c correspond to charging and discharging currents of the parasitic capacitance including the device and measurement system. These short transient currents do not represent a persistent device state and therefore do not affect the programmed conductance levels of the device.[53] Nevertheless, they may contribute to transient current overshoot and additional energy consumption during high-speed pulse operations, which should be minimized by slowing the pulse rise/fall time, optimizing device structures, etc. In all the measurements of Figure 5, the 50 nA threshold was evaluated at approximately 50 ms after the positive spike edge to minimize the effect of capacitive transient current.

All the functions of nociceptors described above apply to the normal nonsensitized (undamaged) state. However, to protect the body from further injury, nociceptors exhibit a phenomenon known as pain sensitization when damaged. In the injured state, pain response is enhanced under painful stimuli compared to the normal condition (known as hyperalgesia) and pain sensation is induced by normally painless (below the threshold) stimuli (known as allodynia).[54] This pain sensitization behavior is demonstrated by applying a series of V_G pulses with amplitudes increasing from +3 to +7.5 V in the normal state and the injured state prepared by subjecting a strong V_G pulse (+8 V, 10 ms). Figure 5h shows the current response I_D in the normal and injured states plotted as a function of the pulse amplitude. The I_D (i.e., pain response) induced by each pulse is significantly increased in the injured state compared to the normal state, and the magnitude of this increase enhances as the intensity of the stimulus (pulse amplitude) increases, emulating the hyperalgesia characteristic of nociceptors, as indicated by the purple arrows. On the other hand, the I_D reaches the threshold level after injury at a pulse amplitude of +6 V, which is lower than the pulse amplitude (+7 V) required in the normal state. This replicates the allodynia characteristic of nociceptors, as indicated by the black arrow.

Finally, we integrated two transistors with different retention times to construct a 1T−1S cell for scalable neuromorphic systems capable of spatial and temporal control. In this configuration, a SiO_2/WO_3 transistor with short retention works as an access transistor (AT), while a $SiO_2/Al_2O_3/WO_3$ transistor with long retention serves as a synapse transistor (ST). As schematically illustrated in Figure 6a, the source of AT is connected to the gate of ST, enabling gate-controlled transmission of programming signals. This configuration preserves the intrinsic synaptic plasticity while providing an additional degree of freedom to dynamically transmit, suppress, or filter synaptic updates without modifying the input stimuli, analogous to

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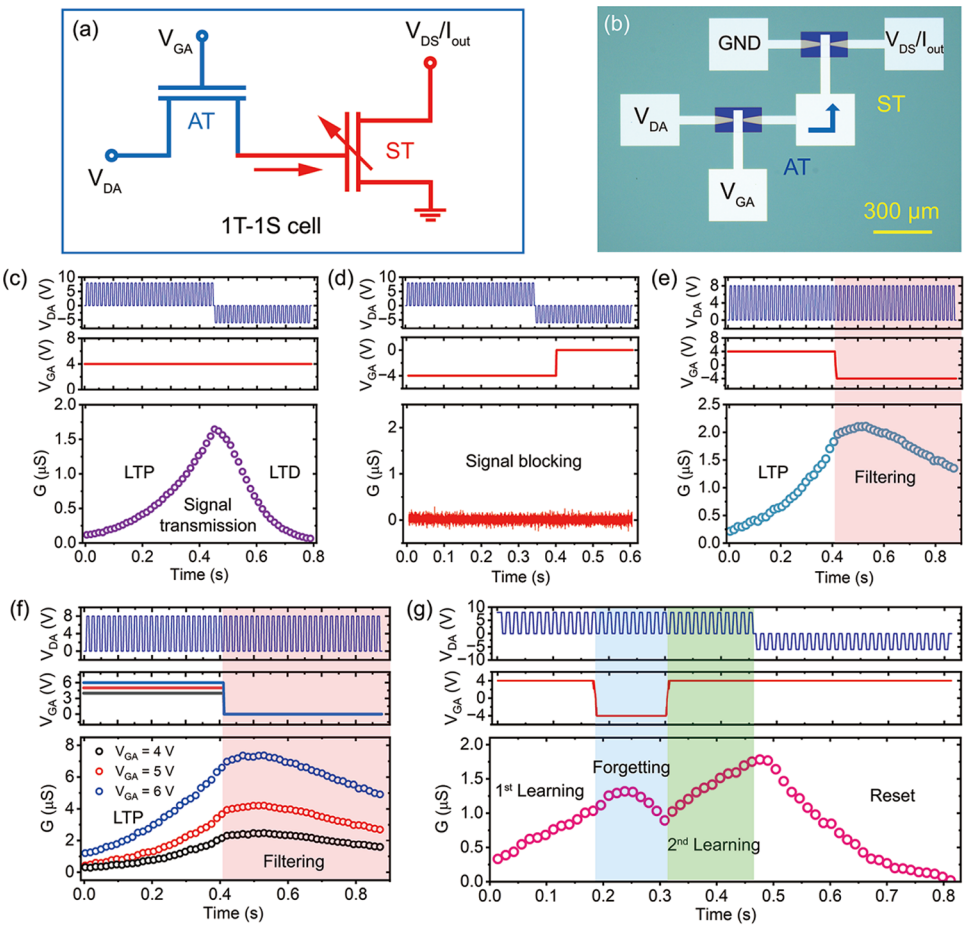


Figure 6. (a) Circuit diagram for a 1T−1S cell composed of a SiO_2/WO_3 access transistor (AT) and a $SiO_2/Al_2O_3/WO_3$ synapse transistor (ST). (b) Optical microscope image of the fabricated 1T−1S cell. Output conductance under (c) signal transmission, (d) signal blocking, and (e) LTP and signal filtering of the synapse controlled by V_{GA}. (f) LTP and signal filtering under different V_{GA}. (g) Repetitive learning and forgetting behavior demonstrated by gate controlling of AT.

event-driven learning/forgetting processes of the brain. In addition, it allows selective refreshing of the memory cells, thus preventing unnecessary energy consumption when processing nonessential information. Figure 6b shows an optical microscope image of the typical 1T−1S cell. Synaptic programming pulses and a constant bias are applied to the drain (V_{DA}) and gate (V_{GA}) of AT, respectively, and the output G is read at the drain (V_{DS}) of ST with applying a small voltage (0.1 V). Figure 6c shows the LTP and LTD characteristics at V_{DS} of ST under application of consecutive positive (+8 V) and negative (−5 V) pulses (5 ms width) to V_{DA} with positive bias (+4 V) to V_{GA}. The resulting conductance change closely matches that of a single $SiO_2/Al_2O_3/WO_3$ transistor (Figure 4e), confirming effective signal transmission without disturbing its intrinsic synaptic characteristic. In contrast, if negative bias (−4 V) is applied to V_{GA} with the same pulse train to V_{DA}, then signal transmission to the ST is completely blocked, as shown in Figure 6d. Even if V_{GA} is set at 0 V afterward, the signal is still not transmitted. Figure 6e shows the change in G when the voltage applied to V_{GA} is switched from positive (+4 V) to negative (−4 V) while positive pulses are applied to V_{DA}. The G initially increases with LTP but decreases gradually once V_{GA} becomes negative. This demonstrates selective learning and forgetting behaviors of the ST through signal filtering and gating capability of the AT, which are analogous to the event-driven learning behavior in the human brain.

Another important feature of the 1T−1S cell is that the AT acts as an analog switch, distinguishing it from conventional Si-based CMOS transistors. Figure 6f shows the change in G under application of positive pulses (+8 V) to V_{DA}, when different positive voltages (+4 to +6 V) are applied to V_{GA} and then switched to 0 V. As V_{GA} increases, the magnitude of the increase in G becomes larger, indicating that signal transmission becomes progressively stronger due to the gate controlling of the AT. When V_{GA} is set to 0 V, G decreases gradually. However, since the rate of decrease is almost constant, the final output G is determined by the magnitude of the positive V_{GA}. We further simulated iterative learning and forgetting behavior by sequentially altering the polarity at V_{GA}. Figure 6g shows the change in G under application of consecutive positive and negative pulses to V_{DA} with varied V_{GA} between +4 and −4 V. By changing the polarity of V_{GA}, the learning (LTP) and forgetting (signal filtering) processes are repeated under positive pulses at V_{DA}, as indicated by the blue and green shaded areas. Finally, by applying negative pulses at V_{DA}, the G decreases to the initial state, resetting the synaptic weight. Note that all the measurements were carried out using voltage pulses with a 5 ms width and interval. Similar behavior was

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observed in a 1T−1S cell composed of alkali ion-gating transistors using a HfO_2 dielectric,[55] but on a timescale more than 10 times longer than our results. The 1T−1S architecture not only enables reliable synapse selection and sneak-path suppression in a crossbar array but also provides an additional degree of freedom for implementing event-driven learning/forgetting at the hardware level. Moreover, realizing synapse transistors with different retention times within the same oxide material platform can reduce fabrication complexity, circuit overhead, and energy consumption, which will support scalable neuromorphic systems.

3. CONCLUSIONS

In summary, this study presents a robust interface engineering strategy to resolve the long-standing trade-off between fast response and long-term stability in ion-gated oxide synapse transistors. By inserting a thin Al_2O_3 diffusion barrier layer between the SiO_2 electrolyte and WO_3 channel, proton migration dynamics are effectively controlled, enabling the emulation of a broad range of biologically relevant synaptic behaviors. These transistors exhibit reliable channel conductance modulation at low gate voltages, with a large dynamic range ($>10^3$) and excellent cycle-to-cycle and device-to-device reproducibility. Essential biosynaptic functions, including long-term potentiation and depression, as well as spike-rate- and amplitude-dependent plasticity, are successfully demonstrated. EB-deposited SiO_2 electrolytes offer high proton mobility, delivering high-speed operation with a pulse width of 50 μs and a retention time of ∼18 s. The introduction of a thin Al_2O_3 diffusion barrier effectively suppresses proton back-diffusion, yielding stable long-term potentiation with a retention time reaching ∼860 s and improving the linearity of weight updates at low conductance levels (∼100 nS). Furthermore, the devices operate with high energy efficiency (down to ∼200 fJ per synaptic event) and achieve a high image recognition accuracy of ∼90% based on an ANN model. In particular, the device with an Al_2O_3 layer exhibits a recognition accuracy of ∼85% across a wide range of pulse widths, from subsecond to submillisecond. Beyond single-device operation, the 1T−1S architecture composed of two transistors with different retention times provides a programmable temporal gating for synaptic updates, enabling selective learning and forgetting. These findings will lead to the establishment of an oxide-based transistor platform that is easy to integrate and capable of emulating complex biological synaptic behaviors across multitimescales.

4. EXPERIMENTAL SECTION

4.1. Device Fabrication

The transistors were fabricated on Si substrates coated with 200 nm SiO_2. First, the source and drain electrodes (with channel length and width of 2 and 25 μm, respectively) were patterned using maskless lithography (NanoSystem Solutions DL-1000). Then, a 5 nm-thick Ti adhesive layer and 35 nm-thick Pt electrodes were deposited onto the patterned substrate using an EB evaporator followed by a lift-off process. Next, the channel region of 300 μm × 200 μm was lithography-patterned, and 20 nm-thick WO_3 was deposited as the channel by RF magnetron sputtering at room temperature from a WO_3 target at 50 W with 5 sccm Ar and 0.2 sccm O_2 flow rates. Then, 35 nm-thick SiO_2 was EB-deposited as the electrolyte. The SiO_2 raw material was purchased from Soltech Co., Ltd. and has a purity of 4N or higher, with the content of impurities such as Si and Nb at 10 ppm or less. For the $SiO_2/Al_2O_3/WO_3$ transistor, thin (1.5−7 nm thick) Al_2O_3 was sputtered subsequently after the WO_3 sputtering at 100 W with similar Ar and O_2 gas flows. After all necessary depositions, a lift-off process was performed. Finally, the gate electrode was lithographically patterned, and 30 nm-thick Pd and 20 nm-thick Au were EB-deposited followed by a lift-off process. To fabricate the 1T−1S cells, four lithography steps were conducted with each step involving resist patterning, film deposition, and lift-off. First, the source/drain electrodes and connecting metal lines were patterned while maintaining the same channel dimensions as those of the single transistors, followed by Pt deposition and lift-off. Next, the channel regions of the ATs were patterned, followed by sequential deposition of WO_3 and SiO_2. Then, the channel regions of the STs were patterned, followed by sequential depositions of WO_3, Al_2O_3, and SiO_2. Finally, the Au/Pd gate electrodes were patterned and deposited on the prefabricated structures.

4.2. Material Characterization

The structural properties of EB-deposited SiO_2 and sputtered WO_3 films were characterized by XRD (Rigaku SmartLab) equipped with Cu Kα ($\lambda = 0.154$ nm) in θ−2θ geometry for 2θ ranging from 20° to 80°. XRR measurements were performed to evaluate the film density using the same equipment. The chemical compositions were identified using HAXPES (Ulvac-PHI Quantes) equipped with Cr Kα (energy: 5414.8 eV). The microstructure of stacked layers was captured using scanning TEM equipped with a 200 kV field emission gun (Talos F200X G2, Thermo Scientific) in a cross-sectional mode. In addition, the associated EDS was employed to identify elemental distribution along the cross-sectional region. FTIR measurements were carried out to analyze the chemical bonding state of the films in an attenuated total reflection mode, using a Thermo Fisher Scientific iS5.

4.3. Electrical Measurement

Electrical characterizations of the fabricated transistors were carried out using a three-probe system at an ambient atmosphere and a four-probe vacuum system under vacuum conditions. The DC $I-V$ characteristics were measured in sweep mode using source measure units (SMUs), while pulsed $I-V$ measurements were performed using pulse measure units (PMUs), with a semiconductor parameter analyzer (Keithley 4200SCS/F). For all measurements, the source electrode was kept grounded, and the I_D was measured by applying a bias to the drain electrode. A sweep voltage or pulse voltage was applied to the gate electrode.

■ ASSOCIATED CONTENT

Supporting Information

The supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.6c14036.

Optical microscope image of the source/drain electrodes, elemental line profile obtained from EDS measurements, XRD patterns of EB-deposited SiO_2 and WO_3 films, output and transfer curves, device-to-device variations in transfer curves, gate leakage current characteristics, XRR spectra fitted with simulation curves, HAXPES survey and core-level spectra, FTIR spectra of EB-deposited SiO_2 and sputtered SiO_2 films, EIS results of two-terminal devices, capacitance−frequency plots of two-terminal devices, transfer curves under different ambient conditions and different RH levels, transfer curve of a transistor with sputtered SiO_2, temperature dependence of LTP/LTD and retention characteristics, LTP/LTD of a transistor with a thick EB-deposited SiO_2, I_D response under V_G pulses to estimate ΔI_D, plots of normalized conductance vs normalized number of pulses to estimate nonlinearity factors, image recognition accuracy

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calculated with SiO_2/WO_3 transistors, nociceptive characteristics of a $SiO_2/Al_2O_3/WO_3$ transistor, performance comparison table of our devices with previously reported devices, and parameters used in NeuroSim+ simulations (DOCX)

AUTHOR INFORMATION

Corresponding Authors

Rupam Mandal − *Research Center for Materials Nanoarchitectonics (MANA), National Institute for Materials Science, Tsukuba 305-0044, Japan;* Email: MANDAL.Rupam@nims.go.jp

Tohru Tsuruoka − *Research Center for Materials Nanoarchitectonics (MANA), National Institute for Materials Science, Tsukuba 305-0044, Japan;* orcid.org/0000-0002-4322-4309; Email: TSURUOKA.Tohru@nims.go.jp

Author

Kazuya Terabe − *Research Center for Materials Nanoarchitectonics (MANA), National Institute for Materials Science, Tsukuba 305-0044, Japan;* orcid.org/0000-0003-3988-3456

Complete contact information is available at: https://pubs.acs.org/doi/10.1021/acsami.6c14036

Notes

The authors declare no competing financial interest.

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