

Characterization of Interface States in CVD Monolayer MoS₂/Al₂O₃ MOS Capacitors Via the Conductance Method

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Abstract—MoS₂ is one of the transition metal dichalcogenides (TMDs) that has been extensively studied as a next-generation semiconductor material due to its high carrier mobility in the monolayer limit. However, the atomically thin nature of MoS₂ poses challenges for capacitance characteristics measurements by metal-oxide-semiconductor (MOS) capacitors, leading to limited research on the characteristics of their interfaces. In this study, we fabricated MOS capacitors with different device areas using a monolayer MoS₂ synthesized by chemical vapor deposition and Al₂O₃ insulator deposited by atomic layer deposition and performed capacitance-voltage measurements. We propose the use of a ring-shaped capacitor which is beneficial for small 2D crystals such as exfoliated TMDs or materials that cannot yet be synthesized on a large scale, and extracted interface trap densities on the order of $10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ for devices with different areas, indicating that under the present measurement conditions, series and access resistances do not dominate the extraction of interface trap density using the conductance method.

Index Terms—conductance method, interface states, metal-oxide-semiconductor capacitors, monolayer MoS₂, two-dimensional transition metal dichalcogenides

I. INTRODUCTION

SINCE the discovery of high-performance transistors based on mechanically exfoliated monolayer MoS₂ [1], it has become a prototypical material for two-dimensional (2D) semiconductor research. Its atomically thin body, combined with an optical bandgap of approximately 1.8–1.9 eV [2] and

reasonably high carrier mobility [3], [4], affords strong electrostatic control [5], [6] and mitigates short channel effects [7], [8], motivating extensive device and interface studies. Conventional capacitance-voltage (C–V) measurements on ultrathin 2D materials MOS capacitors [9]–[11] exhibit additional frequency-dispersion arising from transverse electric field distributions, parasitic capacitances, and resistance associated with carrier supply from the contact electrodes and lateral carrier transport in the MoS₂ region (R_{acc}), all of which complicate the accurate extraction of interface trap density (D_{it}) [12]. Among various characterization techniques, the conductance method is widely regarded as a reliable approach for evaluating D_{it} in MOS structures [12]–[15], as it enables the analysis of voltage and frequency dependence of the conductance in MOS capacitors to analyze the impact of interface states. In this study, we focus on establishing the repeatability and reliability of the conductance method for monolayer MoS₂ MOS capacitors. A ring-shaped capacitor geometry is introduced to obtain a sufficiently large gate-modulated capacitance even from small-area 2D crystals, while enabling the influence of R_{acc} to be evaluated through the diameter dependence of the C–V, C–f, and conductance characteristics. This approach allows reproducible D_{it} extraction and clarifies the measurement conditions under which R_{acc} does not dominate the conductance response.

II. EXPERIMENTAL

Figure 1(a) illustrates the fabrication process flow, while Figure 1(b) and 1(c) present the schematic diagram and optical micrograph of the fabricated devices, respectively. The fabrication process began with the deposition of a metal gate on a glass substrate. Lift-off resist, polymethyl methacrylate (PMMA) A5, and Aqua Save were spin-coated to prevent electron charge-up. Following electron beam lithography (EBL), a 5-nm-thick Ti followed by a 10-nm-thick Pd was deposited using electron beam evaporation. The lift-off process was performed in N-Methyl-2-pyrrolidone. Subsequently, 12.4-nm-thick of Al₂O₃ was grown at 300°C by atomic layer deposition (ALD) using trimethylaluminum and H₂O as precursors. Al₂O₃ thickness was confirmed by spectroscopic ellipsometry. The CVD-grown monolayer MoS₂ was then transferred onto Al₂O₃ using polystyrene (PS) as the carrier polymer [16]. The transfer process involved spin-coating PS onto the as-grown MoS₂, followed by baking at 80°C for 15

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minutes to enhance adhesion. Water was introduced at the interface between MoS₂ and the growth substrate to initiate the lift-off process. Once detached, the MoS₂-PS assembly was dried and transferred onto the target substrate. To improve adhesion and eliminate wrinkles, the transferred MoS₂ was baked at 80 °C for 1 hour, followed by 150 °C for 30 minutes. Finally, the PS layer was removed using toluene. After MoS₂ transfer, PMMA A5 and Aqua Save were spin-coated for the MoS₂ etching process. Following patterning via EBL, the samples underwent O₂ plasma etching, after which the resist was removed using acetone. For contact metal deposition, PMMA and Aqua Save were spin-coated before patterning via EBL. A 10-nm-thick In followed by a 30-nm-thick Au was deposited using electron beam evaporation, followed by a lift-off process in acetone. The devices were fabricated in two batches using an identical fabrication process. Batch 1 consisted of devices with ring diameters of 10, 15, and 20 μm while Batch 2 included devices with ring diameters of 20, 30, and 40 μm. The fabricated devices were annealed in a vacuum at 523 K for 1 hour to improve contact properties. Multi-frequency C–V and conductance measurements were conducted on bottom-gated MOS capacitors using an HP 4824A LCR meter under vacuum at 300 K.

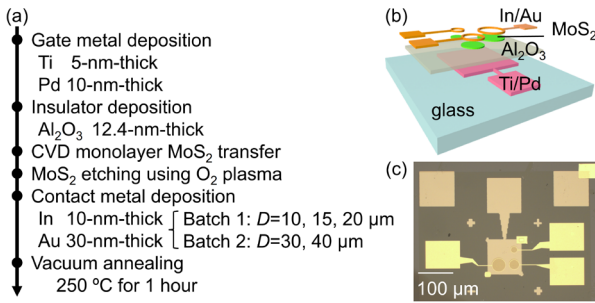


Fig. 1 (a) Fabrication process flow for device fabrication, (b) Schematic illustration of the device structure, and (c) Optical microscopy image.

III. RESULTS AND DISCUSSION

Figure 2 shows the normalized multi-frequency forward and backward C–V curves (1 MHz to 60 kHz) for devices with ring diameters of 10, 15, 20 μm.

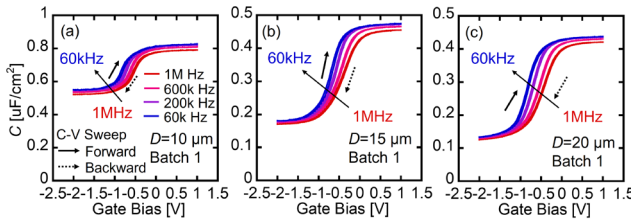


Fig. 2 Measured multi-frequency C–V characteristics for devices with the diameters of (a) 10 μm, (b) 15 μm, and (c) 20 μm.

The C–f mapping in Figure 3(a) shows that the high-frequency capacitance roll-off becomes more pronounced with increasing device diameter, suggesting an additional RC delay associated with lateral carrier supply. In contrast, the weaker and less diameter-dependent dispersion observed in smaller-diameter devices indicates that the influence of R_{acc} is not dominant under these measurement conditions. Therefore, the C–f mapping supports the validity of the conductance-based D_{it} extraction in the smaller-diameter devices by confirming that

the measured admittance response is not dominated by lateral access resistance. Figure 3(b) shows a simplified equivalent circuit used to illustrate the main capacitance and resistance components in the measured admittance response. In the depletion region, the minimum capacitance (C_{min}) is determined by the series combination of the depletion capacitance of MoS₂ (C_{D}) and the oxide capacitance (C_{ox}), in parallel with the overlap capacitance (C_{ov}) originating from the overlap between gate and contact. The C_{ov} does not scale with the device diameter. As the ring diameter decreases, the contribution of C_{ov} to C_{min} increases, which results in a corresponding increase in C_{min} . The apparent flat-band voltage (V_{FB}) was estimated from the linear extrapolation of the $1/C^2$ –V characteristics at 1 MHz, where C is the measured capacitance after subtracting C_{min} to reduce the influence of the offset capacitance. The fixed charge (Q_{ox}) was then calculated (Figure 3(c)). The forward and backward sweeps exhibited a small V_{FB} shift ($\Delta V_{\text{FB}} \sim 0.05$ V), corresponding to a charge-equivalent hysteresis of $\Delta Q_{\text{ox}} \sim 1.8 \times 10^{-8}$ C/cm². The extracted slow trap density (ΔN_{st}) showed $\Delta N_{\text{st}} < 1.2 \times 10^{11}$ cm⁻². This minimal hysteresis and small ΔN_{st} quantitatively indicate a low density of slow traps in the fabricated devices.

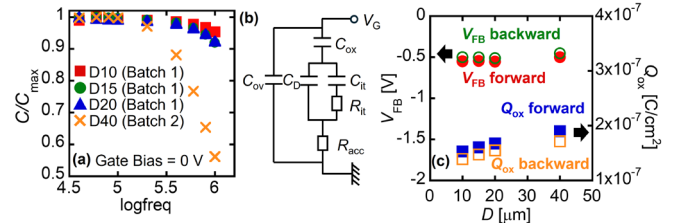


Fig. 3 (a) Measured C–f mapping, (b) Simplified equivalent circuit diagram, (c) Extracted V_{FB} and Q_{ox} for each device.

In this study, C_{ox} was extracted from the C–V characteristics. In the depletion region, the measured capacitance primarily reflects the C_{ov} . In the accumulation region, both C_{ox} and C_{ov} contribute to the total measured capacitance [17]. To minimize the influence of the overlap capacitance in calculating D_{it} , C_{ox} was defined as the difference between C_{max} in accumulation and C_{min} in depletion measured at 60 kHz. From the obtained C_{ox} value, the dielectric constant $k = C_{\text{ox}}d/\epsilon_0$ and the equivalent oxide thickness $\text{EOT} = \epsilon_{\text{SiO}_2}/C_{\text{ox}}$ were calculated, yielding $k = 5.7 \pm 0.4$ and $\text{EOT} = 8.5 \pm 0.6$ nm, where d is the Al₂O₃ thickness, ϵ_0 is the vacuum permittivity, and $\epsilon_{\text{SiO}_2} = 3.9\epsilon_0$.

Following C–V measurements, conductance measurements were performed to evaluate D_{it} . $G_p/A\omega q$ is plotted as a function of frequency for devices with ring diameters of 10, 15, 20, 30, and 40 μm (Figure 4). Due to the inherently low capacitance of small ring capacitors, it is challenging to obtain reliable G–f curves, especially in the low-frequency region, as the signal amplitude becomes comparable to the noise level of the LCR meter. The measured conductance (G_m) is converted to a parallel conductance (G_p) using the following relation [18]:

$$\frac{G_p}{A\omega q} = \frac{\omega C_{\text{ox}}^2 G_m}{G_m^2 + \omega^2 (C_{\text{ox}} - C_m)^2} \quad (1)$$

Here, C_m is the measured capacitance. G_p is normalized with the area (A), frequency (ω), and charge (q). The dispersion of curves indicates that a smaller device area affects both capacitance and conductance measurements, especially at low frequencies (Figure 4(a)).

D_{it} is calculated by using the following relation [18],

$$D_{it} = 2.5 \left(\frac{G_p}{A\omega q} \right)_{\max}$$

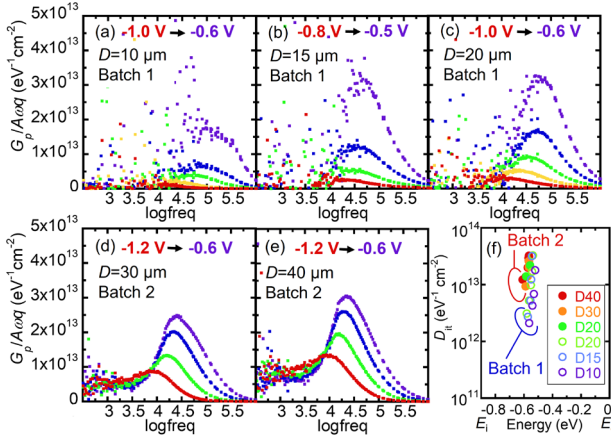


Fig. 4 Measured $G_p/A\omega q$ versus log(frequency) for MOS capacitors with ring diameters of (a) 10 μm , (b) 15 μm , (c) 20 μm , (d) 30 μm , and (e) 40 μm , (f) Extracted D_{it} for devices with different diameters.

Regardless of the ring diameter, the D_{it} values ranged from 10^{12} to $10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$ at the energy position of $\sim 0.6 \text{ eV}$ below the conduction band (Figure 4(f)). The energy level of the trap states was calculated using the following equation [12]:

$$\frac{1}{f} = \frac{\exp\left(\frac{\Delta E}{kT}\right)}{\sigma v_{th} N_{DOS}}$$

Here, ΔE represents the energy difference between the minimum of the conduction band and the position of the Fermi level. N_{DOS} is the density of states in the conduction band per unit area, and σv_{th} denotes the carrier capture probability for a trap at a specific energy level. Based on previous research [12], the parameters were set as follows: $N_{DOS} = 4.5 \times 10^{13} \text{ cm}^{-2}$, $v_{th} = 1.4 \times 10^7 \text{ cm/s}$, $\sigma_{\text{MoS}_2} = 10^{-7} \text{ cm}$. The D_{it} values were observed near the conduction band and increased as they approached the band edge. The extracted D_{it} values were consistent across devices with different ring diameters (Figure 4(f)). This result, together with the C-f mapping in Fig. 3(a), indicates that R_{ac} becomes detectable as a high-frequency capacitance roll-off in larger-diameter devices, whereas it does not dominate the conductance response used for D_{it} extraction under the present measurement conditions. Therefore, the diameter-independent D_{it} values confirm that the conductance method can provide reliable and reproducible D_{it} extraction in the ring-shaped MoS₂ MOS capacitors, while the diameter dependence of the C-f characteristics provides a useful indicator of access resistance-related distortion. Furthermore, the results of devices with a 20 μm diameter fabricated in Batch 1 and Batch 2 were compared. The D_{it} values extracted via the conductance method remained consistent (Figure 4(f)). These results indicate that, although there are variations in the 1L MoS₂ device fabrication process such as transfer-induced variations, the conductance method consistently yields reliable D_{it} values. This confirms the applicability of this method for characterizing the interface properties of Al₂O₃/MoS₂ MOS capacitors, ensuring stable and reproducible evaluation of interface trap density.

Finally, we compared D_{it} obtained from the ring capacitor and FETs ($L_{ch} = 0.5 \mu\text{m}$, $2 \mu\text{m}$; $W_{ch} = 60 \mu\text{m}$) (Figure 5). A good agreement was observed between the ring capacitor with

diameter of 20 μm and the FET with $L_{ch} = 0.5 \mu\text{m}$. On the other hand, for the FET devices, D_{it} increased with longer channel lengths, even within the same batch, consistent with the calculation in a previous study [19], which showed that the channel resistance can affect accurate D_{it} measurements when the channel length is larger than 1 μm . Moreover, for shorter L_{ch} , a larger W_{ch} is required to achieve a sufficiently large capacitor area to improve the signal-to-noise ratio, making the measurement difficult when exfoliated flakes or non-large-area CVD-grown crystals are used. In contrast, the ring-shaped capacitor provides sufficient area for reliable C-V and conductance measurements even from small-area 2D crystals, and its diameter dependence enables evaluation of the effect of R_{acc} on the C-V and conductance characteristics.

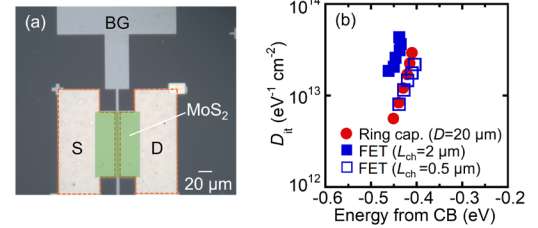


Fig. 5 (a) Optical microscopy image of FET, (b) Extracted D_{it} for ring capacitor ($D = 20 \mu\text{m}$) and FETs ($L_{ch} = 0.5 \mu\text{m}$, $2 \mu\text{m}$; $W_{ch} = 60 \mu\text{m}$).

The obtained D_{it} values (10^{12} - $10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$) are comparable to those reported for other TMDC/high- k interfaces (Table 1). In addition, this study confirms the reliability and reproducibility of the conductance method, indicating the ring-shaped capacitor structure enables accurate D_{it} extraction even from small-area monolayer 2D crystals.

Table. 1 Summary of reported D_{it} values for TMDC/high- k interfaces.

Mat.	Dielectric	Layers (L)	Method	$D_{it} (\text{cm}^{-2} \text{ eV}^{-1})$	ref.
MoS ₂	Al ₂ O ₃	1-L (CVD)	conductance	10^{12} - 10^{13}	this work
MoS ₂	HfO ₂	1-L (CVD)	conductance	10^{12} - 10^{13}	[12]
MoS ₂	HfO ₂	Few-L (exf.)	CV	2×10^{11} - 2×10^{12}	[20]
WSe ₂	Al ₂ O ₃	Multi-L (exf.)	CV	$\sim 10^{11}$	[21]
WS ₂	Al ₂ O ₃	Multi-L (exf.)	CV	$\sim 4 \times 10^{11}$	[22]

IV. CONCLUSION

In this study, C-V characteristics of Al₂O₃/MoS₂ MOS capacitors with varying ring diameters of electrodes were investigated. The results demonstrated that frequency dispersion decreased as the device area was reduced. D_{it} was extracted using the conductance method, and the values were observed to increase near the band edge, ranging from 10^{12} to $10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$. Notably, the extracted D_{it} values remained consistent regardless of the electrode size, indicating that the device area in the current experimental setup does not influence D_{it} extraction. Moreover, comparison of conductance measurements for devices fabricated in different batches but with the same electrode area showed similar D_{it} values. These findings confirm the reliability and repeatability of the conductance method for evaluating interface states in insulator/MoS₂ MOS capacitors. Importantly, the ring-shaped capacitor is advantageous for using small 2D crystals, such as exfoliated TMDCs or materials not yet producible on a large scale, making it a promising structure for extending this approach to a broader class of 2D materials. We have also confirmed that this method can be applied to small-area exfoliated MoS₂ flakes, further supporting its applicability to interface-state evaluation of 2D semiconductor systems.

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