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Dielectric-Stack-Engineered Anti-Ambipolar Transistors for Low-Voltage Ternary Logic

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ABSTRACT We demonstrate an ultralow-voltage ternary multi-valued logic (MVL) inverter based on an extended *p*-channel anti-ambipolar transistor (E*p*-AAT) employing an optimized HfO_2/polystyrene gate dielectric stack. The HfO_2 dielectric enables low-voltage operation, while the polystyrene surface layer provides a low-surface-energy interface for stable organic channel formation. The E*p*-AAT exhibits an intrinsic N-shaped transfer characteristic with a clear negative transconductance region, explained by the combined contributions of the *N1*, *P1*, and *P2* channels. Integrated with an *n*-type transistor, the E*p*-AAT realizes a ternary MVL inverter with three distinct logic states at a supply voltage of 2 V without additional circuit complexity. These results highlight the potential of HfO_2/polystyrene-based E*p*-AATs for MVL circuits.

INDEX TERMS Anti-ambipolar transistor, negative transconductance, ternary multi-valued logic, ultralow-voltage inverter, high-k gate dielectric.

I. INTRODUCTION

As energy efficiency has become a primary constraint in modern computing systems, multi-valued logic (MVL) has gained attention as an alternative to conventional binary logic [1], [2]. Ternary logic has the potential to reduce circuit complexity and switching operations by increasing information density. However, existing implementations often rely on circuit overhead such as multiple transistors, resistive networks, or precise voltage division schemes [3], [4]. Thus, device-level approaches that generate ternary outputs are highly desirable. Recently, anti-ambipolar transistors (AATs) exhibiting nonlinear N-shaped transfer characteristics with negative transconductance (NTC) have been used for MVL. Yet, conventional devices still require high operating voltages [5].

In this work, we propose an organic semiconductor-based extended *p*-channel anti-ambipolar transistor (E*p*-AAT) integrated with an optimized dielectric stack. A fully extended *p*-channel architecture is combined with a high-k HfO_2 gate dielectric and a polystyrene (PS) surface layer to enable low-voltage operation. HfO_2 dielectric reduces the operating voltage, while PS optimizes the interface for uniform channel formation. Unlike conventional AATs, the E*p*-AAT forms an N-shaped transfer characteristic and NTC region through the interplay of the *N1*, *P1* and *P2* channels, driven by the competition between electron and hole transport.

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TABLE 1. Comparison of ternary MVL inverters based on AAT-type devices.

Channel	Dielectric	| V_{DD} | [V]	| V_{IN} | [V]	Gain [V/V]	V_{peak} to V_{valley} range [V]	Ref.
α-6T/PTCDI-C8	Al_2O_3/PMMA	10	10	N/A	N/A	[1]
C8-BTBT/PhC_2-BQQDI	HfO_2	10	6	N/A	N/A	[7]
DNTT/PTCDI-C13	pV3D3	8	8	-30	-4.2 V to -6.9 V (ΔV = 2.7 V)	[8]
DNTT/PTCDI-C13	pC1D1/pV3D3	5	5	−24.21 ± 1.55	-1.5 V to -2.6 V (ΔV = 1.1 V)	[9]
Pentacene/Cl−SAM/Ph-SAM	HfO_2	5	5	<-3	N/A	[10]
SWCNTs/MoS_2	HfO_2	3	3	<10	< 0.1 V to < -0.8 V (ΔV < 1 V)	[11]
C8-BTBT/PhC_2-BQQDI	HfO_2/PS	2	2	16.9 ± 2.5	-1.35 V to -1.75 V (ΔV = 0.4 V)	**This work**

By integrating the E*p*-AAT with an *n*-type transistor, we demonstrate ternary MVL inverter operation at a supply voltage of 2 V, without additional circuit complexity. The ternary-state formation mechanism is systematically analyzed based on the transfer characteristics of the constituent devices.

II. FABRICATION AND MEASUREMENT

We fabricated an ultralow-voltage ternary inverter consisting of an E*p*-AAT and a single *n*-type thin-film transistor (TFT). The E*p*-AAT devices were fabricated on SiO_2 (300 nm)/Si substrates with thermally evaporated Cr/Au gate electrodes (5/30 nm). A 15 nm thick HfO_2 gate dielectric was deposited by atomic layer deposition (ALD), followed by a 5 nm spin-coated PS layer. Prior to the PS deposition, the HfO_2 surface was treated with UV-ozone for 15 min to improve the surface wettability. The 5 nm-thick PS layer (Sigma-Aldrich, 182427) was then formed by spin-coating a 0.2 wt% solution in toluene at 6,000 rpm for 60 s. The film was subsequently annealed at 100 °C for 1 h under vacuum to remove the residual solvent. The resulting PS surface exhibited a smooth morphology with a root-mean-square (RMS) roughness of about 0.2 nm, as confirmed by atomic force microscopy, providing a uniform surface for the subsequent growth of the organic semiconductor layers. The *n*-type PhC_2H_4-benzo[de]isoquinolino[1,8-gh]quinolone diimide (PhC_2-BQQDI) and *p*-type 2,7-dioctyl [1]benzothieno-[3,2-b] [1]benzothiophene (C8-BTBT) organic semiconductors layers were thermally evaporated to thicknesses of 30 and 20 nm, respectively, followed by top Au electrodes (30 nm). All channels and electrodes were patterned using shadow masks, with channel lengths of 80 μm for the E*p*-AAT and 40 μm for the *n*-type TFT, enabling their direct interconnection and seamless formation of the inverter architecture in a single fabrication step.

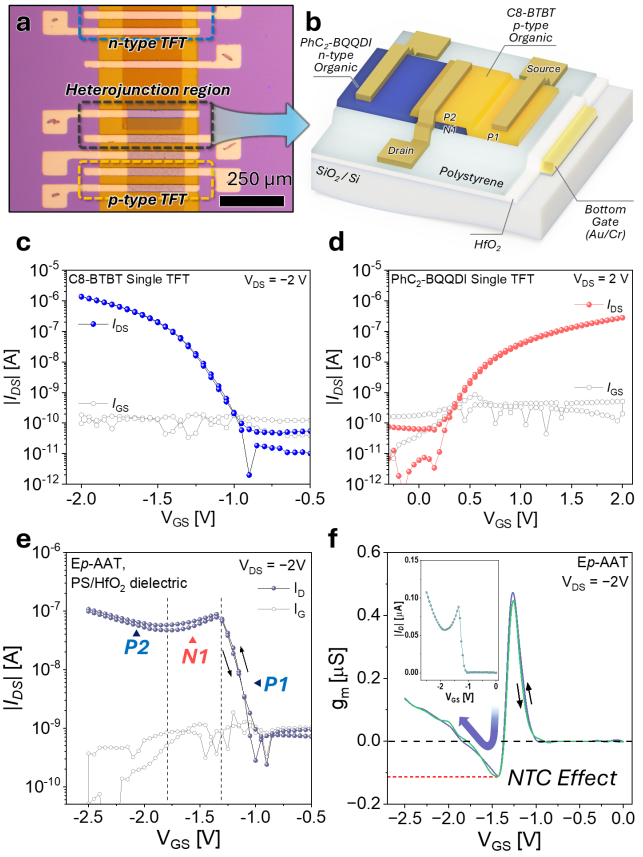


FIGURE 1. (a) Optical microscopy image and (b) schematic diagram of the HfO_2-based E*p*-AAT heterojunction device. Transfer characteristics, including drain current (I_{DS}) and gate current (I_{GS}), of single TFTs based on (c) *p*-type C8-BTBT and (d) *n*-type PhC_2-BQQDI. (e) Transfer characteristics of the E*p*-AAT device with a PS/HfO_2 gate dielectric, exhibiting an N-shaped curve. (f) Corresponding g_m characteristics and linear-scale transfer curve (inset).

III. RESULTS

We demonstrate a low-voltage E*p*-AAT employing a PS/HfO_2 gate dielectric stack for MVL circuit applications. The high dielectric constant of HfO_2 (k ≈ 20-25) enables low-voltage operation with reduced gate leakage [6]. In addition, the PS surface layer provides a hydrophobic interface for organic semiconductor deposition and stable channel formation by modifying the HfO_2 surface energy [5]. Fig. 1a and Fig. 1b show an optical microscopy image and a schematic diagram of the PS/HfO_2-based device, respectively. Unlike conventional AATs that exhibit a Λ-shaped transfer curve, the E*p*-AAT adopts a fully extended *p*-channel architecture in which heterojunctions are formed between the *n*-type channel (*N1*) and the *p*-type channels (*P1* and

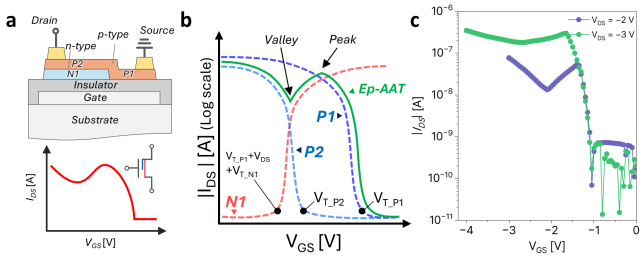


FIGURE 2. **(a) Device schematics and transfer characteristics of Ep-AAT. (b) Decomposition of the N-shaped transfer curve in Ep-AAT into N1, P1, and P2 contributions, explaining peak and valley formation with NTC effects. (c) Transfer characteristics of the Ep-AAT under different V_{DS} conditions (−2 and −3 V).**

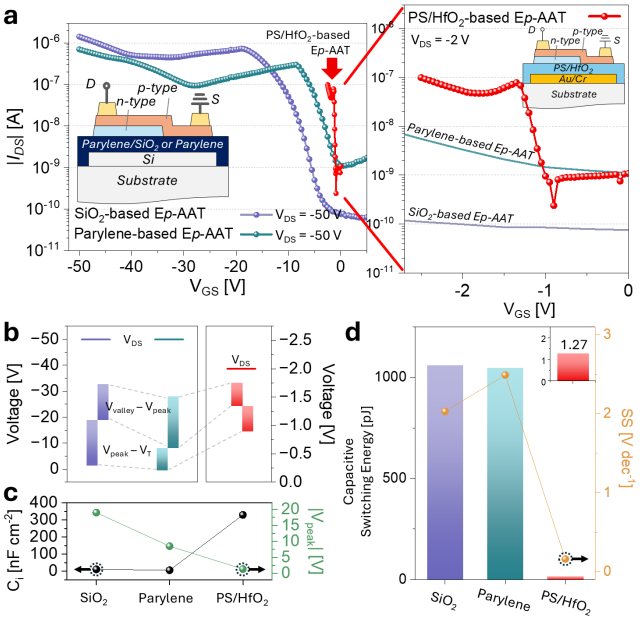


FIGURE 3. **(a) Transfer characteristics of Ep-AAT devices with SiO_2, parylene, and HfO_2 gate dielectrics. (b–d) Comparison of SiO_2-, parylene-, and PS/HfO_2-based Ep-AAT devices: (b) V_{DS} bias conditions and extracted V_{valley}, V_{peak}, and V_T, (c) C_i and $|V_{peak}|$, and (d) SS and capacitive switching energy.**

P2) along the source-drain direction. Here, *P1* denotes the bottom *p*-type channel, whereas *P2* denotes the upper *p*-type channel deposited on *N1*. The transfer characteristics of the individual organic transistors were first evaluated, as shown in Fig. 1c and Fig. 1d. The *p*- and *n*-type TFTs exhibited stable transfer behavior at drain-source voltage (V_{DS}) = −2 and 2 V, respectively, over the corresponding gate-source voltage (V_{GS}) ranges. The turn-on voltage (V_T) of the n-type TFT, denoted as VT_N1, was extracted to be approximately +0.4 V (Fig. 1d).

Next, the transfer characteristics of the E*p*-AAT device were measured. As shown in Fig. 1e, the device exhibits an N-shaped transfer characteristic with NTC behavior during the *p*-channel gate-bias sweep at V_{DS} = −2 V. The peak current appears near $V_{GS} \approx -1.35$ V, originating from the overlapping conduction of the *N1* and *P1* channels (*N1* ∩ *P1*) (Fig. 2a,b). Since *N1* exchanges electrons with the drain electrode, the gate voltage effectively applied to *N1* is $V_{GS} - V_{DS}$, so that *N1* remains in the accumulation state at $V_{GS} \approx -1.35$ V ($V_{GS} - V_{DS} = +0.65$ V > V_{T_N1}), whereas *P1* is controlled by the global V_{GS} with respect to the grounded source. With further gate bias, the drain current decreases and then increases again at more negative gate voltages ($V_{GS} < -2$ V) due to *P2* activation. The V_T of the *P2* (V_{T_P2}) is shifted more negatively than that of *P1* because the gate field must pass through the underlying *N1* layer. While *N1* is in accumulation, the accumulated electrons screen the gate field from *P2*. Once a depletion layer forms in *N1*, the gate field penetrates to *P2*, and the resulting potential redistribution across the stack makes the hole accumulation in *P2* occur at a more negative V_{GS}. As a result, the valley region appears between the cutoff of *N1* and the onset of *P2* conduction, and the overall transfer characteristic can be expressed as (*N1* ∩ *P1*) ∪ *P2*. Fig. 1f shows the corresponding characteristics in the transconductance (g_m) domain. The g_m curve peaks near $V_{GS} \approx -1.35$ V and reaches a minimum of −0.11 μS at the valley. A slight hysteresis observed along the falling and re-increasing regions around the valley (Fig. 1e) is attributed to weak interfacial traps between the N1 and P2 channels [5], [12], [13], as the gate dielectric interface is effectively passivated by the PS layer [14], [15], [16]. This hysteresis appears selectively in the region where the P2 conduction sets in, consistent with the N1/P2 heterointerface origin. It is well established that bare high-k oxide dielectrics such as HfO_2 and AlOx induce pronounced hysteresis in organic TFTs owing to trap states at and near the oxide surface [17], and that thin interlayers such as self-assembled monolayers or polymer films effectively shield the organic channel from these traps [18], [19]. Consistent with these reports, the forward and reverse sweeps of the PS-treated HfO_2 device nearly coincide except for the weak N1/P2 contribution described above (Fig. 1e).

To investigate the effect of dielectric-stack engineering on NTC operation, E*p*-AAT devices were fabricated with two reference dielectric configurations, a 15 nm parylene-treated SiO_2 (300 nm)/Si substrates and a local-gate structure with a 500 nm parylene gate dielectric. As shown in Fig. 3a, both devices exhibit typical N-shaped transfer characteristics but require a high V_{GS} of about −50 V because of the large dielectric thickness and low dielectric constant, limiting low-voltage MVL operation. Fig. 3b compares the voltage ranges of the two transition regions, from V_T to the peak current voltage (V_{peak}) and from V_{peak} to the valley current voltage (V_{valley}). In the optimized E*p*-AAT device, these ranges are reduced by up to 97.4% and 97.1%, respectively, demonstrating effective voltage scaling enabled by the high-k dielectric and interfacial surface modification. Fig. 3c shows the gate-dielectric capacitance per unit area (C_i) and $|V_{peak}|$ as a function of the gate dielectric. The PS/HfO_2-based

device exhibits a C_i of 330 nF·cm^{-2}, more than a 200-fold enhancement, greatly reducing the voltage required to reach the peak current. Based on these transfer characteristics and gate capacitance values, the subthreshold swing (SS) and capacitive switching energy of the E*p*-AAT devices were compared (Fig. 3d). The capacitive switching energy was estimated from the energy stored in the gate capacitor during a voltage transition and calculated using Equation (1) [20], [21],

$$Capacitive\ Switching\ Energy = \frac{1}{2}C_i WL(\Delta V)^2 \quad (1)$$

where W is the channel width, L is the channel length, and ΔV is the voltage swing between V_{peak} and V_{valley}. For the SiO_2- and parylene-based E*p*-AAT devices, W and L were 1000 μm and 100 μm, respectively. For the HfO_2-based E*p*-AAT device, W and L were 60 μm and 80 μm, respectively. The SS was extracted using Equation (2) [22],

$$SS = \left[\frac{dlog(I_D)}{d(V_{GS})}\right]^{-1} \quad (2)$$

where V_{GS} is the V_{GS} and I_{DS} is the drain current. Despite its larger C_i, the PS/HfO_2-based device achieves orders-of-magnitude lower switching energy owing to the reduced operating voltage and much smaller SS.

To further elucidate the drain-bias dependence of the NTC characteristics, the operation of the E*p*-AAT is analyzed in terms of the electrode-referenced channel configuration (Fig. 2a,b). Because the N1 channel exchanges electrons with the drain terminal, the biased drain acts as an effective source for N1, defining the effective V_{GS} applied to the N1 channel as $V_{GS,eff} = V_{GS} - V_{DS}$. Electron accumulation in the N1 channel occurs when $V_{GS,eff}$ exceeds V_{T_N1}, and the accumulation condition ($V_{GS} > V_{T_N1} + V_{DS}$) therefore translates along the V_{GS} axis by V_{DS}. At $V_{DS} = -2$ V, as V_{GS} is swept from 0 V to −2 V, $V_{GS,eff}$ decreases from + 2 V to 0 V, and the N1 channel is cut off at $V_{GS} = V_{T_N1} - 2$ V, at which point the drain current begins to decrease. The valley is subsequently formed at the onset of P2 conduction. When $|V_{DS}|$ increases to 3 V, $V_{GS,eff}$ remains above V_{T_N1} over the same V_{GS} range, and the cutoff point and the resulting valley are extended toward more negative gate voltages, to around $V_{GS} = V_{T_N1} - 3$ V. Furthermore, since the entire N1 characteristic translates along the V_{GS} axis by V_{DS}, the intersection between the N1 and P1 curves, which defines Vpeak, also shifts partially toward more negative V_{GS}.

The V_{DS} dependence was experimentally verified by measuring the identical E*p*-AAT device at $V_{DS} = -2$ and −3 V, which correspond to the supply voltages of the ternary inverter (Fig. 2c). As $|V_{DS}|$ increases from 2 V to 3 V, V_{valley} shifts from −2.35 V to −3.05 V, following the translation of the *N1* cutoff point by V_{DS}, whereas V_{peak} shifts only from −1.50 V to −1.75 V, as expected from its origin at the intersection of the *N1* and *P1* curves. In addition, I_{peak} and I_{valley} increase from 5.5×10^{-8} A to 2.0×10^{-7} A and from 5.7×10^{-9} A to 4.2×10^{-8} A, respectively, owing to the larger drain bias. These results confirm that the drain bias systematically modulates the NTC characteristics in accordance with the effective-source analysis.

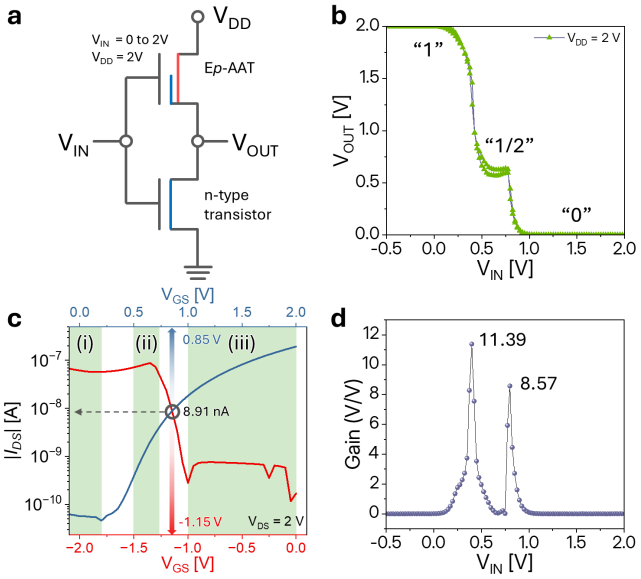


FIGURE 4. (a) Circuit schematic of the ultralow-voltage ternary MVL inverter. (b) Voltage transfer characteristics of the ternary inverter, showing three distinct logic states ("1", "1/2", and "0"). (c) Matched transfer characteristics of the E*p*-AAT and the *n*-type TFT on a logarithmic scale. (d) Voltage gain characteristics of the ternary inverter.

Furthermore, the fabricated device was integrated into a ternary MVL inverter. Fig. 4a shows the inverter configuration composed of a PS/HfO_2-based E*p*-AAT and an *n*-type transistor, where V_{IN} is applied to both device gates and V_{OUT} is measured at the common node. As shown in Fig. 4b, the voltage transfer characteristics (VTCs) clearly resolve three logic states, "1", "1/2", and "0", even at low operating voltage (V_{DD} = 2 V). The operating mechanism is explained by the matched transfer curves of the E*p*-AAT and the *n*-type TFT shown on a logarithmic scale in Fig. 4c. At low V_{IN} (range i), the V_{GS} of the *n*-type TFT is below its V_T (V_{T_N1}), while the V_{GS} of the E*p*-AAT approaches its V_{valley}. Under this condition, the E*p*-AAT dominates the circuit current, delivering V_{DD} to the output and yielding logic state "1". With increasing V_{IN} toward V_{peak}, the *n*-type TFT begins to conduct. At the same time, the current of the E*p*-AAT also increases. As a result, both devices contribute significantly to the output current, leading to voltage division and the intermediate logic state "1/2" in the intermediate V_{IN} region (range ii) of 0.5-0.75 V. Upon further increasing V_{IN}, the two transfer characteristics reach their intersection, beyond which the current of the *n*-type TFT exceeds that of the E*p*-AAT. This ultimately leads to the transition toward logic state "0" in range iii, as the *n*-type TFT becomes dominant and pulls the V_{OUT} toward ground while the E*p*-AAT is turned off. Although the relationship between the intersection point and the intermediate logic state observed in conventional CMOS inverters does not directly apply to our

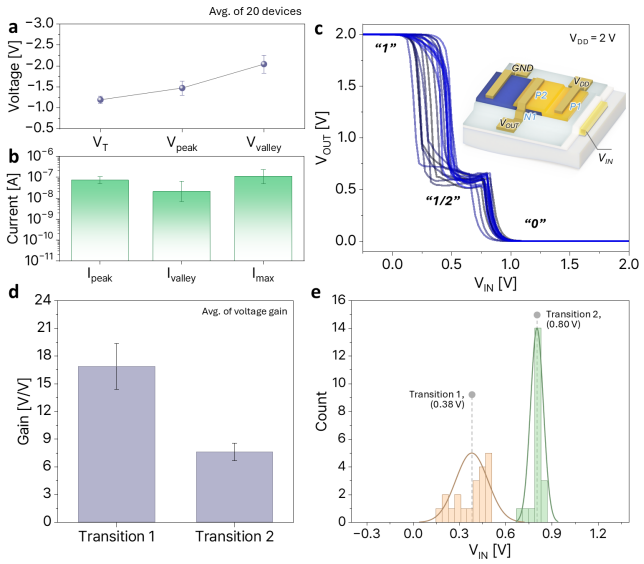


FIGURE 5. Statistical analysis of E*p*-AAT devices and ternary inverters. (a) Average values of the V_T, V_{peak}, and V_{valley} extracted from the transfer curves of the twenty E*p*-AAT devices. (b) Average values of I_{peak}, I_{valley}, and I_{max}. (c) Overlaid VTC curves of the twenty ternary inverters measured at V_{DD} = 2 V, exhibiting three distinct logic states ("1", "1/2", and "0") in all devices. The inset shows a schematic illustration of the ternary inverter configuration. (d) Average voltage gains of the first and second transitions extracted from the twenty VTCs. (e) Histograms of the two transition voltages with the corresponding Gaussian fits. Error bars in (a), (b), and (d) represent one standard deviation.

ternary MVL inverter, the intersection region is associated with the transition between the intermediate and logic "0" states, while the intermediate logic state itself arises from voltage division between the two devices. The voltage gain characteristics in Fig. 4d show distinct peaks at each logic transition, confirming sufficient signal discrimination.

To estimate the electrical response speed of the inverter, a characteristic switching time (t) was estimated from the charge-balance relationship using Equation (3) [23], [24],

$$t \approx \frac{C\Delta V_{OUT}}{I_{D,avg}}, \tag{3}$$

where C is the capacitance estimated from $C = C_i WL$, ΔV_{OUT} is the output-voltage swing, and $I_{DS,avg}$ is the average drain current within the switching region (V_{IN} = 0.3-0.825 V). Using the measured device parameters, the estimated switching time is approximately 3.35 ms, indicating an electrical response on the millisecond timescale under the constant-current approximation. This value represents a model-based estimate of the characteristic switching timescale rather than an experimentally measured rise/fall time or propagation delay.

To evaluate the statistical uniformity of the proposed device structure and fabrication process, we performed a statistical analysis on multiple devices. Fig. 5 summarizes the statistical distributions of the parameters extracted from twenty E*p*-AAT devices and twenty ternary inverters. From the transfer curves of the E*p*-AAT devices, the V_T together with the voltages (V_{peak}, V_{valley}) and currents (I_{peak}, I_{valley}) at the peak and valley points were extracted. The V_T was found to be -1.19 ± 0.09 V on average, while V_{peak} and V_{valley} were maintained within narrow distributions of -1.47 ± 0.17 V and -2.04 ± 0.21 V, respectively (Fig. 5a). Regarding the currents, I_{peak} and I_{valley} were extracted to be $6.7 \pm 2.0 \times 10^{-8}$ A and $3.2 \pm 2.2 \times 10^{-8}$ A, respectively. In addition, the maximum current at $V_{GS} = -3$ V (I_{max}) was $1.3 \pm 0.9 \times 10^{-7}$ A, verifying that the current re-increase driven by the P2 channel conduction after the valley appears consistently in all devices (Fig. 5b).

Furthermore, to quantify the reproducibility of the intermediate logic state, we statistically analyzed the output characteristics of the ternary inverters. Fig. 5c presents the overlaid VTCs of the twenty inverters, in which three distinct logic states are commonly observed in all measured curves. Based on these curves, the deviation ranges of the inverter gain and the intermediate state level were extracted. Each VTC exhibits two transitions, and the gains of the first and second transitions were extracted to be 16.9 ± 2.5 V/V and 7.6 ± 0.9 V/V, respectively, across the twenty curves (Fig. 5d). The intermediate state level, defined as the output voltage at the flattest point of the intermediate plateau where $|dV_{OUT}/dV_{IN}|$ is minimized between the two gain peaks, was 0.592 ± 0.047 V, corresponding to a relative variation of about 8%. This confirms that a distinct intermediate state is reproducibly formed in every device. Moreover, the histograms of the two transition voltages (Fig. 5e) show that the two distributions are clearly separated without overlap, confirming that the three logic states are distinguished not only within a single inverter but also across the entire set of devices. These results demonstrate consistent ternary MVL inverter operation across twenty devices without additional circuit complexity.

IV. CONCLUSION

In summary, we demonstrated an ultralow-voltage ternary inverter based on an E*p*-AAT with an engineered dielectric stack. The E*p*-AAT exhibits an intrinsic N-shaped transfer characteristic with a clear NTC region, arising from its fully extended *p*-channel architecture and the combined contributions of the *N1*, *P1*, and *P2* channels. This characteristic enables three logic states, "1", "1/2", and "0", without additional circuit complexity, with distinct voltage-gain peaks at each transition. Transfer-characteristic analysis further clarifies the ternary-state formation mechanism. Future work will address time-resolved transient characterization to clarify the dynamic circuit performance, including rise/fall behavior, propagation characteristics, and frequency-dependent operation, as well as additional processes such as top encapsulation to further enhance the operational stability. These results suggest that PS/HfO_2-based organic E*p*-AATs are promising compact and energy-efficient building blocks for next-generation low-voltage MVL circuits.

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(Juhyung Seo and Jihyun Shin contributed equally to this work.)

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